Solving Linear and Quadratic Programs with an Analog Circuit

Sergey Vichik, Francesco Borrelli
Department of Mechanical Engineering, University of California, Berkeley, 94720-1740, USA,
{sergv,fborrelli}@berkeley.edu.

Submitted to: CACE Special Issue: From Resiliency and Robustness to Model-based Control. A Tribute to Manfred Moraris Decades-spanning Contributions to the Field of Process Systems Engineering

Abstract

We present the design of an analog circuit which solves linear programming (LP) or Quadratic Programming (QP) problems. In particular, the steady-state circuit voltages are the components of the LP (QP) optimal solution. The paper shows how to construct the circuit and provides a proof of equivalence between the circuit and the LP (QP) problem. The proposed method is used to implement an LP-based Model Predictive Controller by using an analog circuit. Simulative and experimental results show the effectiveness of the proposed approach.

Keywords: optimization, MPC, linear programming, quadratic programming, analog computation, linear complementarity systems

1. Introduction

In 2002, Bemporad, Morari, Dua, and Pistikopoulos showed how to compute the solution to constrained finite-time optimal control problems for discrete-time linear systems as a piecewise affine state-feedback law (Bemporad et al., 2002b). Such a law is computed off-line by using a multi-parametric programming solver which divides the state space into polyhedral regions, and for each region determines the linear gain and offset which produces the optimal control action. This state-feedback law is often referred to as the "explicit solution". Since many control problems belong to this class, either in their natural form or after an approximation and abstraction step, their solution has been studied for decades. However, until that work, as there was no knowledge about the functional form and structure of closed form solutions, computations resorted to some approximation such as gridding or functional interpolation.

Enlightened by that breakthrough, Morari's research group started developing a new theory for optimal control of discrete-time linear systems, constrained linear systems, and hybrid systems. The theory 1) unveils the existence and the properties of the closed form solutions (Borrelli, 2003; Maeder et al., 2009; Borrelli et al., 2005; Grieder et al., 2004; Bemporad et al., 2003; Morari et al., 2003; Bemporad et al., 2002a), 2) explains the effect of uncertainties on the control of constrained systems (Borrelli, 2003; Bemporad et al., 2003), 3) shows how to use linear and nonlinear multiparametric-programming to compute the closed forms solutions (Bemporad et al., 2002a; Borrelli et al., 2003; Bageshwar and Borrelli, 2009), 4) sheds light on the tight link between the desired optimality and the robustness of closed-loop systems and what can actually be achieved on resource-constrained embedded control hardware (in terms of CPU and storage) (Borrelli et al., 2010, 2009). The theory also simplifies and unifies much of the previous work for special classes of systems. In particular, it reduces to the well known Linear Quadratic Regulator for unconstrained linear systems. As an example, now we know the answer to the question "What is the solution to an LQR problem if the system states and inputs are constrained?". In (Borrelli et al., 2005) it was shown that the state feedback control law is continuous and piecewise affine and that the value function is convex and continuously differentiable. For hybrid systems, it was also shown that the optimal control law is, in general, piecewise affine over non-convex and disconnected sets. The class of hybrid systems for which these results apply is very large including systems with both internal and/or controllable switches (Borrelli et al., 2010).

These results have had important consequences for the implementation of Model Predictive Control (MPC) laws. Pre-computing offline the explicit piecewise affine feedback policy reduces the on-line computation for the receding horizon control law to a function evaluation, therefore avoiding the on-line solution of a mathematical program as it is done in Model Predictive Control. This research has enlarged in a very significant way the scope of applicability of Model Predictive Control to small-size/fast-sampled applications (Borrelli, 2003; Avni et al., 2006; Falcone et al., 2007). Since then, Prof. Morari's group and his collaborators have continued to push the capabilities of MPC to faster processes. Recently, using the capabilities of field

programmable gate array (FPGA) they have reached sampling times below five microseconds for problems with tens to a few hundreds of variables (Jerez et al., 2012; Mariéthoz et al., 2009, 2012; Jerez et al., 2013).

To honor this fundamental work, we have chosen to dedicate our original contribution to Professor Morari. In this paper we prove that Model Predictive Control can be implemented by using a simple analog circuit. We hope that this discovery will significantly enlarge the scope of applicability of Model Predictive Control. In fact, the proposed approach and technology could enable the real-time implementation of MPC controllers on the order of nanoseconds with very small power consumption if a VLSI (Very Large Scale Integrated) circuit technology is used.

Analog circuits for solving optimization problems have been extensively studied in the past (Dennis, 1959; Tank and Hopfield, 1986; Kennedy and Chua, 1988). Our renewed interests stem from MPC (Garcia et al., 1989; Mayne et al., 2000). In MPC at each sampling time, starting at the current state, an open-loop optimal control problem is solved over a finite horizon. The optimal command signal is applied to the process only during the following sampling interval. At the next time step, a new optimal control problem based on new measurements of the state is solved over a shifted horizon. The optimal solution relies on a dynamic model of the process, respects input and output constraints, and minimizes a performance index. When the model is linear and the performance index is based on two-norm, one-norm or ∞-norm, the resulting optimization problem can be cast as a linear program (LP) or a quadratic program (QP), where the state enters the right hand side (rhs) of the constraints.

We present the design of an analog circuit whose steady state voltages are the LP/QP optimizers. Thevenin's Theorem is used to prove that the proposed design yields a passive circuit. Passivity and KKT conditions of a tailored Quadratic Program are used to prove that the analog circuit solves the associated LP or QP. The proposed analog circuit can be used to repeatedly solve LPs or QPs with varying rhs and therefore it is suited for a linear MPC controller implementation. For some classes of applications the suggested implementation can be faster, cheaper and consume less power than digital implementation. A comparison to existing literature reveals that the proposed circuit is simpler and faster than previously published designs.

The paper is organized as follows. Existing literature is discussed in Section 2. We show how to construct an analog circuit from a given LP in Section 3. Section 4 proves the equivalence between the LP and the circuit. Section 6 shows how to extend the LP results to solve QP problems. Simulative and experimental results show the effectiveness of the approach in Section 7. Concluding remarks are presented in Section 8.

2. Previous Work on Analog Optimization

2.1. Optimization problems and electrical networks

Consider the linear programming (LP) problem

$$\min_{V=[V_1,\dots,V_n]^T} c^T V \tag{1a}$$

$$\text{s.t.} \quad A_{\text{eq}} V = b_{\text{eq}} \tag{1b}$$

$$A_{\text{ineq}} V \leq b_{\text{ineq}} \tag{1c}$$

where $[V_1, \dots, V_n]$ are the optimization variables, A_{ineq} and A_{eq} are matrices, and c, b_{eq} and b_{ineq} are column vectors. The equality and inequality operators are element-wise operators.

The monograph by J. Dennis (Dennis, 1959) presents an analog electrical network for solving an LP (1). In Dennis's work, the primal and dual optimization variables are represented by the circuit currents and voltages, respectively. A basic version of Dennis's circuit consists of resistors, current sources, voltage sources, and diodes. In this, circuit each element value of matrices A_{ineq} and A_{eq} is equal to the number of wires that are connected to a common node. Therefore, this circuit is limited to problems where the matrices A_{ineq} and A_{eq} contain only small integer values. An extended version of the circuit includes a multiport DC-DC transformer and can represent arbitrary matrices A_{ineq} and A_{eq}. Current distribution laws in electrical networks (also known as minimum dissipation of energy principle or Kirchoff's laws) are used to prove that the circuit converges to the solution of the optimization problem. This work had limited practical impact due to difficulties in implementing the circuit, and especially in implementing the multiport DC-DC transformer.

In later work, Chua et al. (1982) showed a different and more practical way to realize the multiport DC-DC transformer using operational amplifiers. In subsequent works, Chua (Kennedy and Chua, 1988; Chua and Lin, 1984) and Hopfield (Tank and Hopfield, 1986) proposed circuits to solve non-linear optimization problems of the form

$$\begin{aligned} &\min_x \ f(x) \\ &\text{s.t. } g_j(x) \leq 0, \ j = 1 \dots m, \end{aligned} \tag{2}$$

where $x \in \mathbb{R}^n$ is the vector of optimization variables, $f(x)$ is the cost function, and $g_j(x)$ are the m constraint functions. The LP (1) was solved as a special case of problem (2) (Kennedy and Chua, 1988; Tank and Hopfield, 1986). The circuits proposed by Chua, Hopfield, and coauthors model the Karush-Kuhn-Tucker (KKT) conditions by representing primal variables as capacitor voltages and dual variables as currents. The dual variables are driven by the inequality constraint violations using high gain amplifiers. The circuit capacitors are charged with a current proportional to the gradient of the Lagrangian of prob-

lem (2)

$$\frac{\partial x_i}{\partial t} = -\left[\frac{\partial f(x)}{\partial x_i} + \sum_{j=1}^{m} I_j \frac{\partial g_j(x)}{\partial x_i}\right], \tag{3}$$

where $\frac{\partial x_i}{\partial t}$ is the capacitor voltage derivative and I_j is the current corresponding to the j-th dual variable. The derivatives $\frac{\partial f}{\partial x_i}$ and $\frac{\partial g_j}{\partial x_i}$ are implemented by using combinations of analog electrical devices (Jackson, 1960). When the circuit reaches an equilibrium, the capacitor charge is constant ($\frac{\partial x_i}{\partial t} = 0$) and Eq. (3) becomes one of the KKT conditions. The authors prove that their circuit always reaches an equilibrium point that satisfies the KKT conditions. This is an elegant approach since the circuit can be intuitively mapped to the KKT equations. However, the time required for the capacitors to reach an equilibrium is non-negligible. This might be the reason for the relatively large settling time reported to be "tens of milliseconds" for those circuits in (Kennedy and Chua, 1988).

2.2. Applying analog circuits to MPC problems

The analog computing era declined before the widespread use of Model Predictive Control. Quero, Camacho, and Franquelo (1993) have been the first to study the implementation of analog MPC. They use the Hopfield circuit proposed in (Tank and Hopfield, 1986) to implement an MPC controller. The approach they propose is validated with an experimental circuit which reaches the equilibrium after a transient of 1.8 msec.

More recently in (Palusinski et al., 2001), fast analog PI controllers are implemented on an Anadigm's Field Programmable Analog Array (FPAA) device (Anadigm, 2013) for an application involving a fast chemical microreactor. An FPAA is an integrated device containing configurable analog blocks and configurable block interconnections. The analog circuit designed in (Palusinski et al., 2001) has a computation time that is faster than that of a digital controller implementing the PI controller. The article briefly proposes to use an FPAA for MPC without specifying details. To the best of the authors knowledge, no further work has been published in this direction.

3. LP Analog Circuit

Without loss of generality, we assume that A_{ineq}, A_{eq} and c have non-negative entries. Any LP (1) can be transformed into this form by introducing an auxiliary vector $\bar{V}$ as follows:

$$\begin{aligned} \min_{\bar{V},V} \quad & {c^+}^T V + {c^-}^T \bar{V} \\ \text{s.t.} \quad & A^+_{\text{eq}} V + A^-_{\text{eq}} \bar{V} = b_{\text{eq}} \\ & A^+_{\text{ineq}} V + A^-_{\text{ineq}} \bar{V} \leq b_{\text{ineq}} \\ & V + \bar{V} = 0 \end{aligned}$$

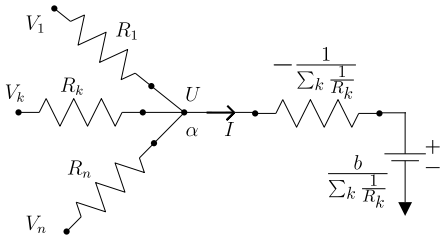

Figure 1: Equality enforcing circuit consisting of n resistors ($R_1 \dots R_n$), a negative resistance, and a reference voltage.

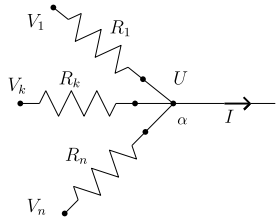

Figure 2: A node with n connected wires.

where A_{ineq}, A_{eq}, and c are split into positive and negative parts ($A_{\text{ineq}} = A^+_{\text{ineq}} - A^-_{\text{ineq}}$, $A_{\text{eq}} = A^+_{\text{eq}} - A^-_{\text{eq}}$ and $c = c^+ - c^-$).

In the beginning of this section, we present the basic building blocks which will be later used to create a circuit that solves problem (1). The first basic block enforces equality constraints of the form (1b). The second building block enforces inequality constraints of the form (1c). The last basic block implements the cost function.

3.1. Equality constraint

Consider the circuit depicted in Fig. 1. V_k is the potential of node k, R_k is the resistance between node k and the common node α with potential U, $-\frac{1}{\sum_k \frac{1}{R_k}}$ is a negative resistance, and $\frac{b}{\sum_k \frac{1}{R_k}}$ is a constant voltage source.

Proposition 1 (Equality constraint circuit)**.** *The circuit in Fig. 1 enforces the equality constraint*

$$\begin{bmatrix} \frac{1}{R_1} & \cdots & \frac{1}{R_n} \end{bmatrix} \begin{bmatrix} V_1 \\ \vdots \\ V_n \end{bmatrix} = b. \tag{5}$$

Proof. Consider the circuit depicted in Fig. 2. In this circuit, n wires are connected to a common node. We call this common node α, its potential U, and the current that exits this node I. Kirchhoff's current law (KCL) implies

$$\sum_{k=1}^{n} I_k = \sum_{k=1}^{n} \frac{V_k - U}{R_k} = I, \tag{6}$$

where I_k is the current through branch k, and R_k is the resistance between node k and node α. Eq. (6) can be written as an equality constraint on potentials V_k,

$$\sum_{k=1}^{n} \frac{V_k}{R_k} = I + U \sum_{k=1}^{n} \frac{1}{R_k}. \tag{7}$$

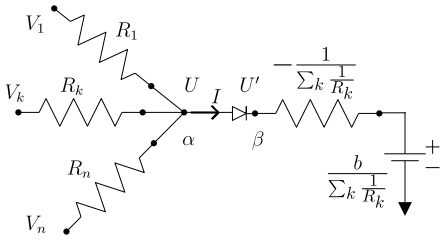

Figure 3: Inequality enforcing circuit.

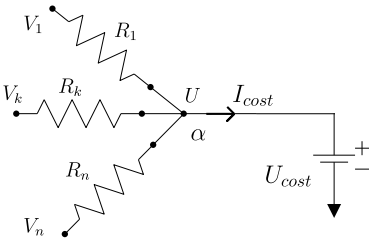

Figure 4: Cost circuit.

If the right hand side (rhs) of (7) is set to any desired value b, then (7) enforces an equality constraint on a linear combination of V_k. The voltage U is set to

$$U = -\frac{I}{\sum_{k=1}^{n} \frac{1}{R_k}} + \frac{b}{\sum_{k=1}^{n} \frac{1}{R_k}}. \tag{8}$$

The rhs in (8) is implemented by a negative resistance of $-\frac{1}{\sum_{k=1}^{n} \frac{1}{R_k}}$ and a constant voltage source of $\frac{b}{\sum_{k=1}^{n} \frac{1}{R_k}}$. Eq. (8) together with (7) yield the desired (5). Therefore, the circuit shown in Fig. 1 enforces (5). □

Note that the negative resistance $-\frac{1}{\sum_k \frac{1}{R_k}}$ in the circuit in Fig. 1 can be realized by using an operational amplifier (Chen, 2002, pp. 395-397).

3.2. Inequality constraint

Consider the circuit shown in Fig. 3. Similarly to the equality constraint circuit, n wires are connected to a common node α. α's potential is U and the current exiting this node is I. An ideal diode connects node α to node β. The potential of node β is U'.

Proposition 2 (Inequality constraint circuit)**.** *The circuit in Fig. 3 enforces the inequality constraint*

$$\begin{bmatrix} \frac{1}{R_1} & \dots & \frac{1}{R_n} \end{bmatrix} \begin{bmatrix} V_1 \\ \vdots \\ V_n \end{bmatrix} \leq b. \tag{9}$$

Proof. Kirchhoff's current law (KCL) implies (6) as in the previous case. The diode enforces $U' \geq U$. In Fig. 3, the voltage U' can be computed as follows

$$U' = \frac{b - I}{\sum_{k=1}^{n} \frac{1}{R_k}} \geq U. \tag{10}$$

Eq. (6) and $U \leq U'$ yield

$$\sum_{k=1}^{n} \frac{V_k}{R_k} = I + U \sum_{k=1}^{n} \frac{1}{R_k} \leq I + U' \sum_{k=1}^{n} \frac{1}{R_k} = b, \tag{11}$$

which can be compactly rewritten as (9). Therefore, the circuit shown in Fig. 3 enforces (9).

□

The diode in Fig. 3 enforces

$$I \geq 0, \tag{12a}$$
$$I(U - U') = 0. \tag{12b}$$

By using (10) and rearranging its terms, (12b) can be rewritten as:

$$I \left(\left(\sum_{k=1}^{n} \frac{1}{R_k} \right) U - b + I \right) = 0. \tag{13}$$

Eq. (13) will be used later in Section 4 to characterize the LP circuit.

3.3. Cost function

Consider the circuit in Fig. 4. In this circuit the potential of node α is equal to U_{cost} and the current that exits the node is I_{cost}. From (7) we have

$$c^T V = I_{\text{cost}} + U_{\text{cost}} \sum_{k=1}^{n} \frac{1}{R_k} \triangleq J. \tag{14}$$

where $c = [1/R_1 \ \dots \ 1/R_n]^T$, $V = [V_1 \ \dots \ V_n]^T$ and J is the cost function. This part of the circuit implements the minimization of the cost function. A thorough explanation of the cost circuit requires the equations of the whole LP circuit which will be presented in Section 4.2. Here we present a brief intuitive interpretation.

Later we will show that the LP circuit is passive. This implies that when U_{cost} is set to a low value, the voltages V_k are driven in a direction that minimizes the current I_{cost}. Consequently, the cost J is decreased by decreasing U_{cost}.

3.4. Connecting the basic circuits

This section presents how to construct the circuit that solves a general LP. We construct the conductance matrix $G \in \mathbb{R}^{(m+1)\times n}$ as

$$G \triangleq \begin{bmatrix} c^T \\ A \end{bmatrix} = \begin{bmatrix} c^T \\ A_{\text{eq}} \\ A_{\text{ineq}} \end{bmatrix}, \tag{15}$$

and denote G_{ij} as the i, j element of G. For a given LP (1), the R_{ij} resistor is defined as

$$R_{ij} \triangleq \frac{1}{G_{ij}}, \ i = 0, \dots m, \quad j = 1, \dots, n, \tag{16}$$

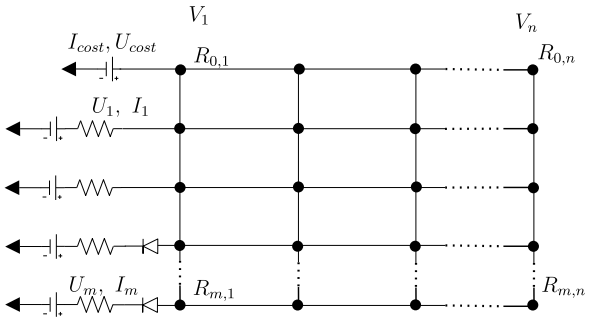

Figure 5: Electric circuit solving an LP. Vertical wires are variable nodes with potentials $V_1 \dots V_n$. Black dots represent resistances that connects vertical and horizontal wires. Horizontal wires are cost or constraint nodes. Each horizontal wire is connected to a ground via a negative resistance, a constant voltage source and a diode for inequalities nodes. The topmost horizontal wire is the cost circuit which is connected to a constant voltage source.

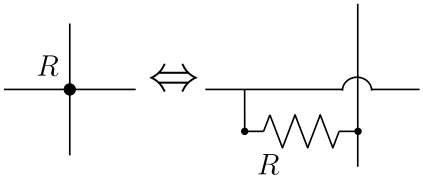

Figure 6: Compact representation of a resistor.

where the first row of G (corresponding to c^T) is indexed by $i = 0$.

Consider the circuit shown in Fig. 5. The circuit is shown using a compact notation where each resistor R_{ij} is represented by a dot, vertical wires represent variable nodes with potentials $V_1 \dots V_n$ and horizontal wires represent *constraint nodes*. The compact representation of a resistor through the dot symbol is clarified in Fig. 6. If $G_{ij} = 0$, then no resistor is present at the corresponding dot.

The LP circuit is constructed by connecting the nodes associated with the variables $V_1 \dots V_n$ to all three types of the basic circuits: equality, inequality and cost. We will refer to such nodes as *variable nodes*. Each row of the circuit in Fig. 5 is one of the basic circuits presented in Sections 3.1, 3.2 and 3.3. We claim that, if U_{cost} is "small enough", then the values of the potentials $V_1 \dots V_n$ in this circuit are a solution of (1). This claim is proven in the next section.

Remark 1. *Note that one can easily change the rhs of equality constraints* (5) *or/and inequality constrains* (9) *to a different value* $\bar{b}$ *by simply using a voltage source equal to* $\bar{b}/\sum_{k=1}^{n} \frac{1}{R_k}$. *This allows one to solve parametric problems by simply changing the value of the external voltage sources.*

The circuit as shown in Fig. 5 contains no dynamic elements such as capacitors or inductors. Therefore, the time required to reach steady-state is governed by the parasitic effects (e.g. wires inductance and capacitance) and by the properties of the elements used to realize negative resistance (usually opamp) and diode. Hence, a good electronic design can achieve solution times on the order of these parasitic effects. Indeed, our preliminary results of ongoing work on VLSI implementation indicate that time constants can be as low as a few nanoseconds.

4. Steady-State Analysis of the LP Circuit

Consider the LP circuit in Fig. 5 with R_{ij} defined by Eqs. (15)-(16). In this section we show that there exists a range of U_{cost} values such that the LP circuit in Fig. 5 solves the optimization problem (1). In particular, the steady-state circuit voltages are the components of an LP optimal solution. First, we derive the steady state equations of the electric circuit and then we show the equivalence.

4.1. Steady state solution

Consider the circuit in Fig. 5. Let $U = [U_1, \dots, U_m]^T$ be the voltages of the constraint nodes as shown on Fig. 5. By applying the KCL (Kirchhoff's current law) to every variable node with potential $V_1, \dots, V_n$, we obtain

$$G_{0,j}(U_{\text{cost}} - V_j) + \sum_{i=1}^{m} G_{i,j}(U_i - V_j) = 0, \quad j = 1, \dots, n \tag{17}$$

which can be rewritten in the matrix form

$$\begin{bmatrix} c_1 & . & c_n \\ A_{11} & . & A_{1n} \\ \vdots & . & \vdots \\ A_{m1} & . & A_{mn} \end{bmatrix}^T \begin{bmatrix} U_{\text{cost}} \\ U_1 \\ \vdots \\ U_m \end{bmatrix} = \begin{bmatrix} (\sum_{i=0}^{m} G_{i,1})V_1 \\ \vdots \\ (\sum_{i=0}^{m} G_{i,n})V_n \end{bmatrix}. \tag{18}$$

Eq. (18) can be compactly written as

$$cU_{\text{cost}} + A^T U = \text{diag}(c^T + \mathbf{1}^T A)V, \tag{19}$$

where m is the number of equality and inequality constraints, $\mathbf{1}$ is a vector of ones, and $\text{diag}(x)$ is a diagonal matrix with x on its diagonal.

Next, we apply KCL on all nodes with potentials $[U_{\text{cost}}, U_1, \dots, U_m]$ to obtain

$$\sum_{j=1}^{n} c_j(U_{\text{cost}} - V_j) = I_{\text{cost}} \tag{20}$$

$$\sum_{j=1}^{n} G_{i,j}(U_i - V_j) = I_i, \qquad i = 1, \dots, m, \tag{21}$$

which can be written in the matrix form

$$\begin{bmatrix} c_1 & . & c_n \\ A_{11} & . & A_{1n} \\ \vdots & . & \vdots \\ A_{m1} & . & A_{mn} \end{bmatrix} \begin{bmatrix} V_1 \\ \vdots \\ V_n \end{bmatrix} = \begin{bmatrix} U_{\text{cost}} \sum_{j=1}^{n} c_j \\ U_1 \sum_{j=1}^{n} A_{1,j} \\ \vdots \\ U_m \sum_{j=1}^{n} A_{m,j} \end{bmatrix} + \begin{bmatrix} I_{\text{cost}} \\ I \end{bmatrix}, \tag{22}$$

where $I = [I_1 \ \dots \ I_n]$. Eq. (22) can be compactly rewritten as

$$c^T V = \mathbf{1}^T c U_{\text{cost}} + I_{\text{cost}} \tag{23a}$$
$$AV = \text{diag}\left(\mathbf{1}^T A^T\right) U + I. \tag{23b}$$

The equality voltage regulator law (8) and the inequality law (10) can be compactly written as

$$\text{diag}\left(\mathbf{1}^T A_{\text{eq}}^T\right) U_{\text{eq}} = b_{\text{eq}} - I_{\text{eq}} \tag{24a}$$
$$\text{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right) U_{\text{ineq}} \leq b_{\text{ineq}} - I_{\text{ineq}}. \tag{24b}$$

By substituting (24) into (23b), we obtain

$$A_{\text{eq}} V = b_{\text{eq}} \tag{25a}$$
$$A_{\text{ineq}} V \leq b_{\text{ineq}}. \tag{25b}$$

Substitution of (23b) for inequalities to the diode constraint (13) yields

$$\left[A_{\text{ineq}} V - b_{\text{ineq}}\right]_i \left[I_{\text{ineq}}\right]_i = 0, \ \forall i \in \mathcal{I}, \tag{26}$$

where $\mathcal{I}$ is the set of all inequality constraints.

We collect (19), (23), (25), and (12a) into one set of equations which characterize the circuit

$$AV = \text{diag}\left(\mathbf{1}^T A^T\right) U + I \tag{27a}$$
$$c U_{\text{cost}} + A^T U = \text{diag}(c^T + \mathbf{1}^T A) V \tag{27b}$$
$$A_{\text{eq}} V = b_{\text{eq}} \tag{27c}$$
$$A_{\text{ineq}} V \leq b_{\text{ineq}} \tag{27d}$$
$$I_{\text{ineq}} \geq 0 \tag{27e}$$
$$\left[A_{\text{ineq}} V - b_{\text{ineq}}\right]_i \left[I_{\text{ineq}}\right]_i = 0, \forall i \in \mathcal{I} \tag{27f}$$
$$c^T V = \mathbf{1}^T c U_{\text{cost}} + I_{\text{cost}}, \tag{27g}$$

where U, I, I_{cost} and V are the unknowns. The voltage U_{cost} of the cost node is set externally.

4.2. Equivalence of the optimization problem and the electric circuit

We consider the following assumptions.

Assumption 1. *The LP* (1) *is feasible and the feasible set is bounded.*

Assumption 2. *The dual of LP* (1) *is feasible and the set of dual optimal solutions is bounded.*

Assumption 3. *In the LP* (1)*, G is non-negative, $\mathbf{1}^T G > 0$ and $\mathbf{1}^T G^T > 0$.*

Theorem 1 (LP circuit equivalence)**.** *Let Assumptions 1-3 hold. Then, there exists U_{cost}^{crit}, such that a solution V^* to* (27) *is also an optimizer of the LP* (1) *for all $U_{cost} \leq U_{cost}^{crit}$.*

Theorem 1 will be proven in the following way: first we claim that the Eqs. (27a)-(27f) have a solution when the cost function is not present ($c = 0$); second, we show that there exists $U_{\text{cost}}^{\text{crit}}$ such that any solution to (27) is also an LP solution; third, we show that for all $U_{\text{cost}} \leq U_{\text{cost}}^{\text{crit}}$ any solution to (27) is also an LP solution.

As explained earlier in this paper, the assumption on the non-negativity of G in Theorem 1 is not restrictive. Also, $\mathbf{1}^T G > 0$ and $\mathbf{1}^T G^T > 0$ are always satisfied for LP problems without zero rows or zero columns.

In Theorem 1, we require that the sets of primal optimal and dual optimal solutions are bounded. This can be guaranteed if the primal feasible set is bounded and linear independence constraint qualification (LICQ) (Hestenes, 1966, p. 29) holds.

Remark 2. *In Theorem 1, we require the LP to be primal and dual feasible. This requirement may be relaxed by using a different LP formulation, such as the big-M two-phase simplex method (Bertsimas and Tsitsiklis, 1997, p. 117) or a homogeneous self-dual problem (Ye et al., 1994).*

4.3. Proof of Theorem 1

Consider an electric circuit with constraint sub circuits and no cost sub circuit. Such an electric circuit is characterized by Eqs. (27a)-(27f) with $c = 0$.

Lemma 1 (Existence of solution to a zero-cost circuit)**.** *Let Assumption 1 hold. Assume that A is non-negative, $\mathbf{1}^T A > 0$ and $\mathbf{1}^T A^T > 0$. Then, the Eqs.* (27a)-(27f) *have a solution when $c = 0$.*

Proof. First we rearrange (27a)-(27f). Eq. (27a) can be split into equality and inequality parts

$$A_{\text{eq}} = \text{diag}\left(\mathbf{1}^T A_{\text{eq}}^T\right) U_{\text{eq}} + I_{\text{eq}} \tag{28}$$
$$A_{\text{ineq}} = \text{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right) U_{\text{ineq}} + I_{\text{ineq}}. \tag{29}$$

Eq. (27b) can be rewritten as

$$A_{\text{eq}}^T U_{\text{eq}} + A_{\text{ineq}}^T U_{\text{ineq}} = \text{diag}\left(\mathbf{1}^T A\right) V. \tag{30}$$

Therefore, (27a)-(27f) can be written as

$$A_{\text{eq}}V = \text{diag}\left(\mathbf{1}^T A_{\text{eq}}^T\right) U_{\text{eq}} + I_{\text{eq}} \tag{31a}$$
$$A_{\text{ineq}}V = \text{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right) U_{\text{ineq}} + I_{\text{ineq}} \tag{31b}$$
$$A_{\text{eq}}^T U_{\text{eq}} + A_{\text{ineq}}^T U_{\text{ineq}} = \text{diag}\left(\mathbf{1}^T A\right) V \tag{31c}$$
$$A_{\text{eq}}V = b_{\text{eq}} \tag{31d}$$
$$A_{\text{ineq}}V \leq b_{\text{ineq}} \tag{31e}$$
$$I_{\text{ineq}} \geq 0 \tag{31f}$$
$$\left(A_{\text{ineq}}V - b_{\text{ineq}}\right)_i I_{\text{ineq}_i} = 0,\ \forall i \in \mathcal{I}. \tag{31g}$$

Next, consider the following quadratic program (QP)

$$\begin{aligned} &\min_V \ \frac{1}{2} V^T Q V \\ &s.t.\ A_{\text{eq}}V = b_{\text{eq}} && \text{(32a)} \\ &\quad\ A_{\text{ineq}}V \leq b_{\text{ineq}}, && \text{(32b)} \end{aligned}$$

From Assumption 1, Problem (32) has a finite solution for any Q because the feasibility domain is bounded and not empty. The value of Q will be selected later. We use this problem to find a solution to (27a)-(27f). The KKT conditions are necessary optimality conditions for problems with linear constraints (Bazaraa et al., 2006, Theorem 5.1.3). Therefore, there exist $V^\star$, $\mu^\star$, $\lambda^\star$ which satisfy the KKT conditions

$$A_{\text{eq}}^T \mu^\star + A_{\text{ineq}}^T \lambda^\star + QV^\star = 0 \tag{33a}$$
$$A_{\text{eq}}V^\star = b_{\text{eq}} \tag{33b}$$
$$A_{\text{ineq}}V^\star \leq b_{\text{ineq}} \tag{33c}$$
$$\lambda^\star \geq 0 \tag{33d}$$
$$\left(A_{\text{ineq}}V^\star - b_{\text{ineq}}\right)_i \lambda_i^\star = 0,\ i \in \mathcal{I}, \tag{33e}$$

where $\mu^\star$ and $\lambda^\star$ are the dual variables of the QP (32).

We choose Q, $U_{\text{eq}}^\star$, $U_{\text{ineq}}^\star$, $I_{\text{eq}}^\star$ and $I_{\text{ineq}}^\star$ as described by the following equations.

$$\begin{aligned} Q = &\,\text{diag}\left(\mathbf{1}^T A\right) - A_{\text{eq}}^T \,\text{diag}\left(\mathbf{1}^T A_{\text{eq}}^T\right)^{-1} A_{\text{eq}} \\ &- A_{\text{ineq}}^T \,\text{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right)^{-1} A_{\text{ineq}} && \text{(34a)} \end{aligned}$$
$$I_{\text{eq}}^\star = \text{diag}\left(\mathbf{1}^T A_{\text{eq}}^T\right) \mu^\star \tag{34b}$$
$$U_{\text{eq}}^\star = \text{diag}\left(\mathbf{1}^T A_{\text{eq}}^T\right)^{-1} A_{\text{eq}} V^\star - \mu^\star \tag{34c}$$
$$I_{\text{ineq}}^\star = \text{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right) \lambda^\star \tag{34d}$$
$$U_{\text{ineq}}^\star = \text{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right)^{-1} A_{\text{ineq}} V^\star - \lambda^\star. \tag{34e}$$

Note that the rhs of Eqs. (34) consists of quantities one can compute. Note that the matrices $\text{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right)$ and $\text{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right)$ are invertible and positive from the assumptions of Lemma 1. Eqs. (34) are combined with (33) to obtain

$$A_{\text{eq}}V^\star = \text{diag}\left(\mathbf{1}^T A_{\text{eq}}^T\right) U_{\text{eq}}^\star + I_{\text{eq}}^\star \tag{35a}$$
$$A_{\text{ineq}}V^\star = \text{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right) U_{\text{ineq}}^\star + I_{\text{ineq}}^\star \tag{35b}$$
$$A_{\text{eq}}^T U_{\text{eq}}^\star + A_{\text{ineq}}^T U_{\text{ineq}}^\star = \text{diag}\left(\mathbf{1}^T A\right) V^\star \tag{35c}$$
$$A_{\text{eq}}V^\star = b_{\text{eq}} \tag{35d}$$
$$A_{\text{ineq}}V^\star \leq b_{\text{ineq}} \tag{35e}$$
$$I_{\text{ineq}}^\star \geq 0 \tag{35f}$$
$$\left(A_{\text{ineq}}V^\star - b_{\text{ineq}}\right)_i I_{\text{ineq}_i}^\star = 0,\ i \in \mathcal{I}. \tag{35g}$$

In particular, substitution of (34b) into (34c) and of (34d) into (34e) yields Eqs. (35a) and (35b) respectively; substitution of (34a), (34b) and (34d) into (33a) yields (35c); substitution of (34d) into (33d) and into (33e) yields (35f) and (35g) respectively.

In conclusion, Eqs. (35) are Eqs. (31) evaluated at $V^\star$, $U^\star$, and $I^\star$ defined as above. Therefore, there exist $V^\star$, $U^\star$, and $I^\star$ that solve (27a)-(27f) when $c = 0$. □

Our next goal is to show that there exists a U_{cost} such that the circuit solution is also a solution to the LP (1). To show this we make use of the LP dual problem (Bertsimas and Tsitsiklis, 1997)

$$\max_\lambda \ b^T \lambda \tag{36a}$$
$$\text{s.t. } [A_{\text{eq}}^T\ A_{\text{ineq}}^T]\lambda = c \tag{36b}$$
$$\left[0\ I_{|\mathcal{I}|}\right] \lambda \geq 0, \tag{36c}$$

where $I_{|\mathcal{I}|}$ is an identity matrix of size equal to the number of inequality constraints. We create the following feasibility problem

$$\min_{\lambda, V} \ 0 \tag{37a}$$
$$\text{s.t. } A_{\text{eq}}V = b_{\text{eq}},\ A_{\text{ineq}}V \leq b_{\text{ineq}} \tag{37b}$$
$$[A_{\text{eq}}^T\ A_{\text{ineq}}^T]\lambda = c,\ \left[0\ I_{|\mathcal{I}|}\right] \lambda \geq 0 \tag{37c}$$
$$c^T V + b_-^T \lambda + b_+^T \lambda_- = 0,\ \lambda + \lambda_- = 0, \tag{37d}$$

where b_+ and b_- are the absolute values of the positive and the negative components of b respectively, and λ_- equals $-\lambda$. Note that in Eq. (37d) all coefficients are non-negative, and that (37d) is equivalent to $c^T V = b^T \lambda$. All feasible points of problem (37) are primal (1) and dual (36) optimal solutions (Bertsimas and Tsitsiklis, 1997).

Remark 3. *From the Assumption 3 and from the structure of* (37d)*, it follows that the matrix of equality and inequality constraints has non-negative coefficients and non-zero rows and columns.*

Problem (37) is solved by the circuit shown in Fig. 7. The circuit contains two parts: the primal circuit at the bottom and the dual circuit at the top. Primal and dual circuits have the form described in Fig. 5 and consist of equality and inequality sub circuits, corresponding to primal and dual constraints, respectively. Note that the cost

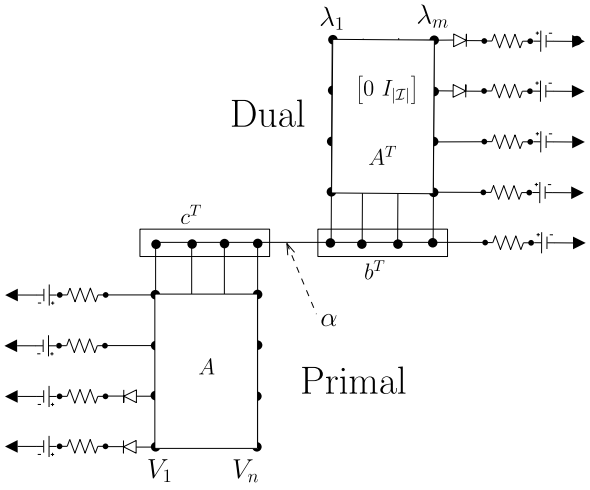

Figure 7: Circuit implementing the primal-dual feasibility problem (37). Primal and dual parts are connected via the zero duality gap constraint. For compactness, b_+ and b_- are represented as b and λ_- is part of λ.

circuit is not present in the primal and the dual circuits. Instead, the primal and dual circuits are connected by an equality sub circuit that corresponds to the zero duality gap constraint (37d).

Proposition 3. *Let Assumptions 1-3 hold. The circuit in Fig. 7 admits a solution. Moreover, at any circuit solution, the voltages V^* of the variable nodes are a solution to the original LP* (1)*.*

Proof. The circuit in Fig. 7 consists only of equality and inequality sub circuits. As shown in sections 3.1 and 3.2, the variable node voltages must satisfy the associated equality or inequality constraints and thus must satisfy Eqs. (37). The feasible set of problem (37) is the set of all primal optimal and dual optimal variables of problem (1). This feasible set is bounded by Assumptions 1-2 . This fact and the results from Remark 3 imply that all the assumptions of Lemma 1 are satisfied. We conclude that the circuit admits a solution. Moreover, every solution must be a solution of the original LP (1) because it satisfies simultaneously dual and primal problems with zero duality gap (Bertsimas and Tsitsiklis, 1997). □

Note that the circuit in Fig. 7 is not a practical way to implement an LP solver. In fact, the matrix A, and vectors c and b appear in two places and a small mismatch can lead to an infeasible problem. Moreover, the ability of easily modifying the LP rhs is lost (see Remark 1). In fact, the components of the rhs vector b also appear as resistors in the zero duality gap constraint.

In the circuit shown in Fig. 7, the dual and the primal circuits are connected with a single wire. We denote by U_{cost}^{crit} the voltage of this connection when the circuit settles.

Lemma 2 (Existence of U_{cost}^{crit})**.** *Let Assumptions 1-3 hold. Consider the circuit in Fig. 5 and its corresponding Eqs.* (27)*. A solution V^* to* (27) *with $U_{cost} = U_{cost}^{crit}$ is an optimizer of the LP* (1)*.*

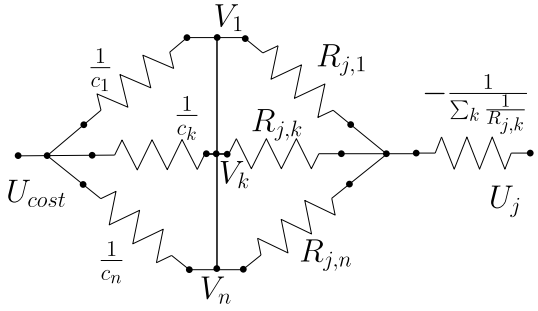

Figure 8: Subnetwork that connects the cost node and node j, when the remaining resistors are assumed to be zero.

Proof. If a voltage equals to $U_{\text{cost}}^{\text{crit}}$ is applied externally to the wire that connects the primal and the dual parts (at point α in Fig. 7), we can remove the dual circuit without affecting the primal one. Therefore, the circuit in Fig. 5 admits the same solution as the primal circuit in Fig. 7. □

To complete the proof of Theorem 1 we need to show that for any voltage $U_{\text{cost}} \leq U_{\text{cost}}^{crit}$, the circuit will continue to yield the optimal solution. Assume that U_{cost} is perturbed by ΔU_{cost} from the value U_{cost}^{crit}. We denote perturbed values of variable voltages V as ΔV and perturbed values of the cost current I_{cost} as ΔI_{cost}. Next, we examine the Thevenin equivalent resistance (Chen, 2004) as seen from the cost node. Refer to Fig. 8 showing a subnetwork connecting a cost node and an arbitrary node j. We want to compute a lower bound on the equivalent resistance as seen from the cost node. To this aim, we conservatively assume that all other positive resistors in the network are zero, i.e. $R_{k,l} = 0, \forall k, l$ s.t. $k \neq j$. In this scenario, all the variable nodes have the same potential that is equal to the potential U_j. This implies that the total resistance R_{total} which can be seen from the cost node is greater than or equal to all the cost resistances in parallel. Therefore we have:

$$R_{\text{total}} \geq \frac{1}{\sum_{i=1}^{n} c_i}. \tag{38}$$

From (27g), it follows that

$$c^T \Delta V = \left(\sum_{i=1}^{n} c_i \right) \Delta U_{\text{cost}} + \Delta I_{\text{cost}}. \tag{39}$$

Using the total equivalent resistance we know that

$$\Delta I_{\text{cost}} = -\frac{\Delta U_{\text{cost}}}{R_{\text{total}}}. \tag{40}$$

Combination of (39), (40) and (38) yields

$$\frac{c^T \Delta V}{\Delta U_{\text{cost}}} = \sum_{i=1}^{n} c_i - \frac{1}{R_{\text{total}}} \geq 0. \tag{41}$$

Eq. (41) states that the change in cost value must have the same sign as the change in ΔU_{cost}. Therefore, when U_{cost} is decreased the cost must decrease or stay the same. However, the cost cannot decrease, since it is already optimal. Therefore the cost must remain constant, and the circuit holds the solution to the problem (1) for any $U_{\text{cost}} \leq U_{\text{cost}}^{crit}$. This result completes the proof of Theorem 1.

Remark 4 (U_{cost}^{crit} computation)**.** *Consider the rhs vector b of constraints* (1)*. If b is contained in a polytope Θ, the value of U_{cost}^{crit} needs to be low enough to yield a correct solution for any $b \in \Theta$. A lower bound to $U_{cost}^{crit}(b)$ for any $b \in \Theta$ can be computed in many ways. A simple way is to solve for U_{cost} for all vertices of Θ and choose the minimum. This approach becomes intractable for large Θ and more efficient methods are the subject of ongoing research.*

5. Dynamic Analysis of the LP Circuit

In the previous section, we have shown that an equilibrium of the circuit in Fig. 5 is a solution to the LP problem (1). The next step is to analyze the stability of the equilibrium points under the presence of parasitic dynamic effects. This investigation is the subject of current ongoing research. Next we present two critical aspects which help understanding the dynamic properties of the proposed circuit.

5.1. Circuit passivity

We are interested in showing that the general circuit in Fig. 5 is passive. This important property has two interesting consequences. First, one can study convergence and stability properties of the proposed circuit by using existing results on passive (or dissipative) systems (Heemels et al., 1998) (this is a topic of ongoing research work). Second, one can observe an interesting link between convexity of the original problem and passivity of the resulting circuit. In fact, a non-convex QP circuit designed by using the approach presented in this paper would not be passive.

We examine an N-port resistor network which includes all positive and negative resistors of the original circuit shown in Fig. 5 and ignores the diodes and the constant voltage sources. The resulting network is shown in Fig. 9.

Proposition 4 (Network non-negativity)**.** *The resistance network in Fig. 9 is equivalent to a resistance network with non-negative resistors.*

Proof. Our goal is to obtain a lower bound of an equivalent resistance between any two ports. From Fig. 9 we see that a sub-network that connects two ports consists of two negative resistances — one for each port, and a mesh of positive resistors between them. We want to find an equivalent resistance that exists according to Thevenin's theorem (Chen, 2004). Let U_i and U_j be the two nodes in question. Next, motivated by a fact that replacement of any of the positive resistances with a zero resistance may only reduce the total equivalent resistance, we make a conservative assumption that all the resistors in this network, excluding resistors directly connected to negative resistors of the U_i and U_j nodes, are zero, thus $R_{k,l} = 0, \forall k, l$ s.t. $k \neq i, j$. In this case, all variable nodes have the same potential. This sub-network is illustrated in Fig. 10. The equivalent resistance of this network is zero since, according to (8), the negative resistance is constructed to be equal to the negative of the parallel combination of the other node resistances. Therefore, the equivalent resistance between any two ports is at least zero. □

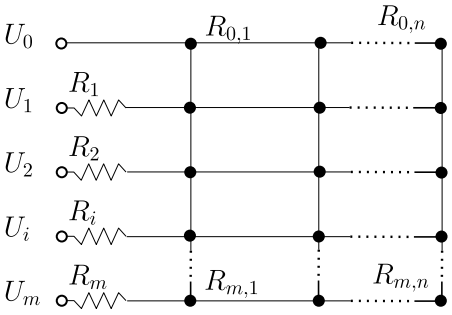

Figure 9: N-port resistor network with ports U_i. All $R_{i,j}$ are positive resistances, all R_k are negative resistances.

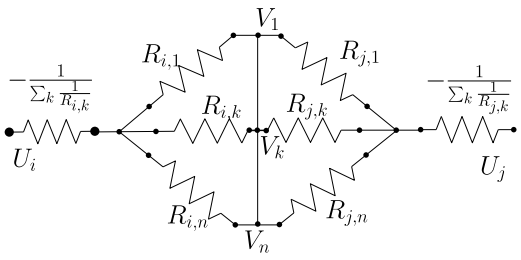

Figure 10: Subnetwork that connects nodes i and j, assuming that all other resistors are zero.

5.2. Parasitic Effects

The network in Fig. 11 is a modification of the LP circuit in Fig. 5 when the effect of parasitic wire capac-

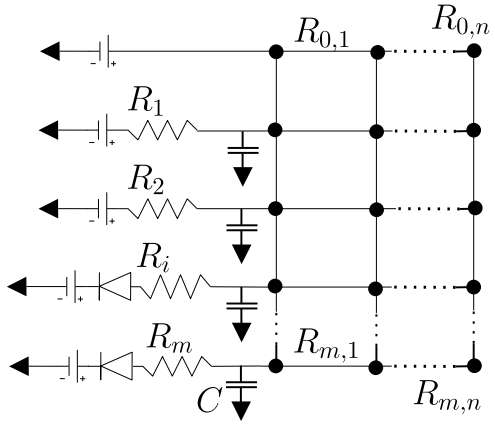

Figure 11: LP Analog Circuit with Parasitic Capacitance

itances are included in the model. The network has capacitors connected to all constraint nodes. The capacitors represent parasitic capacitance present in any real electric circuit. The circuit in Fig. 11 can be seen as a switched linear system where the diode states define the system mode. The negative resistances present in the circuit can lead to circuit instability (Heemels et al., 2002). In particular, if the negative resistor has an infinite bandwidth, this circuit can be shown to be unstable. In practice, the time constants of the negative resistors are limited and can be seen as tuning variables. One can use existing hybrid system theory and tools to design a piece-wise linear stabilizing controller where the unknowns are the time constants of the circuit implementing the negative resistances. In particular, since the approach of this paper is suitable for "small" optimization problems, computational methods for testing the stability of a hybrid system can be effective in this application. Useful approaches include the search for piecewise quadratic Lyapunov functions (DeCarlo et al., 2000; Pettersson and Lennartson, 1996, 1999), multiple Lyapunov functions (Branicky, 1998), or stabilizing controllers designed with the help of mixed integer optimization (Borrelli, 2003). Discovering simple heuristics for tuning the time constants of the negative resistors for the class of circuits presented in this paper is a topic of ongoing research.

6. Quadratic Programming Circuit

In this section we show how to use the results presented in the previous sections to solve Quadratic Programs (QPs). We consider the strictly convex QP

$$\begin{aligned} \min_V \ & \frac{1}{2}V^T Q V + d^T V \\ s.t. \ & \bar{A}_{\text{eq}} V = \bar{b}_{\text{eq}} \\ & \bar{A}_{\text{ineq}} V \leq \bar{b}_{\text{ineq}}, \end{aligned} \tag{42}$$

satisfying the following assumptions.

Assumption 4. *The QP (42) is feasible.*

Assumption 5. *The matrices $\bar{A}_{eq}, \bar{A}_{ineq}$ and d in the QP (42) are non-negative.*

Assumption 6. *The matrix Q in the QP (42) belongs to the set of all symmetric positive definite strictly diagonally dominant matrices with negative off-diagonal terms, i.e., $Q \in \mathcal{Q}^-$ where*

$$\begin{aligned} \mathcal{Q}^- \triangleq \{Q : & (Q = Q^T) \wedge (Q \succ 0) \wedge (Q_{ii} > \sum_{j,j\neq i} \|Q_{ij}\|) \\ & \wedge (Q_{ij} < 0 \text{ for } i \neq j)\}. \end{aligned} \tag{43}$$

Any strictly positive QP with a strictly diagonally dominant quadratic cost can be written in the form (42) satisfying Assumptions 5-6. However the transformation might not be unique.

The next theorem presents the main result of this section.

Theorem 2 (QP circuit equivalence)**.** *Consider the QP* (42) *and let Assumptions 4-6 hold. There exist A_{eq}, b_{eq}, A_{ineq}, b_{ineq} such that the steady-state voltages V^* of the circuit in Fig. 5 solving* (27) *with $c = 0$ are the optimizer of the QP* (42)*.*

Theorem 2 will be proven in three steps. In the first step, we consider the LP circuit of the previous section with a zero cost function. We recall Lemma 1 and show that it solves a QP with a positive semi-definite cost matrix $Q_A = \text{diag}(\mathbf{1}^T A) - A^T \text{diag}\left(\mathbf{1}^T A^T\right)^{-1} A$. In the second step, we rewrite the difference between $V^T Q_{\bar{A}} V$ and the cost in problem (42) as a sum of quadratic and linear terms. In the third step, we show how to construct A from $\bar{A}$ such that Q_A contains these additional quadratic and linear terms.

6.1. Proof of Theorem 2

In Lemma 1, it was shown that the solution to Eqs. (27) when $c = 0$ is equivalent to the solution of the QP

$$\begin{aligned} \min_V \ & \frac{1}{2}V^T Q_A V \\ s.t. \ & A_{\text{eq}} V = b_{\text{eq}} \\ & A_{\text{ineq}} V \leq b_{\text{ineq}}, \end{aligned} \tag{44}$$

$$Q_A = \text{diag}(\mathbf{1}^T A) - A^T \text{diag}\left(\mathbf{1}^T A^T\right)^{-1} A. \tag{45}$$

Next we prove that Q_A is positive semi-definite.

Lemma 3. *Let $A \in \mathbb{R}^{m\times n}$ and $c \in \mathbb{R}^n$ be non-negative, $\mathbf{1}^T A > 0$, and $\mathbf{1}^T A^T > 0$. Then the matrix*

$$Q_A = \text{diag}(c^T + \mathbf{1}^T A) - A^T \text{diag}\left(\mathbf{1}^T A^T\right)^{-1} A \tag{46}$$

is positive semi-definite.

Proof. From the definition of Q_A (46), the diagonal element in row j of Q_A is

$$\begin{aligned} Q_{A_{jj}} &= c_j + \sum_i A_{ij} - \sum_i \frac{A_{ij}A_{ij}}{\sum_k A_{ik}} \\ &= c_j + \sum_i A_{ij}\left(1 - \frac{A_{ij}}{\sum_k A_{ik}}\right). \end{aligned} \tag{47}$$

The diagonal element $Q_{A_{jj}}$ is non-negative, since A is non-negative and $\frac{A_{ij}}{\sum_k A_{ik}} \leq 1$. The row sum of all off-diagonal elements is

$$\sum_{l,l\neq j} Q_{A_{jl}} = \sum_{l,l\neq j}\sum_i \frac{A_{ij}A_{il}}{\sum_k A_{ik}}. \tag{48}$$

The difference between the j-th diagonal element and the sum of all the off-diagonal elements of row j is

$$\begin{aligned} & c_j + \sum_i A_{ij}\left(1 - \frac{A_{ij}}{\sum_k A_{ik}}\right) - \sum_{l,l\neq j}\sum_i \frac{A_{ij}A_{il}}{\sum_k A_{ik}} \\ & = c_j + \sum_i A_{ij}\left(1 - \frac{A_{ij}}{\sum_k A_{ik}} - \frac{\sum_{l,l\neq j} A_{il}}{\sum_k A_{ik}}\right) = c_j. \end{aligned} \tag{49}$$

If $c > 0$, the matrix Q_A is strictly diagonally dominant. If $c \geq 0$, the matrix Q_A is diagonally dominant. The matrix Q_A has non-negative main diagonal elements (47). Therefore, Q_A is positive definite when $c > 0$ or positive semi-definite for $c \geq 0$. □

Consider the QP (42). Since $Q \neq Q_{\bar{A}}$ and $d \neq 0$, the circuit in Fig. 5 with $A_{\text{eq}} = \bar{A}_{\text{eq}}$, $b_{\text{eq}} = \bar{b}_{\text{eq}}$, $A_{\text{ineq}} = \bar{A}_{\text{ineq}}$, $b_{\text{ineq}} = \bar{b}_{\text{ineq}}$ does not solve the QP (42). In the next step, we rewrite the QP cost matrices Q and d in a special form. The form will be used later in the third step to design the circuit which solves the QP.

Proposition 5. *Consider the cost $J = \frac{1}{2}V^T QV + d^T V$ of the QP (42) and let Assumptions 4-6 hold. Let $Q_{\bar{A}} = \text{diag}(c^T + \mathbf{1}^T\bar{A}) - \bar{A}^T \text{diag}\left(\mathbf{1}^T\bar{A}^T\right)^{-1}\bar{A}$. Then there exist scalars $\beta > 0$, $\alpha_{ij} > 0$ and r_i for $i, j = 1, \ldots, n$ such that*

$$\beta J = \frac{1}{2}V^T\left(Q_{\bar{A}} + \Delta Q\right)V + \beta d^T V, \tag{50}$$

where

$$\Delta Q \in \mathcal{Q}^-, \tag{51}$$

$$\Delta Q \triangleq \sum_{i,j=1,\ i\neq j}^{N} \alpha_{ij}\Delta Q^{ij} + \sum_{i=1}^{N}\alpha_{ii}\Delta Q^{ii}, \tag{52}$$

$$\beta d = -\sum_{i=1}^{N}\alpha_{ii}r_i\Delta d^i. \tag{53}$$

- *R1 the matrix ΔQ^{ij} with $i \neq j$ has all zero elements with the exception of two diagonal elements (i,i) and (j,j) equal to 1 and two off-diagonal elements (i,j) and (j,i) equal to -1,*
- *R2 the matrix ΔQ^{ii} has all zero elements with the exception of 1 at position (i,i),*
- *R3 the vector Δd^i has all zero elements with the exception of 1 at the i-th position.*

Proof. Consider the QP (42) and the matrices $Q_{\bar{A}} \succeq 0$ and $Q \in \mathcal{Q}^-$. Define $\Delta Q = \beta Q - Q_{\bar{A}}$. We prove (51) by finding a scalar β "large enough" such that $\Delta Q = \beta Q - Q_{\bar{A}}$ and $\Delta Q \in \mathcal{Q}^-$. Such a scalar exists since Q is strictly diagonally dominant by the Assumption 6. Note that the minimizer of $\beta J = \beta\left(\frac{1}{2}V^T QV + d^T V\right)$ is the same as of J.

It is immediate to see that ΔQ^{ij} and ΔQ^{ii} with properties $R1$ and $R2$ can generate any matrix in the set $\mathcal{Q}^-$. This proves (52), R1, R2 with $\alpha_{ij} > 0$. The i-th non-zero element of βd in Eq. (53) is equal to $-\alpha_{ii}r_i$, where $\alpha_{ii} > 0$. In order to satisfy (50) we set $r_i = -\beta d_i/\alpha_{ii}$. □

The third and last step consists in proving how to modify the original circuit so that ΔQ and βd^T as defined by Eq. (52) and (53) can be obtained.

Let the problem (1) be augmented with a redundant constraint

$$a^T V < \infty, \tag{54}$$

where $a^T \geq 0$ is a non-negative row vector. This constraint has no influence on the feasible set since it is redundant. Define

$$A' \triangleq \begin{bmatrix} \bar{A} \\ a^T \end{bmatrix}. \tag{55}$$

From (46), it follows that

$$Q_{A'} = Q_{\bar{A}} + \text{diag}(a) - \frac{aa^T}{1^T a}. \tag{56}$$

If a has only two non-zero entries a_i and a_j, then $Q_{A'}$ is the sum of the quadratic term $Q_{\bar{A}}$ arising from the original constraints $\bar{A}$ and the matrix $\alpha_{ij}\Delta Q^{ij}$. $\alpha_{ij}\Delta Q^{ij}$ has all zero elements with the exception of two diagonal elements (i,i) and (j,j) equal to $\frac{a_i a_j}{a_i+a_j}$ and two off-diagonal elements (i,j) and (j,i) equal to $-\frac{a_i a_j}{a_i+a_j}$. In conclusion, by adding a redundant constraint in the circuit with only two non-zero entries a_i and a_j, one can modify the elements (i,i), (i,j), (j,i) and (j,j) of the quadratic cost as

$$Q_{A'} = Q_{\bar{A}} + \alpha_{ij}\Delta Q^{ij},\ i \neq j \tag{57a}$$

$$\alpha_{ij} = \frac{a_i a_j}{a_i + a_j} \geq 0. \tag{57b}$$

where ΔQ^{ij} has the property R1 in Proposition 5. The redundant constraint is implemented by connecting each variable node V_i with resistor $1/a_i$ to a common node. Since the constraint is always inactive, the diode is always in non-conducting mode. Therefore, there is no need to include the diode and the negative resistance in the circuit.

We are left to show that we can modify the circuit to obtain terms of the type $\alpha_{ii}\Delta Q^{ii}$ in (52) and $\alpha_{ii}r_i\Delta d^i$ in (53). We augment the unknown vector V with an additional constant variable $V_{n+1} = r_i$

$$V' \triangleq [V, r_i], \tag{58}$$

and a redundant constraint

$$a^T V' < \infty, \tag{59}$$

where $a = [0, \ldots, 0, \alpha_{ii}, 0, \ldots, 0, \alpha_{ii}]$ is a $n+1$ dimensional vector of all zeros with the exception of α_{ii} at positions i and $n+1$. Then,

$$\begin{aligned}\frac{1}{2}V'^T Q_{A'}V' &= \frac{1}{2}V^T Q_{\bar{A}}V + \frac{1}{2}\alpha_{ii}(V_i - r_i)^2 \\ &= \frac{1}{2}V^T Q_{\bar{A}}V + \frac{1}{2}\alpha_{ii}V_i^2 - \alpha_{ii}r_i V_i + \frac{1}{2}r_i^2.\end{aligned} \tag{60}$$

In conclusion, by adding a redundant constraint of the type $\alpha_{ii}V_i + \alpha_{ii}r_i$, the cost $V'^T Q_{A'}V'$ becomes

$$\begin{aligned}&\frac{1}{2}V'^T Q_{A'}V' \\ &\quad= \frac{1}{2}V^T\left(Q_{\bar{A}} + \alpha_{ii}\Delta Q^{ii}\right)V - \alpha_{ii}r_i\Delta d^i V + \frac{1}{2}r_i^2,\end{aligned} \tag{61}$$

where Δd^i and ΔQ^{ii} have the properties R2-R3 in Proposition 5.

In conclusion, one one can add a number of redundant rows a^T to the original matrix of equality and inequality constraints $\bar{A}$ and add constant voltage sources r_i so that any ΔQ and βd^T defined by Eqs. (52) and (53) can be obtained. This completes the proof of Theorem 2.

Remark 5. *If the matrix Q in (42) is not diagonally dominant, the diagonal of matrix ΔQ might have negative values. This leads to negative resistors $R = {}^1/_{2\alpha_{ii}}$. Although this can be implemented, the negative resistance in the circuit may lead to a violation of the dissipative property of the network. This is a topic of current research.*

7. Simulations and Experiments

This section presents three examples where the approach proposed in this paper has been successfully applied. In the first example, a QP is solved by the proposed electrical circuit and simulated by the SPICE (Nagel and Pederson, 1973) simulator. In the second example, an analog LP is used to control a linear system by using Model Predictive Control. In the third example an experiment is conducted by realizing the circuit for a small LP with standard electronic components.

7.1. Quadratic Programming

We demonstrate the method and explore its limits by solving the problem QPCBLEND from the Maros and Meszaros QP problem set (Maros and Mészáros, 1999). The original problem has 83 variables, 43 equality constraints, and 114 inequality constraints. After translation to the all-positive form and the addition of constant variables (see Sections 3 and 6) the problem has 169 variables, 126 equality constraints, and 114 inequality constraints. The circuit that solves this problem was constructed with non-ideal components, including parasitic capacitance of $10fF$ that roughly corresponds to typical VLSI CMOS analog design and an operational amplifier with gain-bandwidth product (GBW) of 10GHz.

The convergence of the electric circuit is shown in Fig. 12. The circuit converges to a solution that is slightly different from the optimum because non-ideal elements are used. As can be seen in the figure, the steady-state error between the circuit cost and the optimal one $\mathtt{J}_{opt} - \mathtt{J}$ is in the order of 10^{-3}. Similarly the steady-state norm of the solution error $\|X_{opt} - X\|$ in in the order of 10^{-3}. There is a small constraint violation ($\|AX - b\|_2 = 9.3 \times 10^{-4}$) since the operational amplifiers have finite gain and require non-zero violation to generate voltage. As expected, if higher gain (HG) operational amplifiers are used (GBW of 100GHz), the infeasibility and the optimal cost error decrease.

The circuit transient can be partitioned into two phases. During the first $1000ns$ (or first $100ns$ for the high gain

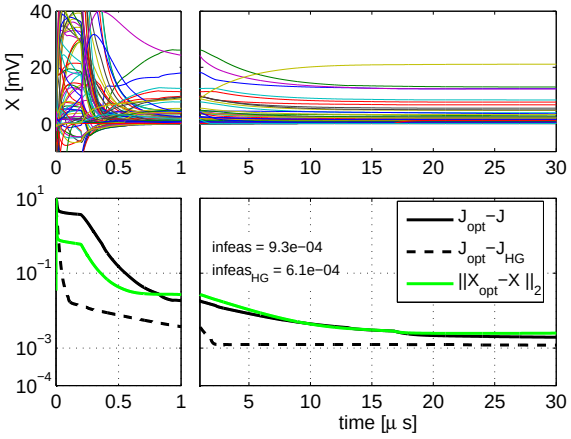

Figure 12: Solution of problem QPCBLEND. The upper plot shows the circuit voltages corresponding to the problem unknowns as a function of time. The lower plot shows the error between the circuit cost and the optimal one, and the norm of the solution error as a function of time. Two type of operational amplifiers are tested: nominal ones and the high-gain ones (denoted as $_{HG}$ circuit).

circuit), rapid convergence to a solution close to the optimal one can be observed. Afterwards, the circuit continues to improve the solution with a smaller change in the cost value. This behavior suggests that there are two main circuit modes - fast modes are associated to components which move in the direction of the cost gradient, slow modes are associated to voltages quasi-orthogonal to the cost gradient. The fast modes converge rapidly and provide a solution close to the optimum while the slow modes gradually improve the solution over a longer time period.

7.2. MPC example

This example demonstrates the implementation of a model predictive controller with an LP analog circuit. For this example, we work with the dynamical system $\frac{dx}{dt} = -x + u$, where x is the system state and u is the input. We want x to follow a given reference trajectory while satisfying input constraints. The finite time optimal control problem at time t is formulated as

$$\min_{u_0 \dots u_{n-1}} \sum_{i=1}^{N} |x(i) - x_{ref}(i)| \tag{62a}$$

$$x_{i+1} = x_i + (u_i - x_i)\delta,\ i = 0, \dots, N \tag{62b}$$

$$-1.5 \le u_i \le 1.5,\ i = 0, \dots, N \tag{62c}$$

$$x_0 = x(t), \tag{62d}$$

where N is the prediction horizon, $x_{ref}(i)$ is the reference trajectory at step i, δ is the sampling time, and $x(t)$ is the initial state at time t. Only the first input, u_0, is applied at each time step t.

With $N = 16$, the LP in (62) has 96 variables, 63 equality constraints, and 49 inequality constraints. An electric circuit that implements the system dynamics together with

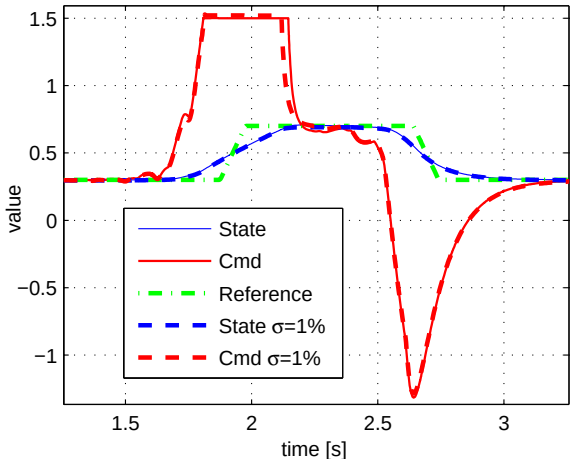

Figure 13: Example of MPC implementation. Solid lines represent the nominal controller and dashed lines represent the controller implemented with random 1% error of analog devices.

the circuit that implements the MPC controller were constructed and simulated using SPICE. The voltage value representing the system state was measured and enforced on the x_0 node of the LP. The optimal input value u_0 was injected as input to the simulated system dynamics. Note that in this setup there is no sample and hold. Rather, the two circuits continuously interact with each other. Fig. 13 shows the closed loop simulations results. Notice the predictive behavior of the closed loop control input and the satisfaction of the system constraints.

In order to demonstrate system performance for imperfect analog devices, another simulation result with 1% random Gaussian error in the values of the resistors is presented on the same Fig. 13. There is no significant change in system behavior.

7.3. Hardware implementation example

We implemented a small LP using standard electronics components. The same problem was realized by Hopfield (Tank and Hopfield, 1986) and Chua (Kennedy and Chua, 1988). The LP is defined as follows

$$\begin{aligned} &\min_{x_1,x_2} c^T[x_1\ x_2]^T \\ s.t.\ &\frac{5}{12}x_1 - x_2 \le \frac{35}{12}, \quad \tfrac{5}{2}x_1 + x_2 \le \tfrac{35}{2} \\ &-x_1 \le 5, \qquad x_2 \le 5 \end{aligned} \tag{63}$$

where c is a cost vector that is varied to get different solution points. The circuit was realized using resistors of 1% accuracy, operational amplifiers (OP27) for the negative resistance, and a comparator (LM311) with a switch (DG201) for implementing functionality of an ideal diode.

Various values for the cost function c and test results are summarized in Table 1. Table 1 shows that the experimental results are accurate up to 0.5%. The circuit

Table 1: Experimental and theoretical results (in parenthesis) for LP solution.

cost direction	x1 (exact)	x2 (exact)
1 1	4.996 (5.0)	4.99 (5.0)
-1 1	7.002 (7.0)	5.005 (5.0)
-1 -1	-7.012 (-7.0)	-4.98 (-5.0)
1 0	6.976 (7.0)	0.005 (0.0)

reaches an equilibrium 6 μs after the cost voltage was applied. The convergence time is governed by a slew rate of the OP27 that is limited to 2.8 $V/\mu s$.

8. Conclusion

We presented the design of an electric analog circuit able to solve feasible Linear and Quadratic Programs. The method is used to implement and solve MPC based on linear programming. We presented simulation and experimental results demonstrating the effectiveness of the proposed method.

The reported LP solution speed of 6 μs is faster than any result that was previously reported in the literature, and may be significantly decreased further by selecting faster components or implementing the design using faster technology, such as a custom VLSI design or FPAA device.

Future research directions have interesting challenges in both theory and implementation. The theoretical aspects include analog complexity theory and the study of the dynamic circuit behavior using the theory of Linear Complementary systems (Heemels et al., 1998). The implementation aspects include solutions to the optimal circuit design, implementation using VLSI technologies, and application to real-world problems.

9. Acknowledgments

The authors would like to sincerely thank the anonymous reviewers for their comments. Our gratitude also goes to Prof. Ilan Adler for valuable discussions that provided helpful inputs to this work, such as the primal-dual LP circuit; Dr. Yudong Ma and Anthony Kelman for their help in analysis of QP properties; Sarah Koehler for valuable discussions and help in preparation of the paper. Also, we gratefully acknowledge the financial support of Helen Betz Foundation for this research.

References

Anadigm, 2013. Anadigm, the dpasp company. http://www.anadigm.com/fpaa.asp.

Avni, O., Borrelli, F., Katzir, G., Rivlin, E., Rotstein, H., 2006. Scanning the environment with two independent cameras - biologically motivated approach. In: Intelligent Robots and Systems, 2006 IEEE/RSJ International Conference on. pp. 5297–5302.

Bageshwar, V., Borrelli, F., 2009. On a property of a class of offset-free model predictive controllers. Automatic Control, IEEE Transactions on 54 (3), 663–669.

Bazaraa, M. S., Sherali, H. D., Shetty, C. M., 2006. Nonlinear programming: theory and algorithms. Wiley-interscience.

Bemporad, A., Borrelli, F., Morari, M., 2002a. Model predictive control based on linear programming - the explicit solution. Automatic Control, IEEE Transactions on 47 (12), 1974–1985.

Bemporad, A., Borrelli, F., Morari, M., 2002b. Model predictive control based on linear programming˜ the explicit solution. IEEE Transactions on Automatic Control 47 (12), 1974–1985.

Bemporad, A., Borrelli, F., Morari, M., 2003. Min-max control of constrained uncertain discrete-time linear systems. Automatic Control, IEEE Transactions on 48 (9), 1600–1606.

Bertsimas, D., Tsitsiklis, J. N., 1997. Introduction to linear optimization. Athena Scientific Belmont, MA.

Borrelli, F., 2003. Constrained Optimal Control of Linear & Hybrid Systems. Vol. 290. Springer Verlag.

Borrelli, F., Baoti, M., Bemporad, A., Morari, M., 2005. Dynamic programming for constrained optimal control of discrete-time linear hybrid systems. Automatica 41 (10), 1709 – 1721.

Borrelli, F., Baoti, M., Pekar, J., Stewart, G., 2010. On the computation of linear model predictive control laws. Automatica 46 (6), 1035 – 1041.

Borrelli, F., Bemporad, A., Morari, M., 2003. Geometric algorithm for multiparametric linear programming. Journal of Optimization Theory and Applications 118 (3), 515–540.

Borrelli, F., Falcone, P., Pekar, J., Stewart, G., 2009. Reference governor for constrained piecewise affine systems. Journal of Process Control 19 (8), 1229 – 1237, ¡ce:title¿Special Section on Hybrid Systems: Modeling, Simulation and Optimization¡/ce:title¿.

Branicky, M., April 1998. Multiple Lyapunov functions and other analysis tools for switched and hybrid systems. IEEE Transactions on Automatic Control 43 (4), 475–482.

Chen, W., 2002. The Circuits and Filters Handbook, Second Edition. Circuits & Filters Handbook 3e. Taylor & Francis.

Chen, W., 2004. The Electrical Engineering Handbook. AP Series in Engineering Series. Elsevier Science.

Chua, L., Lin, G.-N., feb 1984. Nonlinear programming without computation. Circuits and Systems, IEEE Transactions on 31 (2), 182 – 188.

Chua, L. O., Lin, G. N., Lum, J. J., 1982. The (p+q)-port transformer. International Journal of Circuit Theory and Applications 10 (4), 335–359.

DeCarlo, R., Branicky, M., Pettersson, S., Lennartson, B., 2000. Perspectives and results on the stability and stabilizability of hybrid systems. Proceedings of the IEEE 88 (7), 1069–1082.

Dennis, J. B., 1959. Mathematical programming and electrical networks. Technology Press of the Massachusetts Institute of Technology [Cambridge].

Falcone, P., Borrelli, F., Asgari, J., Tseng, H., Hrovat, D., 2007. Predictive active steering control for autonomous vehicle systems. Control Systems Technology, IEEE Transactions on 15 (3), 566–580.

Garcia, C. E., Prett, D. M., Morari, M., 1989. Model predictive control: theory and practice - a survey. Automatica 25 (3), 335–348.

Grieder, P., Borrelli, F., Torrisi, F., Morari, M., 2004. Computation of the constrained infinite time linear quadratic regulator. Automatica 40 (4), 701 – 708.

Heemels, W., Schumacher, J., Weiland, S., dec 1998. Dissipative systems and complementarity conditions. In: Decision and Control, 1998. Proceedings of the 37th IEEE Conference on. Vol. 4. pp. 4127 –4132 vol.4.

Heemels, W. P. M. H., Camlibel, M., Schumacher, J., 2002. On the dynamic analysis of piecewise-linear networks. Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on 49 (3), 315–327.

Hestenes, M. R., 1966. Calculus of variations and optimal control theory. Applied Mathematics Series. John Wiley & Sons, New York, London, Sydney.

Jackson, A. S., 1960. Analog computation. McGraw-Hill.

Jerez, J., Ling, K. V., Constantinides, G., Kerrigan, E., 2012. Model predictive control for deeply pipelined field-programmable gate array implementation: algorithms and circuitry. Control Theory Applications, IET 6 (8), 1029–1041.

Jerez, J. L., Goulart, P., Richter, S., Constantinides, G., Kerrigan, E., Morari, M., Jul. 2013. Embedded Predictive Control on an FPGA using the Fast Gradient Method. In: European Control Conference.

Kennedy, M., Chua, L., may 1988. Neural networks for nonlinear programming. Circuits and Systems, IEEE Transactions on 35 (5), 554 –562.

Maeder, U., Borrelli, F., Morari, M., 2009. Linear offset-free model predictive control. Automatica 45 (10), 2214 – 2222.

Mariéthoz, S., Domahidi, A., Morari, M., Dec. 2012. High-Bandwidth Explicit Model Predictive Control of Electrical Drives. IEEE Trans. on Industry Applications 48 (6), 1980 – 1992.

Mariéthoz, S., Mäder, U., Morari, M., Nov. 2009. High-speed FPGA implementation of observers and explicit model predictive controllers. In: IEEE IECON, Industrial Electronics Conf. Porto, Portugal.

Maros, I., Mészáros, C., 1999. A repository of convex quadratic programming problems. Optimization Methods and Software 11 (1-4), 671–681.

Mayne, D. Q., Rawlings, J. B., Rao, C. V., Scokaert, P. O., 2000. Constrained model predictive control: Stability and optimality. Automatica 36 (6), 789–814.

Morari, M., Baotic, M., Borrelli, F., 2003. Hybrid systems modeling and control. European Journal of Control 9 (2-3), 177–189.

Nagel, L., Pederson, D., 1973. SPICE (Simulation Program with Integrated Circuit Emphasis). Memorandum No. ERL-M382.University of California, Berkeley.

Palusinski, O. A., Vrudhula, S., Znamirowski, L., Humbert, D., 2001. Process control for microreactors. In: Chemical Engineering Progress. Vol. 97. Bell & Howell Information and Learning Company.

Pettersson, S., Lennartson, B., 1996. Stability and robustness for hybrid systems. In: Proc. 35th IEEE Conf. on Decision and Control. Kobe, Japan, pp. 1202–1207.

Pettersson, S., Lennartson, B., Jul. 1999. Exponential stability of hybrid systems using piecewise quadratic lyapunov functions resulting in LMIs. In: Proc. IFAC World Congress. Beijing, China, pp. 103–108.

Quero, J. M., Camacho, E. F., Franquelo, L. G., 1993. Neural network for constrained predictive control. Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on 40 (9), 621–626.

Tank, D., Hopfield, J., may 1986. Simple 'neural' optimization networks: An a/d converter, signal decision circuit, and a linear programming circuit. Circuits and Systems, IEEE Transactions on 33 (5), 533 – 541.

Ye, Y., Todd, M. J., Mizuno, S., 1994. An o(n l)-iteration homogeneous and self-dual linear programming algorithm. Mathematics of Operations Research 19 (1), pp. 53–67.