Multiple Columns for High Throughput Complementary E-Beam Lithography (CEBL)

Enden D. Liu, Cong Tran, Ted Prescop, David K. Lam, Multibeam Corp, Santa Clara, CA

Abstract

Developers of e-beam lithography systems are pursuing diverse strategies to bolster throughput. To achieve parallelism, some e-beam efforts focus on building multiple-columns, and others focus on developing columns with multiple beamlets. In this paper, we discuss the benefits and throughput of a multiple column approach for a particular application: Complementary E-Beam Lithography (CEBL). CEBL is a novel approach where the e-beam lithography system is used only to pattern the smallest features. Everything else is patterned with existing optical lithography equipment. By working hand-in-hand with optical lithography, CEBL provides an urgently needed solution to create next-generation microchips. Moreover, CEBL is extendable for multiple technology generations. We show how a multiple column approach is the best way to meet the requirements for CEBL, including high throughput, high resolution and overlay accuracy, without excess complexity or cost.
Key Words: Electron Beam Lithography, Electron Beam Direct Write, Throughput, Multibeam.

1. Introductions

Electron beam lithography has been used for over 30 years. It provides high resolution and quick turn-around-time, for low volume wafer manufacturing, and photomask writing. Because electron beam lithographic tools write one feature at a time, its throughput is very slow when compared with optical scanners / steppers. In the last few years, multiple beam and other methods were proposed, and built to enhance the throughput of the electron lithographic tools.

Driven by the Moore's law and competitions among device makers, the feature size of each new technology node keeps on shrinking over the last 30 years. Now, the most advanced technology node requires feature sizes beyond the resolution limit of the 193 nm immersion scanners. New technologies (pitch doubling using spacer / etch back method; double masking) have been used to create feature smaller than the optical resolution limit. As the pitch doubling method becomes more mature, it extends the life to the optical scanners for more technology nodes to come. However, the pitch doubling method requires more masking steps, and / or more film deposition & etch back operations. The cost and turn-around-time of pitch doubling method become a concern.

A new method using both optical lithography and alternative lithography tools is proposed by Yan Borodovsky[1] of Intel in a Nikon LithoVision Workshop in 2010. This method is explained as follows. First, a restricted design rule is applied for feature sizes around 20 nm (40 nm pitch) or smaller. It requires 1-Dimensional layout for each of conducting levels (poly, metal-1, metal-2, for example). Using this 1D layout rule, the process window of linewidth control is maximized for 40 nm lines and spaces, at the resolution limit of the 193i scanners. After the 40 nm lines/spaces are printed, a pitch doubling method (spacer deposition and anisotropic etch back) is used to create 20 nm lines/spaces. To make real circuits out of the lines/spaces grating pattern, a "line-cut" masking step is required. This line-cut masking step can be done by using 4 photomasking operations, to avoid the resolution limit (80 nm pitch) of the 193i scanners. Alternatively, this line-cut patterning can also be done by using 1 EUV masking operation, or using Electron Beam Lithography without any mask. Borodovsky called it "complementary lithography". To further enhance the process capability and throughput, David Lam[2] of Multibeam Corp. proposed "Complementary Electron Beam Lithography" in BACUS conference in 2010, using multiple columns in a column array, to enhance the throughput of Complementary Electron Beam Lithography (CEBL).

Alternative Lithographic Technologies IV, edited by William M. Tong, Douglas J. Resnick, Proc. of SPIE
Vol. 8323, 83231Y · © 2012 SPIE · CCC code: 0277-786X/12/$18 · doi: 10.1117/12.916118

2. Complementary Electron Beam Lithography (CEBL) using Multiple Column Array Design

To improve the throughput of electron beam lithography, various multiple electron beam lithography have been proposed, (see Chapter 4 Electron Beam Lithography, written by T. Abe, et al, in a book, "Sub-Half-Micro Lithography for VLSI', edited by K. Suzuki[3], et al., Cambridge University Press, 2000, in Reference # 3). Liu[4] and his coauthors have published the column design and performance in a previous SPIE paper in 2011.

An electro-static column was designed & tested. Because the compact size and low power consumption, this column can be assembled into column array, such as an 88 column array on top of a 300 mm wafer. Each column has its own Schottky Thermal Field Emitter gun source, lenses, deflectors, and backscattered electron detector. This column design is particularly suited for the line-cut application in Complementary Electron Beam Lithography, in which there are only a few feature sizes & very low pattern density per design level. One can use a fixed shape (or Gaussian) beam to write the line-cut features (made of simple rectangles or squares only) in a vector scan mode, to get the optimized feature definitions, and decent wafer throughput (~ 5 wafers per hour).

3. Multiple Beam Writing Strategy

The writing strategy of this multiple column array is illustrated in Figure 1.

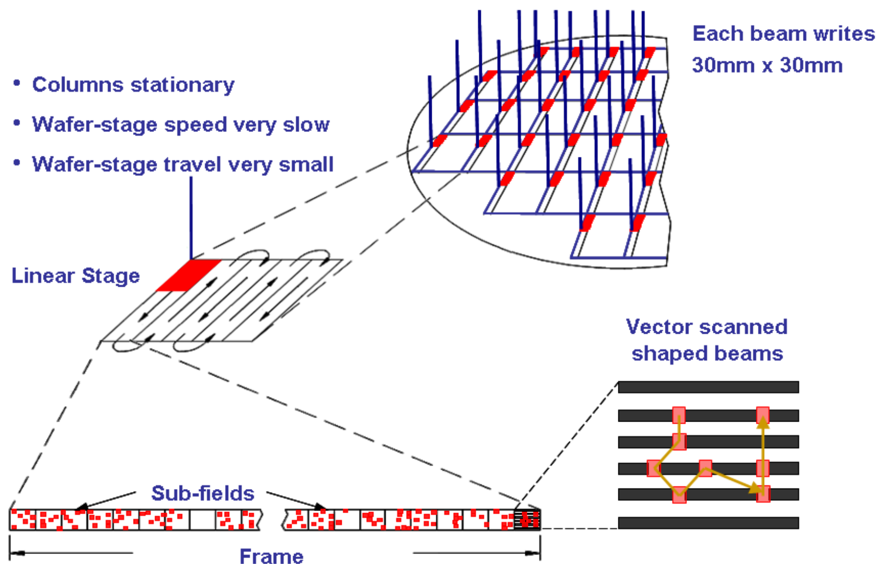

Figure 1. Multibeam's multi-column vector-scan e-beam lithography for CEBL, using multiple columns, individual & independently controlled, with 30x30 mm spacing, writing in stripes, main-fields, and vector scanning inside a subfield. The column array does not move, while the wafer stage moves in a serpentine way.

Electrostatic column design provides very compact column dimensions. It allows us to arrange 88 columns into an array with 33x26 or 30x30 mm grid spacing, on a 300 mm wafer. During writing, the column array is stationary, while the wafer is sitting on a moving stage. The wafer moves back and forth with a travel distance ~ 40 mm, which is a little longer than the column spacing. While the wafer is moving in a serpentine path with a constant speed of ~30 mm/second, each column controller sends signals to its own deflectors, blanker, to deflect and turn on/off the beam, in a "writing on the fly" manner. Because each column has its own controller and solid state memory hard drive, the writing pattern per column does not need to be identical. Each column writes 33x26 mm square area. This writing area is subdivided into many stripes, which is about 0.1 mm in width, and 33 mm in length. Within each 0.1x33 mm2 stripe, the main field deflector can deflect the beam position to +/-50 um, which we call it as a frame, with 2 um x 100 um in width and length. Each frame is made of 50

subfields, which are 2x2 um square in area. High precision and high speed sub-field deflectors are used to write line-cut or other features, in vector scan mode in each subfield area.

4. Vector Scan for Line-cut in CEBL Applications

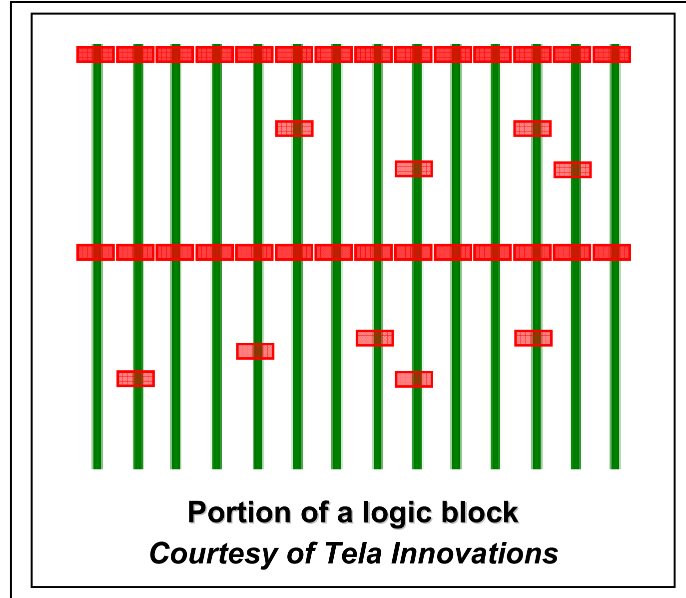

Figure 2. Example of line-cut features (in red) over metal-1 (green) 16 nm lines and spaces of a circuit block in an ASIC design, courtesy of Tela Innovations.

For low feature density applications, such as the line-cut design, the vector scan offers much better throughput than a raster scan method. For example, Figure 2 shows the line-cut layout (in red) over the metal-1 lines / spaces pattern (in green), in a typical ASIC design, courtesy of Tela Innovations. In this design, the feature density of line-cut level is ~ 3%, which makes the vector scan speed much faster than a raster mode. There are 37 line-cut features in this block. 28 of the 37 features are located along 2 lines, while 9 are isolated features. Each line-cut is a 16x32 nm feature, over 16 nm metal-1 lines / spaces. For each isolated feature, we need to blank, deflect and wait for the beam to settle down before writing. For the features along a long line, we need to blank, deflect and wait for settling in the first shot. For the rest of feature in this line, we can move the beam without blanking and settling.   In this way, the averaged blanking and settling time over these 37 line-cut features is reduced by a factor of 3X (~ (9+2)/37). Assuming a 10 ns exposure time and 20 ns blanking & settling time for isolated features, the average shot time becomes 10 + 20*(9+2)/37 = 16 ns / shot. If the other circuit designs are similar to that in Figure 2, in terms of density and ratio of line features versus isolated features, we can calculate the wafer throughput in the following equation, using the averaged shot time per feature as ~ 20 ns.

Throughput in time / wafer = (Number of shots / wafer) * (averaged shot time) + (overhead time) (1)
Averaged shot time = (Resist dose required) * (Feature area / shot) / (Beam current) + (blanking, etc.) (2)

The overhead time includes wafer transfer, wafer alignment, tool calibrations. It is expected to be ~ 120 seconds per wafer. From the above 2 equations, it becomes obvious that the resist dose level and beam current are the 2 key factors in determining the wafer throughput. The detailed factors are discussed in the following sessions.

5. High beam Current per column

In each Multibeam column, a Schottky Thermal Field Emission (TFE) gun source is used. The properties of TFE gun source has been discussed in details by Lyn W. Swanson and Gregory A. Schwind, in Chapter 2 of "Handbook of Charged Particle Optics', edited by Jon Orloff[5]. The gun tip radius of a typical TFE is ~ 0.5 microns, while its angular brightness is ~ 0.2 – 0.5 mA/(steradian solid angle), depending on the extractor voltage, and tip radius and operating temperature. In this paper, we select 0.25 mA/sr as a typical value of the TFE source brightness, at normal operation temperature of 1800 degree K. Given the definition and a typical value of the TFE brightness, the beam current can be expressed in the following equation.

Beam current per column = (TFE source angular brightness)*(3.1416*(half angle)^2) (3)

Table 1: Beam Current per TFE in each column

Half angle, degrees	0.1	0.15	0.2	0.25	0.3	0.35	0.4
Beam Current, nA	2.39	5.38	9.57	14.95	21.53	29.31	38.28

In Electron Beam Lithography applications, we select the aperture diameter in the range of 40 - 120 µm, (corresponding to 0.15 to 0.4 degrees in beam half angle), to achieve "beam resolution" suitable for the minimum feature size, while maintaining the maximum beam current available. Typically, we can get 25 nA per column. Because there are 88 columns per array, over a 300 mm wafer, we can deliver 2.2 mA beam current to expose the resist on a 300 mm wafer.

6. Wafer Writing Time:

In our column design, we use a fixed shape beam, in a constant current mode. It means that the current density per feature is inversely proportional to the feature area. It implies that shot time is much shorter for smaller feature. After we select a particular resist, the dose level is fixed by the resist properties. In a constant beam current mode, the writing time per wafer (excluding overhead, deflecting, & blanking time) becomes a constant, independent of feature sizes. This is because the writing time per feature is proportional the square of the shot size in one dimension, while the shot count is proportional to the inverse of the square of the shot size. Under this constant current mode, the total writing time alone, per wafer, is a function of electron beam current, resist sensitivity, writing area in the following equation:

Writing time = (Wafer area)*(feature density)*(resist dose required)/((beam current)*(# of columns)) (4)

Using equation 4, the writing time is summarized the following table.

Table 2: Writing time in minutes per wafer for 2.5, 5, 10, 20 & 40% feature density, at 4 different resist dose (20, 30, 50, 80 µC/cm2), using 88 columns with 25 nA / column.

	Resist Sensitivity, µC/cm2			
Writing time in minutes/wafer @ various feature density	20 µC/cm2	30 µC/cm2	50 µC/cm2	80 µC/cm2
2.5%	2.6	3.9	6.5	10.4
5%	5.2	7.8	13.0	20.9
10%	10.4	15.6	26.1	41.7
20%	20.9	31.3	52.1	83.4
40%	41.7	62.6	104.3	166.8

In CEBL line-cut applications, we expect the feature density in the range of 2.5% - 5% (see Figure 2 as an example, with 3% feature density). The 88 column array can complete the writing in less than 5.2 or 7.8 min per wafer using resist with 20 or 30 µC/cm2 sensitivity respectively with 5% feature density. When the resist sensitivity is 50 or 80 µC/cm2, the writing time becomes 13 and 21 minutes with 5% feature density. It is important to select the resist with good sensitivity and resolution, so that we can optimize the wafer throughput. Of course, we need to add overhead time, including blanking, deflecting, settling, wafer alignment, and wafer transfer to the writing time. If the overhead time is ~ 2 min / wafer, we can expect that wafer throughput should be ~ 10 minutes/wafer using 30 µC/cm2 as the dose level. This makes a throughput close to 5 wafers per hour.

However, the above discussion does not consider one important factor in Electron Beam Lithography: shot noise induced critical dimension control issue. This shot noise can be explained as the natural fluctuation of the incoming electron counts, which follows a Poisson distribution. This fluctuation can be treated as exposure level variation, which causes variations in CDU or LER. It becomes a critical factor when the number of electrons per feature is in the range of several hundreds or thousands of electrons. Typically, the shot noise can be estimated as square root of the number of electrons, in Poisson distribution. For example, if a feature is written with 400 electrons, its shot noise is +/- 20 electrons, which represents +/- 5% exposure level variations. As known by all lithographers, the exposure variation will lead to the variation of critical dimensions, depending on the slope of CD versus exposure curve. A rule of thumb in lithography is that we should control the exposure variations (shot noise alone) to be < 3.0%, which is similar to the specification of light level uniformity control in scanners. Table 3 provides a list of shot noise in % at various dose levels. Here, we assume that each feature of the line-cut is a square feature. The shot noise is defined in the following equation.

Shot noise = square root of (number of electrons per feature) / (number of electrons per feature) (5)
Number of electrons per feature = (dose in µC/cm2) * (feature size in nm)^2 / (1.602*10^(-19) Coulomb) (6)

Table 3 Shot noise level for various feature sizes using different resist sensitivities. Cells high-lighted in green represent that the shot noise is < 2%, the light yellow ones represent shot noise < 3%.

	Shot noise in % at various resist sensitivity in µC/cm2									
Line-cut size, nm	20	40	60	80	100	120	140	160	180	200
11	8.2%	5.8%	4.7%	4.1%	3.7%	3.3%	3.1%	2.9%	2.7%	2.6%
16	5.6%	4.0%	3.2%	2.8%	2.5%	2.3%	2.1%	2.0%	1.9%	1.8%
22	4.1%	2.9%	2.4%	2.0%	1.8%	1.7%	1.5%	1.4%	1.4%	1.3%
28	3.2%	2.3%	1.9%	1.6%	1.4%	1.3%	1.2%	1.1%	1.1%	1.0%
32	2.8%	2.0%	1.6%	1.4%	1.3%	1.1%	1.1%	1.0%	0.9%	0.9%
45	2.0%	1.4%	1.2%	1.0%	0.9%	0.8%	0.8%	0.7%	0.7%	0.6%

According to Table 3, we can use a resist with 40 µC/cm2 dose sensitivity for 28x28 nm square features or greater, while keeping the shot noise < 2.5%. When the feature size shrinks to 16x16 nm square, we need to use resist with 100 (or higher) µC/cm2 sensitivity to ensure that the shot noise is kept at 2.5% or less. The statements above on the shot noise issue agree with other publications, reported by Nicholas Rao[6], et al., and P. Kruit[7], et al..

7. CEBL Resist & Dose Selections

Many commercial resists are available for electron beam lithography. However, for < 20 nm resolution, only 3 commercial resists can do the job. They are PMMA, HSQ, and ZEP. PMMA and HSQ are well known for their high resolution

capability, but also as very slow resists (meaning high dose required), while ZEP provides 3-7 X faster in exposure speed, while being able to deliver resolution ~ 10 nm.

To fulfill the requirements of keeping shot noise < 3%, we have identified the electron beam resist for the use in CEBL applications. For positive resist, we can use PMMA and ZEP resists. For negative resist, we can use HSQ. All these 3 resist are known for their high resolution capability in 10 nm features, as pointed out by B. Cord[8] in his Ph.D. Thesis at MIT. There are several CAR resists available commercially, but their resolutions are not as good as PMMA, ZEP and HSQ resists, These 3 resists do not use “chemical amplifications”, so we don’t need to deal with the diffusion length of the radicals or active compounds. Here we use PMMA and ZEP as the preferred resist for CEBL applications.

Table 4. Resist selections for CEBL applications with different technology nodes.

Feature size, nm	Resist	Beam Energy, keV	Resist Dose, μC/cm2	# of electrons / feature	Shot Noise
11	PMMA	30	300	2266	2.1%
16	ZEP	25	100	1598	2.5%
20	ZEP	20	80	1998	2.2%
28	ZEP	15	60	2936	1.8%
32	ZEP	10	40	2557	2.0%
45	ZEP	5	20	2528	2.0%

Table 5 Writing time per shot and throughput of CEBL applications for 6 different generations of minimum feature sizes.

Minimum feature size, nm	Beam Energy, keV	Resist Dose, μC/cm2	Beam Current, nA / column	Exposure time / shot, ns	Throughput, wph
16	25	100	27	9.5	2.52
20	20	80	24	13.3	3.06
28	15	60	21	22.4	3.91
32	10	40	18	22.8	4.89
45	5	20	15	27.0	7.65

Using the resist dose recommended in Table 4, we can estimate the writing time per wafer for different design rules or technology nodes. We select PMMA for the 11x11 nm features, while we use ZEP resist for all other CEBL applications. The sensitivity and resolution of ZEP resist fit what need very well.

In Table 5, we use an 88 column array, and the column array can be operated at a beam energy, from 5 keV to 25 keV. Because the column design is based on all electrostatic lenses and deflectors, it can operate at different beam energy, after careful calibration work. In the throughput calculation in Table 5, we assume that the line-cut feature density is ~ 3%, 75%

of the line-cut features are designed as lines, blanking & settling time for isolated features is 20 ns, and the wafer overhead time for wafer transfer and alignment is 1.8 minutes/wafer.

For features or design rules of 16x16 nm line-cut, we can use ZEP resist, which is more sensitive than PMMA, with similar resolution capability, and also much better etching resistance in pattern transfer.

We also select the beam energy to lower level for relaxed feature sizes, to take the advantages of better resist sensitivity of the resist at lower beam energy level. The rule of thumb is to select resist and beam energy which provides adequate resolution, at the best resist sensitivity, if we can fulfill the shot noise requirement.

It is worthy of pointing out that the same ZEP requires a higher dose when the beam energy increases. This is because the higher beam energy electrons lose less energy (in percentages) in the resist when compared with lower beam energy electrons. In general, the resist sensitivity is linearly proportional to the beam energy in the working range from 5 keV to 30 keV beam energy.

8. Wafer throughput versus line-cut feature size in different technology nodes

If we consider ZEP resist only (ignore the 11 nm feature size, which uses PMMA), the plot of throughput versus feature size a fall in a straight line, implying that the throughput is linearly proportional to the feature size, as shown in Figure 3.

The key reason that Figure 3 shows a straight line relationship is because the exposure time per shot goes up when feature size increases. This can be explained as follows. First we use a column design for a fixed beam shape, not a variable shape. In this way, the column runs in a constant current mode, (fixed beam current level, once an aperture size is selected), not constant current density (current per unit area) mode as in variable shaped beam column design. As the result, the current density is inversely proportionally to the feature area (or resolution square). For a 16x16 nm square feature, its current density is 4X of that of a 32x32 nm square feature, at a constant beam current level. Hence, we can reduce shot time per feature, as the feature size decreases, even though the dose goes up for the smaller features. Second, because of shot noise consideration, we need to use higher dose (less sensitive resist) when the feature size decreases. Considering both of these 2 factors (constant current mode and shot noise requirement), the throughput follows a linear function, inversely proportional to the feature size. Interestingly, as the required dose goes up for smaller features, we can select higher beam energy to achieve both higher beam resolution and higher dose in the resist at the same time. Not only a higher beam energy level provides a better resolution, but also, it provides more beam current as lens becomes more powerful in focusing the source into the aperture in the column. In other words, we select a higher beam energy level, to print smaller features and to get more beam current per shot for line-cut designs in more advanced technology nodes. This trend helps us to improve the throughput when the feature size shrinks. This is shown in the "shot time versus feature size plot", as shown in Figure 4, where the shot time goes down as the feature size shrinks, despite of less sensitive resist used in more advanced technology nodes. As the results, we obtain a linear relationship of wafer throughput versus the feature size in different technology nodes.

In MB CEBL column design, we use a fixed shape, with a constant beam current, per feature. For line-cut or contact level, a fixed shape beam is good for most of the features in the layout. For CEBL applications, we can optimize column design specifically with a fixed aperture, to enhance the beam current available, and wafer throughput.

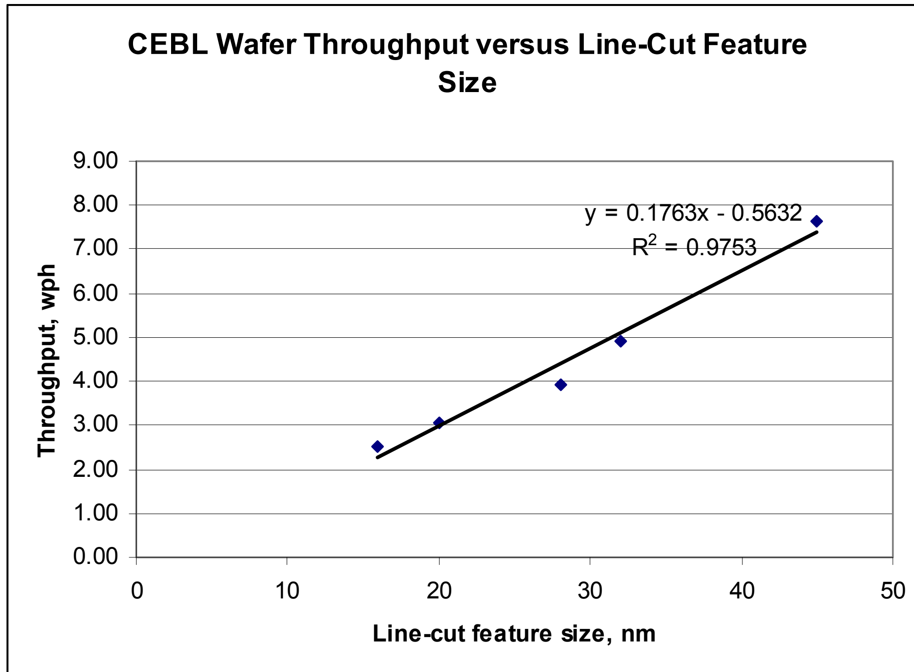

Figure 3: Multibeam CEBL wafer throughput at various line-cut feature sizes.

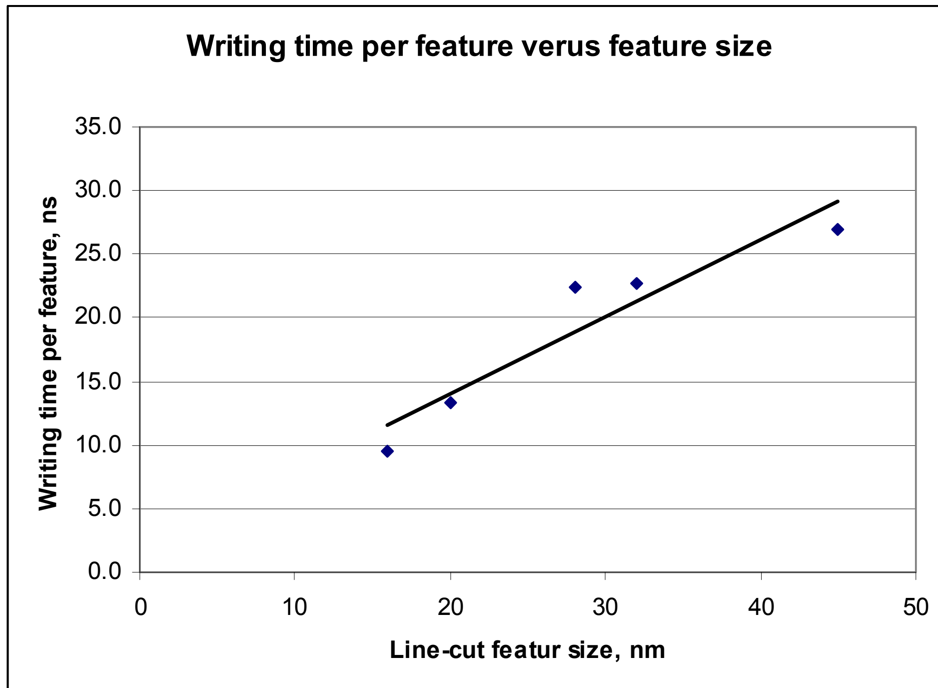

Figure 4. Writing time per feature versus feature size for different technology nodes

9. High Speed Data Transfer Strategy

To write each feature or shot, a column controller sends out 5-6 byte information for the deflectors and blanker circuits. Let's use an aggressive shot time, 15 ns per shot as the averaged writing speed per feature. Then, the data transfer rate in a single column, from controller to deflectors and blanker, is 6 Bytes in 15 ns, or 400 M Bytes / second.. This data transfer rate per column is well within the technology available today, using solid state memory drives & 64 bit microprocessors.

10. High Resolution Column

As Liu[4] reported in the SPIE conference in 2011, this electrostatic column can provide electron beam resolution from 11 nm to 35 nm in Full Width Half Maximum, depending on the selection of beam energy, aperture sizes or beam current levels, as shown in Figure 5.

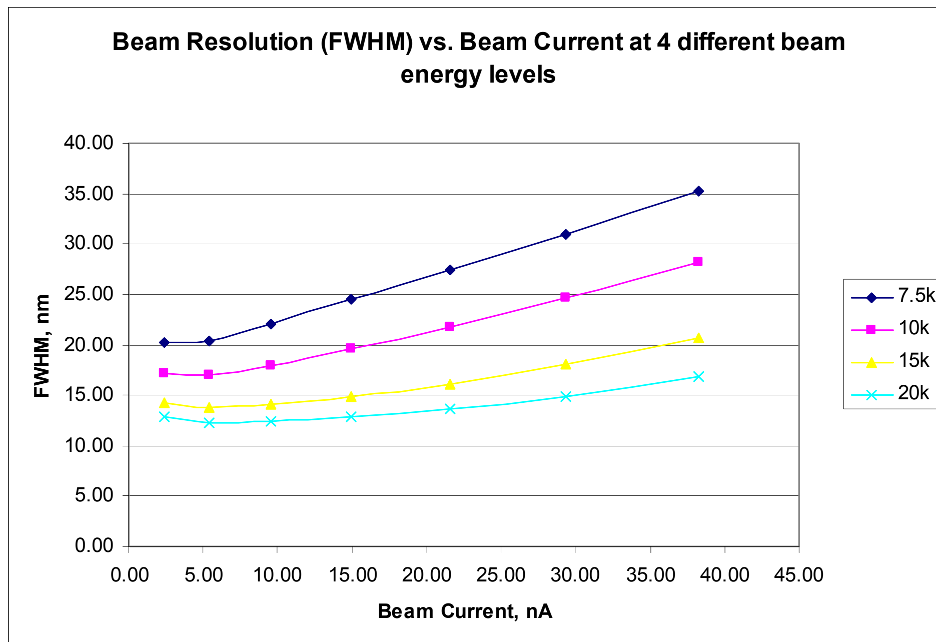

Figure 5 Simulated Beam Resolution (Full Width Half Maximum) versus Beam Current for 4 different beam energy levels.

11. Conclusions

We have shown that electrostatic columns can achieve high resolution (< 20 nm FWHM), with adjustable beam energy, from 5 to 50 keV. Using column array of compact electrostatic column design, we can reach good wafer throughput for CEBL applications. The beam energy can be selected for different generations of technology nodes, to optimize the requirement of high wafer throughput and high resolution. With ZEP resist, we can achieve ~ 5 wph for CEBL applications in various generations of technology nodes. For the most demanding technology nodes (16 nm line-cut features), we select 25 keV beam energy to meet the resolution requirement. For less demanding technology nodes, (such as 32 nm line-cut features), we select 10 keV beam energy, to take advantage of better resist sensitivity at lower

beam energy to enhance the CEBL wafer throughput. We select ZEP resist because it provides excellent resolution and dry etch resistance and is 3-7 times more sensitive than PMMA or HSQ resists.

The advantages of this column array design are listed here.

1) Each column is independently controlled by its own controller, for data transfer, deflection, and alignment. A data transfer rate of 400 MB/s is well within the capability of current technology.
2) The all electro-static column design provides high beam current per column, and also high resolution, because the column is not restricted to 5 keV. In fact, it is designed for a wide range of beam energy, from 5 to 50 keV, to achieve resolutions from 30 nm at 5 keV to 10 nm at 50 keV.
3) The wafer exposure is done in a distributed way by 88 columns spreading over the 300 mm wafer, such that the local heating and surface charge is less sever during writing, when compared with other designs which send all the electrons into a small area on the wafer.

REFERENCES:

[1] Y. Borodovsky, “ArF Lithography Extension for Critical Layer Patterning”, Nikon LithoVision 2010 Workshop, San Jose, CA., Feb 21010, http://www.nikonprecision.com/ereview/spring_2010/article05.html

[2] David K. Lam, Enden D. Liu and Ted Prescop, “Multibeam EBDW as Complementary Litho,” Photomask Technology, Proc. SPIE 7823, (2010).

[3] Katsumi Suzuki, et al., [Sub-Half-Micron Lithography for ULSIs], Cambridge University Press, Cambridge & New York, 107-192, 2000.

[4] Enden D. Liu, and Ted Prescop, “Optimization of E-beam Landing Energy for EBDW,” Alternative Lithography Technologies III, Proc. SPIE 7970, 79701S (2011).

[5] Orloff, Jon, [Handbook of Charged Particle Optics], CRC Press, Boca Raton & New York, 103-142 (1997).

[6] Nicholas Rau, et al., “Shot-noise & edge roughness effects in resist patterned at 10 nm exposure”, J. Vac. Sci. Technol. B 16, 3784 (1998).

[7] P. Kruit & S. Steenbrink, “Local critical dimension variation from short-noise related line edge roughness”, J. Vac. Sci. Technol. B 23(6), 3033, (2005)

[8] Bryan M. Cord “"Achieving sub-10-nm Resolution with Scanning Electron Beam Lithography", Ph. D. Thesis, MIT, (2009), http://dspace.mit.edu/handle/1721.1/53267