AIP | Journal of Applied Physics

# Influence of the surface morphology on the channel mobility of lateral implanted 4H-SiC(0001) metal-oxide-semiconductor field-effect transistors

Patrick Fiorenza, Filippo Giannazzo, Alessia Frazzetto, and Fabrizio Roccaforte

Citation: J. Appl. Phys. **112**, 084501 (2012); doi: 10.1063/1.4759354
View online: http://dx.doi.org/10.1063/1.4759354
View Table of Contents: http://jap.aip.org/resource/1/JAPIAU/v112/i8
Published by the American Institute of Physics.

# Influence of the surface morphology on the channel mobility of lateral implanted 4H-SiC(0001) metal-oxide-semiconductor field-effect transistors

Patrick Fiorenza,[1] Filippo Giannazzo,[1] Alessia Frazzetto,[2,3] and Fabrizio Roccaforte[1]
[1]*Consiglio Nazionale delle Ricerche, Istituto per la Microelettronica e Microsistemi (CNR-IMM), Strada VIII n. 5, Zona Industriale, 95121 Catania, Italy*
[2]*Scuola Superiore di Catania, Università degli Studi di Catania, Via Valdisavoia 9, 95123 Catania, Italy*
[3]*STMicroelectronics, Stadale Primosole 50, 95121 Catania, Italy*

(Received 15 June 2012; accepted 25 September 2012; published online 16 October 2012)

The influence of the surface morphology on the channel mobility of 4H-SiC metal-oxide-semiconductor field effect transistors annealed under two different conditions is discussed. The devices were fabricated using post-implantation annealing at 1650 °C. In particular, while the use of a protective capping layer during post-implantation annealing preserved a smooth 4H-SiC surface resulting in a channel mobility of 24 $cm^2\ V^{-1}\ s^{-1}$, a rougher morphology of the channel region (with the presence of surface macrosteps) was observed in the devices annealed without protection, which in turn exhibited a higher mobility (40 $cm^2\ V^{-1}\ s^{-1}$). An electrical analysis of $SiO_2$/SiC capacitors demonstrated a reduction of the interface state density from $7.2 \times 10^{11}$ to $3.6 \times 10^{11}\ cm^{-2}\ eV^{-1}$, which is consistent with the observed increase of the mobility. However, high resolution transmission electron microscopy showed an almost atomically perfect $SiO_2$/4H-SiC interface. The electrical results were discussed considering the peculiar surface morphology of the annealed 4H-SiC surfaces, i.e., attributing the overall reduction of the interface state density to the appearance of macrosteps exposing non-basal planes. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4759354]

## I. INTRODUCTION

Due to its excellent physical properties (such as a wide band gap, a high critical electric field, and high thermal conductivity), silicon carbide (SiC) is an outstanding material for high performances power electronic devices.[1,2] In the last decades, significant advancements have been achieved in the improvement of material quality (and increase of wafer size) and in device technology on this material. Indeed, several SiC based devices have been demonstrated, like Schottky diodes, junction barrier Schottky diodes (JBS), and metal-oxide-semiconductor field effect transistors (MOSFETs).[3] In spite of these progresses, these devices have not yet reached the expected optimal performances, also due to some scientific and technological open issues mainly related to surfaces and interfaces.[4]

The $SiO_2$/4H-SiC interface deserves a special attention, since it is the main building block of MOSFET devices and its electro-structural quality typically has a direct impact on the inversion channel mobility. In particular, electrically active defects at the $SiO_2$/SiC interfaces, such as carbon clusters, silicon suboxide bonds, or intrinsic defects in the near-interfacial oxide layers have been indicated as the origin of a high density of interface states in MOS and, hence, of the commonly observed low channel mobility in SiC MOSFETs.[5–7] Interface states in the bandgap localized close to the conduction band edge and fixed charges in the oxide can affect the MOSFET transconductance in two distinct ways. First, electron trapping by interface states causes a reduction in the density of free carriers in the inversion layer with respect to that induced by the gate bias. Furthermore, the mobility of inversion-layer electrons is lowered by Coulomb scattering both by the trapped and fixed charges.[8,9] To reduce the interface states density and alleviate the mobility problem, different post-oxidation-annealings (POA) of the gate oxide in NO or $N_2O$ have been explored[10,11] and can be efficient to provide adequate mobility values in the range of 30–50 $cm^2\ V^{-1}\ s^{-1}$.[12–16] Even higher values (up to 150 $cm^2\ V^{-1}\ s^{-1}$) were achieved employing annealings in alumina furnaces or in $POCl_3$, but the reliability of these gate oxides represents still a serious concern.[17,18]

An additional issue in vertical 4H-SiC MOSFETs is that the source and body regions are typically formed by a selective doping obtained by ion-implantation. These processes, in turn, require high-temperature annealing processes for electrical activation of the implanted-species (up to 1800 °C for p-type dopants),[19–22] which can degrade the surface region where the inversion channel is formed. While the surface morphology of SiC can be preserved during the post implantation annealing with a carbon capping layer,[20–25] the effects of these post-implantation thermal treatments on the channel mobility remain controversial. As an example, Haney *et al.*[26] observed that the channel mobility is not significantly affected by post-implantation annealing in the range 1200–1800 °C, using a carbon cap. However, lately Naik *et al.*[27] reported that the use of a carbon cap during device fabrication leads to a reduced channel mobility, due to an increased surface roughness induced by the cap. Even an anisotropy of the drain current was observed in some particular cases, where a pronounced "step bunching" was present in the sample surface.[28]

Recently, we have observed that Al-implanted lateral MOSFETs processed without a protection during post-implantation annealing show a higher channel mobility

 

($40\,cm^2\,V^{-1}\,s^{-1}$) with respect to devices fabricated using a protecting carbon capping layer ($24\ cm^2\ V^{-1}\ s^{-1}$).[29] Although Coulomb scattering was recently indicated as the dominant factor which limits the channel mobility in 4H-SiC,[29,30] the impact of the morphological surface conditions on MOSFETs performances remained unclear.

In order to clarify this left open issue, in this work, we present a further electrical and structural characterization of the $SiO_2$/SiC interface. The density of interface states, evaluated by capacitance-voltage measurements on MOS capacitors fabricated on the samples subjected to the two different post-implantation annealing conditions, was found to be higher in the sample protected by the cap-layer with respect to the uncapped one, consistently with the observed trend of channel mobility. However, an almost perfect interface at an atomic level was found in both cases by transmission electron microscopy.

The results were discussed considering the peculiar surface morphology of the annealed 4H-SiC surfaces, attributing the overall reduction of the interface state density to the appearance of macrosteps exposing non-basal planes.

## II. EXPERIMENTAL

In these experiments, we used nitrogen doped (n-type) 4H-SiC epitaxial layers with a doping concentration of $10^{16}\,cm^{-3}$, grown onto heavily doped $n^+$-type substrates with a 4°-off axis misorientation towards the ⟨11-20⟩ direction. Lateral n-channel MOSFETs were fabricated to determine the field effect channel mobility $\mu_{FE}$.[31] Al-implantation at different energies (in the range 40–450 keV) and fluences in the order of $10^{12}$ ions/$cm^2$ was used to create a body region with a doping concentration around $10^{17}\,cm^{-3}$. Source and drain were formed by heavy P-implantation n-type doping. Two different post-implantation annealing conditions were employed to obtain the electrical activation of the dopant, both performed at 1650 °C, *with* or *without* using a protective carbon capping layer on the sample surface. The capping layer was formed after implantation by a layer of photoresist baked at 800 °C and was removed after the high-temperature activation annealing, by a low temperature oxidation followed by a wet chemical cleaning in a HF-based solution.[25]

A 30 nm-thick $SiO_2$ layer, deposited by plasma enhanced chemical vapour deposition at around 400 °C, was used as gate dielectric. Prior to oxide deposition a standard clean followed by an etch in hydrofluoric solution carried out. After gate oxide deposition, a POA annealing at 1150 °C was performed in $N_2O$. Nickel silicide was used for Ohmic contacts The interface states density ($D_{it}$) has been estimated using the conductance method[32] on MOS capacitors fabricated on the same wafers.

The capacitance voltage (C-V) characteristics of the MOS capacitors and the current voltage (I-V) characteristics of the MOSFETs were measured in a Karl-Suss probe station using a Agilent B1500A parameter analyzer. The C-V measurements on the MOS capacitors were carried out at variable frequency in the range of 1kHz–1 MHz. The MOSFET characteristics were measured at different temperatures in the range of 298–423 K, using a Lakeshore 331 temperature controller connected to the chuck. The electrical measurements were performed in different points of the wafer. In this paper, we report representative results of the experimentally observed trend over the wafer.

The surface morphology of SiC channel region after the post-implantation annealing processes was studied by atomic force microscopy (AFM) using a Digital Instrument D3100 equipped with the Nanoscope V controller. The microstructure of the $SiO_2$/4H-SiC interface was monitored by transmission electron microscopy (TEM) using a JEOL 2010 F instrument.

## III. RESULTS AND DISCUSSION

First of all, the electrical characterization of the lateral MOSFETs was performed in order to assess the mobility behavior. Fig. 1(a) shows the transfer characteristics ($I_D$-$V_G$) of 4H-SiC lateral MOSFETs taken in the linear region at a drain voltage $V_{DS} = 200$ mV. The two lateral MOSFETs characterized were subjected to an annealing at 1650 °C to

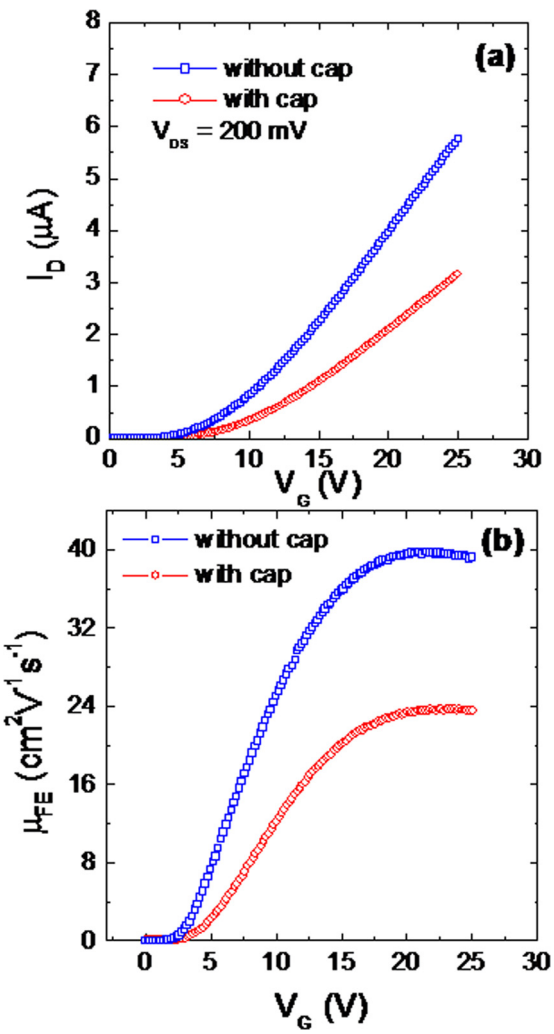


FIG. 1. (a) Drain current ($I_D$) as a function of gate bias ($V_G$) for lateral 4H-SiC MOSFETs processed either with or without using a capping layer during post-implantation high-temperature annealing: (b) Field effect mobility ($\mu_{FE}$) as a function of $V_G$ determined by the MOSFETs transfer characteristics for the two annealing conditions.

activate the p-type implanted body region, either with or without a protective carbon capping layer. As can be seen a higher current level is measured in the sample annealed without protection. From the transfer characteristics shown in Fig. 1(a), it was possible to determine the field effect mobility ($\mu_{FE}$), using the relation:[31]

$$\mu_{FE} = \frac{g_m L}{W C_{ox} V_{DS}}, \quad (1)$$

where $g_m$ is the transconductance $\frac{\partial I_{DS}}{\partial V_G}$ taken in the linear regions (at $V_{DS} = 200\,mV$), $L$ and $W$ are the channel length and width, respectively, and $C_{ox}$ is the gate capacitance per unit of area. The values of the mobility are plotted in Fig. 1(b). It must be pointed out that, in the field effect mobility determination from MOSFET transconductance measurements, the effect of the reduction of the inversion-layer charge density due to electron trapping by interface states is not directly taken into account. Therefore, the measured $\mu_{FE}$ values can be underestimated with respect the "real" inversion channel mobility. The most direct way to take into account this effect is performing channel mobility measurements on MOS-Hall bars, where mobility and carrier density are independently measured.[8,9] Although the value of the channel mobility is clearly dependent on the adopted measurement method, in our case, the direct comparison of the field effect mobility of the two differently prepared samples is a useful approach to get information on the dominant scattering mechanisms at the $SiO_2$/4H-SiC interface.

Evidently, as expected from the current behavior, the field effect mobility is higher for the device annealed without capping layer. In particular, the maximum values were $40\,cm^2\ V^{-1}s^{-1}$ and $24\ cm^2\ V^{-1}\ s^{-1}$, for the samples processed without and with capping layer, respectively.

It must be pointed out that after removal of the capping layer, the p-type implanted SiC surface where the inversion channel of the MOSFETs forms exhibited a roughness almost a factor of 5 lower with respect to the region annealed without protection. The same behavior was observed also in the non-implanted regions of the wafers, where the MOS capacitors were fabricated. Consequently, it can be concluded that this roughness is not the main limiting factor which inhibits the carrier transport (namely, the mobility) in the channel. As a matter of fact, this hypothesis is confirmed by the temperature dependence of the mobility $\mu_{FE}$, which is reported in Fig. 2 in the temperature range of 298–423 K. It can be noticed that in both cases the mobility increases with increasing temperature.

In order to consider the different scattering phenomena, the field effect mobility in 4H-SiC MOSFETs can be expressed considering a combination of several factors:[33,34]

$$\mu = \left(\frac{1}{\mu_B} + \frac{1}{\mu_{AC}} + \frac{1}{\mu_{SR}} + \frac{1}{\mu_C}\right)^{-1}, \quad (2)$$

namely, as a combination of the bulk mobility factor ($\mu_B$), the acoustic-phonon scattering ($\mu_{AC}$), the surface roughness scattering ($\mu_{SR}$), and the Coulomb scattering ($\mu_C$). It is worth noting that the use of the Matthiessen-like expression (Eq. (2)) to describe the mobility has the advantage that the various scattering mechanisms limiting the total carrier mobility are nearly separated. In this way, it is possible to easily include additional scattering mechanisms in the model without changing the formalism.[35] In this sense, the bulk electron mobility ($\mu_B$), often referred as low field mobility, is included as it is typically dominant at high temperatures and low fields, where carrier confinement effects become less important, and the electron mobility approaches the mobility in the bulk.[35]

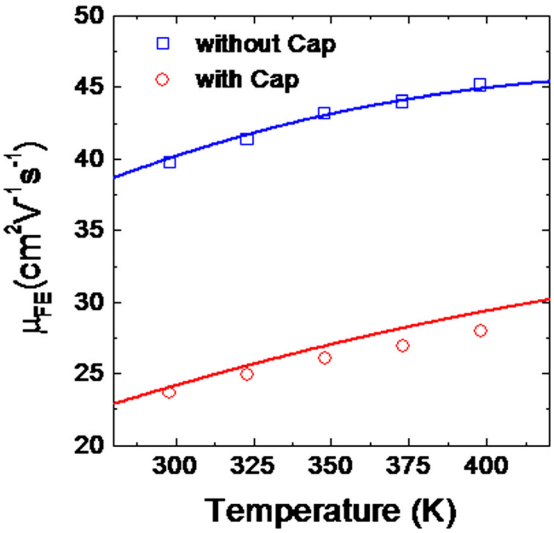


FIG. 2. Temperature dependence of the field effect mobility ($\mu_{FE}$) for the devices processed with or without a capping layer. The continue lines are the theoretical fit obtained with two different values of the trapped charge density.

Under these assumptions, an increasing mobility with temperature is an indication that the Coulomb term $\mu_C$ is the dominant one in Eq. (2). In fact, in this range the bulk mobility, phonon-scattering and interface roughness contributions decreases with temperature.[33–37] On the other hand, the Coulomb scattering term ($\mu_C$) in Eq. (2) is typically increasing with temperature and can be expressed as:[38]

$$\mu_C(T) = N T^{\alpha} \frac{Q_{inv}^{\beta}}{Q_{trap}}, \quad (3)$$

where $Q_{inv}$ is the inversion charge per unit area, $\beta$ is a empirical coefficient, $Q_{trap}$ is the trapped charge per unit area, $T$ is the absolute temperature, $\alpha$ is a temperature coefficient, and $N$ is a proportionality constant.[33]

According to the previous considerations, the temperature dependence of the mobility reported in Fig. 2 suggests that the Coulomb scattering generated by the presence of trapped charges at the $SiO_2$/SiC interface strongly limits the mobility of the carriers in the MOS channel.

Considering the complete expression of the mobility (Eq. (2)) and the material parameters reported in Refs. 33 and 34, the experimental data in Fig. 2 were fitted using the interfacial trapped charges ($Q_{trap}$) in the Coulomb term as a free parameter. The other parameters in Eq. (3) were taken from the literature, i.e., $\alpha = 1$,[35] $\beta = 1$,[9,39] and $N = 7.525 \times 10^{-3}\ cm^2\ V^{-1}\ s^{-1}\ K^{-\alpha}$.[33] Moreover, the surface roughness

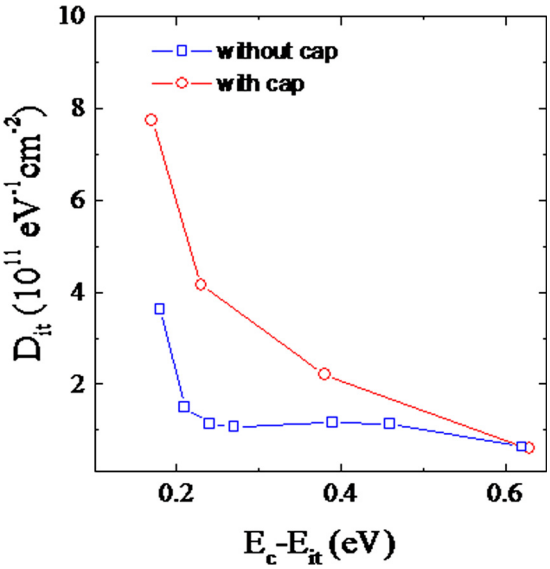


FIG. 3. Interface state density ($D_{it}$) measured on the 4H-SiC MOS fabricated on the same wafers

contribution $\mu_{SR}$ for the two samples was calculated taking into account the correlation length and the surface roughness,[36] as determined from the AFM data reported in Figs. 5(a) and 5(b).

Basing on these assumptions, a higher density of trapped charges $Q_{trap}$ at the interface ($5 \times 10^{11}/cm^2$) was required to fit the mobility behavior of the device processed with the capping layer with respect to the device processed without cap ($2.8 \times 10^{11}/cm^2$). The fitting curves are reported also in Fig. 2 together with the experimental data points.

Even if a better description of the mobility trend would require to consider also electron trapping effects in the fit, the validity of our approach has been confirmed by a direct measure of the density of the interface states ($D_{it}$), performed on n-type MOS capacitors fabricated on the same wafers using the conductance method. In fact, measuring the $D_{it}$ in n-type MOS capacitors is useful for understanding the mobility behaviour of n-channel MOSFETs, since electrons moving in the inversion layer are strongly affected by the interface states located near the conduction band edge.

Fig. 3 shows the energy distribution of the interface state density for both the MOS processed protecting the semiconductor surface with the capping layer and without the capping layer, respectively. In both cases, the density of the interface states decreases when moving inside the band gap. The maximum $D_{it}$ values are measured for both samples close to the conduction band edge and they are $3.6 \times 10^{11}\,cm^{-2}\,eV^{-1}$ and $7.2 \times 10^{11}\,cm^{-2}\,eV^{-1}$ for the sample treated without and with the capping layer, respectively. Clearly, a lower density of interface states in the sample annealed without cap explains the higher channel mobility. Indeed, it is also worth noting that the values of $D_{it}$ and the corresponding channel mobility found in our MOSFETs perfectly follow the experimental trend of the correlation curve $\mu_{FE}$ vs $D_{it}$ reported in Ref. 14. It is also interesting to observe that the integral over the band gap of the $D_{it}$ profiles gives values in the order of $10^{11}\,cm^{-2}$, in good agreement with the

TABLE I. Transition layer thickness at $SiO_2$/4H-SiC interfaces, and corresponding peak mobility and interface trapped charges values. The data are taken from Refs. 4 and 40.

| Transition layer thickness (nm) | Peak mobility ($cm^2\,V^{-1}\,s^{-1}$) | Interface trapped charges ($10^{11}\,cm^{-2}$) |
|---|---|---|
| 6 | 29 | 4.7 |
| 11 | 24 | 6.9 |
| 20 | 10 | 24.9 |

parameter used to fit the temperature behavior of the mobility.

In order to get a better understanding of the electrical results, a further morphological-structural analysis of the interface has been performed.

Recently, the inversion channel mobility at $SiO_2$/4H-SiC interfaces was correlated with the interface state density and the mobility degradation was associated with the

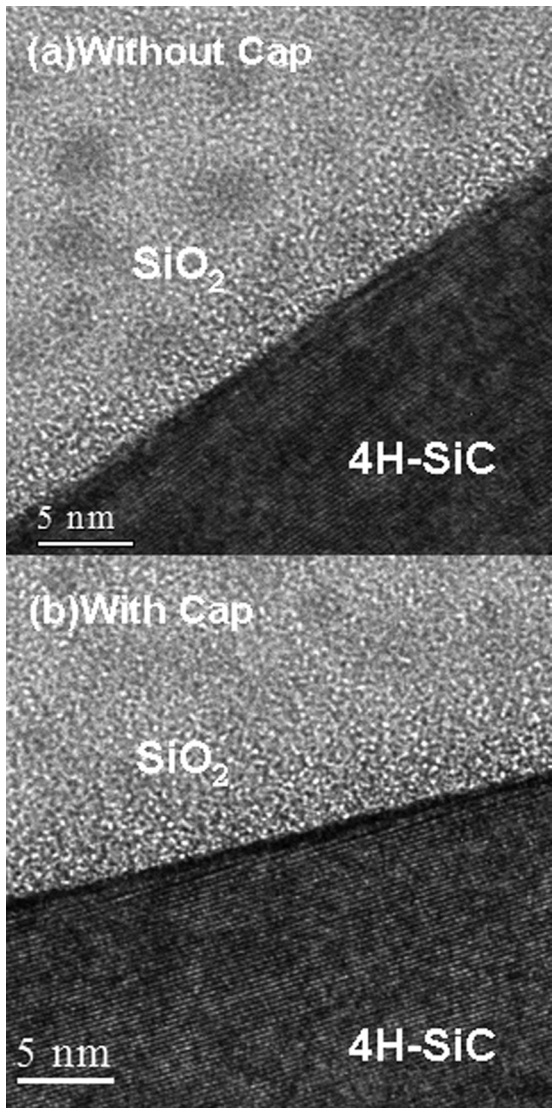


FIG. 4. High resolution transmission electron microscopy images of the gate region ($SiO_2$/4H-SiC interface) in the lateral MOSFET processed under the two different conditions. The images were taken along the [1-100] zone axis, which is perpendicular to the [0001] direction of 4H-SiC.

formation of an interfacial transition layer, characterized by an excess of carbon.[40] The main results of this investigations are summarized in Table I, which reports the values of the thickness of the transition region at $SiO_2$/4H-SiC interfaces as measured by TEM, and the corresponding values of channel mobility and interface trapped charges density[40] determined by devices characterization.

Hence, in our samples, a high resolution TEM analysis of the gate oxide/4H-SiC interface was carried out in order to verify the formation of such a transition layer. The micrographs are shown in Figs. 4(a) and 4(b), for the sample processed without and with the capping layer, respectively. As can be seen, in both cases, the images reveal an almost perfect structural quality of the interface region, since the atomic stacking of 4H-SiC is visible and no interfacial transition layer is visible. This result is in agreement with other literature works in which the formation of such interfacial disordered layer was not observed.[41–43]

Basing on this result, other factors, like a different efficiency of nitrogen passivation at $SiO_2$/4H-SiC interface during POA in the two samples, must be invoked to explain our results. As a matter of fact, recently Chang *et al.*[44] argued that even the composition and crystallographic orientation of the SiC surface layer can influence the amount of nitrogen incorporated during the nitridation process of a gate oxide. Furthermore, Saitoh *et al.*[45] recently evaluated the density of interface states in MOS capacitors fabricated on 4H-SiC surfaces with different cut angles, demonstrating a decrease of the $D_{it}$ values close to conduction band edge from $5 \times 10^{12}\,cm^{-2}\,eV^{-1}$ to $3 \times 10^{11}\,cm^{-2}\,eV^{-1}$ moving from vicinal (8°-off) surfaces to 90°-off surfaces, corresponding to the (11-20) face.

Basing on those experimental evidences, we can argue that in our case the peculiar surface morphology of the channel region which depends on the post-implantation annealing conditions can result into different values of $D_{it}$ and, ultimately, in a different channel mobility.

Fig. 5 shows the morphologies (acquired by AFM) of the 4H-SiC surfaces processed without (a) and with (b) the capping layer, and the corresponding cross sectional TEM micrographs of the $SiO_2$/4H-SiC interfaces ((c) and (d)), acquired at a lower magnification. The AFM single scanned lines taken on the surfaces of the two samples are shown in Fig. 5(e). From Figs. 5(a) and 5(b), the surface roughness (RMS) was 0.36 nm and 1.75 nm in the sample annealed with or without capping layer, respectively. The higher roughness in the sample treated without the capping layer originates from to the enhancement of the step bunching upon annealing. As can be seen in the TEM micrograph (Fig. 5(c)) and in the AFM line profile (Fig. 5(e) squares), the sample surface shows facets with typical height of about 5 nm, whose orientation is correlated to the original miscut direction of the wafers. In the present case, the substrates are cut along the (0001) basal plane with a 4° off-axis misorientation toward the ⟨11-20⟩ direction. Each of these steps exposes both the (0001) basal plane and the planes along the ⟨11-2n⟩ direction. On another hand, the sample treated with the capping layer presents a smoother surface (Figs. 5(b) and 5(d)) where no facets are observed. The line profile in Fig. 5(e), circles, shows the typical 4H-SiC steps with ~0.5 nm height.

From geometrical calculations based on the AFM morphology and cross section TEM images in Fig. 5, it was possible to estimate the percentage of the SiC surface area exposing the basal plane (0001) and the (11-2n) planes, both in the samples annealed with and without the protective cap. In the first case, more than 93% of the exposed surface was represented by the basal plane (0001). On the contrary, in the sample annealed without the carbon cap, more than 45% of the total area exposes the (11-2n) planes. Hence, according to the experimental evidences reported in Ref. 45, this peculiar morphology allows to justify the observed reduction in the $D_{it}$ at $SiO_2$/4H-SiC interface with step bunching. The proposed scenario is fully consistent with other recent findings on devices on macrostepped SiC surfaces.[46] In this sense, it cannot be ruled out that our experimental conditions might result into an anisotropy of the current conduction, as already observed in Ref. 28.

Finally, it must be also pointed out that a different efficiency of nitrogen incorporation on the (0001) and (11-2 n) facets during the POA process can be also invoked as a possible mechanism responsible of the different $D_{it}$ values in the two samples. As a matter of fact, it has been also reported that the amount of incorporated nitrogen can be well correlated with the trend of $D_{it}$ and $\mu_{FE}$ in 4H-SiC MOSFETs.[14]

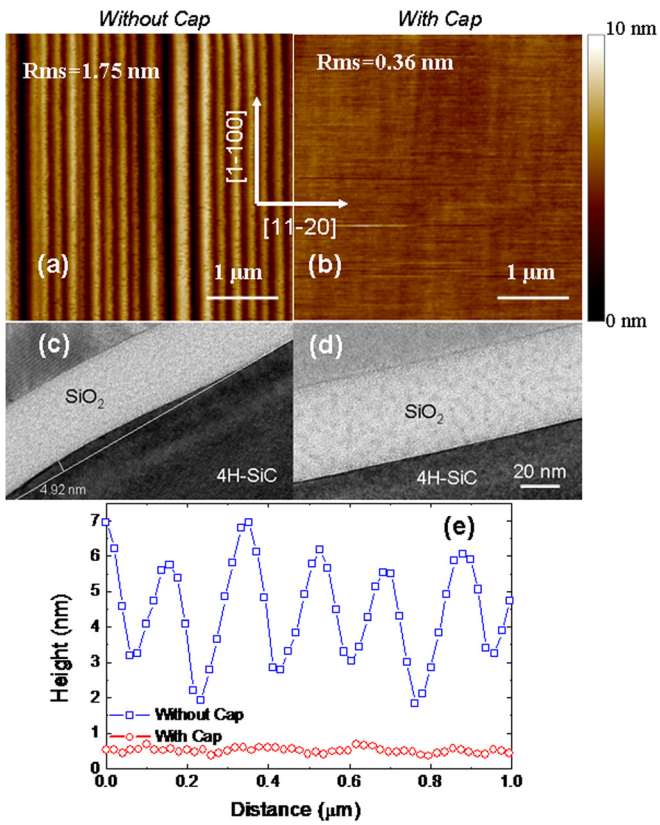


FIG. 5. AFM morphologies of the 4H-SiC surfaces treated without (a) and with (b) the capping layer, and corresponding cross sectional TEM micrographs of the $SiO_2$/4H-SiC interfaces ((c) and (d)). (e) AFM single scanned line taken on the surfaces of the two samples.

## IV. SUMMARY

In this paper, we correlated the morphological and structural properties of $SiO_2$/4H-SiC interfaces with the channel mobility in lateral implanted MOSFETs. In particular, irrespective of the interface roughness originating by post-implantation annealing, the channel mobility was found to increase with the temperature, thus being justified by the occurrence of Coulomb scattering phenomena and electron trapping at interface states. Lower values of $D_{it}$ were measured in the sample with a higher channel mobility. While a micro-structural analysis showed an almost perfect $SiO_2$/4H-SiC interface, without the formation of a interfacial transition layer, the different values of the interface states density can be explained by geometrical considerations on the peculiar morphology of the annealed 4H-SiC surfaces.

Clearly, under the practical point of view it is worth to remind that the oxide reliability can be severely affected by a poor surface morphology of the underlying SiC substrate. Hence, device makers must set the surface process in order to find the optimal compromise between the channel mobility and the oxide reliability.

## ACKNOWLEDGMENTS

The authors would like to thank C. Bongiorno for his support during TEM analyses. ST Microelectronics R&D in Catania is acknowledged for funding and invaluable assistance. The work was supported by the LAST POWER project. (ENIAC Joint Undertaking–Grant Agreement No. 120218).

[1]W. J. Choyke, H. Matsunami, and G. Pensl *Silicon Carbide: Recent Major Advances* (Springer-Verlag, Berlin, 2004).
[2]M. Shur, S. Rumyanstev, and M. Levinshtein, *SiC Materials and Devices* (World Scientific, Singapore, 2006), Vol. 1.
[3]B. J. Baliga, *Silicon Carbide Power Devices* (World Scientific Publishing Co. Pte. Ltd., 2005).
[4]F. Roccaforte, F. Giannazzo, and V. Raineri, J. Phys. D: Appl. Phys. **43**, 223001 (2010) and references therein.
[5]V. V. Afanasev, M. Bassler, G. Pensl, and M. Schulz, Phys. Status Solidi A **162**, 321 (1997).
[6]V. V. Afanas'ev, F. Ciobanu, S. Dimitrijev, G. Pensl, and A. Stesmans, J. Phys.: Condens. Matter **16**, S1839–S1856 (2004).
[7]F. Ciobanu, G. Pensl, V. V. Afanas'ev, and A. Schöner, Mater. Sci. Forum **483–485**, 693 (2005).
[8]N. S. Saks and A. K. Agarwal, Appl. Phys. Lett. **77**, 3281 (2000).
[9]E. Arnold and D. Alok, IEEE Trans. Electron Devices **48**, 1870 (2001).
[10]H. Li, S. Dimitrijev, H. B. Harrison, and D. Sweatman, Appl. Phys. Lett. **70**, 2028 (1997).
[11]G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, M. Di Ventra, S. T. Pantelides, L. C. Feldman, and R. A. Weller, Appl. Phys. Lett. **76**, 1713 (2000).
[12]G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, R. K. Chanana, R. A. Weller, S. T. Pantelides, L. C. Feldman, O. W. Holland, M. K. Das, and J. W. Palmour, IEEE Electron Device Lett. **22**, 176 (2001).
[13]C. Y. Lu, J. A. Cooper, T. Tsuji, G. Chung, J. R. Williams, K. McDonald, and L. C. Feldman, IEEE Electron Device Lett. **50**, 1582 (2003).
[14]J. Rozen, A. C. Ahyi, X. Zhu, J. R. Williams, and L. C. Feldman, IEEE Electron Device Lett. **58**, 3808 (2011).
[15]Y. Wang, T. Khan, M. K. Balasubramanian, H. Naik, W. Wang, and T. Paul Chow, IEEE Trans. Electron Devices **55**, 2046 (2008).
[16]S.-H. Ryu, S. Dhar, S. Haney, A. Agarwal, A. Lelis, B. Geil, and C. Scozzie, Mater. Sci. Forum **615–617**, 743 (2009).
[17]F. Allerstam, G. Gudjönsson, H. Ö. Ólafsson, E. Ö. Sveinbjörnsson, T. Rödle, and R. Jos, Semiconductor Sci. Technol. **22**, 307 (2007).
[18]D. Okamoto, H. Yano, K. Hirata, T. Hatayama, and T. Fuyuki, IEEE Electron Device Lett. **31**, 710 (2010).
[19]T. Troffer, M. Schadt, T. Frank, H. Itoh, G. Pensl, J. Heindl, H. P. Strunk, and M. Maier, Phys. Status Solidi A **162**, 277 (1997).
[20]Y. Negoro, K. Katsumoto, T. Kimoto, and H. Matsunami, J. Appl. Phys. **96**, 224 (2004).
[21]F. Giannazzo, F. Roccaforte, and V. Raineri, Appl. Phys. Lett. **91**, 202104 (2007).
[22]M. Rambach, A. J. Bauer, and H. Ryssel, Phys. Status Solidi B **245**, 1315 (2008).
[23]K. V. Vassilevski, N. G. Wright *et al.*, Semicond. Sci. Technol. **20**, 271 (2005).
[24]R. Nipoti, F. Mancarella, F. Moscatelli, R. Rizzoli, S. Zampolli, and M. Ferri, Electrochem. Solid-State Lett. **13**, H432 (2010).
[25]A. Frazzetto, F. Giannazzo, R. Lo Nigro, V. Raineri, and F. Roccaforte, J. Phys. D: Appl. Phys. **44**, 255302 (2011).
[26]S. Haney and A. Agarwal, J. Electron. Mater. **37**(5), 666 (2008).
[27]H. Naik, K. Tang, and T. P. Chow, Mater. Sci. Forum **615–617**, 773 (2009).
[28]K. K. Lee, T. Ohshima, A. Ohi, H. Itoh, and G. Pensl, Jpn. J. Appl. Phys., Part 1 **45**, 6830 (2006).
[29]A. Frazzetto, F. Giannazzo, P. Fiorenza, V. Raineri, and F. Roccaforte, Appl. Phys. Lett. **99**, 072117 (2011).
[30]H. Naik and T. P.Chow, Mater. Sci. Forum **679–680**, 595 (2011).
[31]D. K. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed. (John Wiley and Sons, Hoboken, New Jersey, 2006).
[32]E. H. Nicollian and J. R. Brews, *MOS Physics and Technology* (Wiley, New York, 1982).
[33]A. Pérez-Tomás, P. Brosselard, P. Godignon, J. Millán, N. Mestres, M. R. Jennings, J. A. Covington, and P. A. Mawby, J. Appl. Phys. **100**, 114508 (2006).
[34]A. Pérez-Tomàs, P. Godignon, N. Mestres, and J. Millàn, Microelectron. Eng. **83**, 440–445 (2006).
[35]C. Lombardi, S. Manzini, A. Saporto, M, Vanzi, IEEE Trans. Comput.-Aided Des. **7**, 1164 (1988).
[36]G. Mazzoni, A. L. Lacaita, L. M. Perron, and A. Pirovano, IEEE Trans. Electron Devices **46**, 1423 (1999).
[37]F. Roccaforte, F. La Via, V. Raineri, F. Mangano, and L. Calcagno, Appl. Phys. Lett. **83**, 4181 (2003).
[38]A. Pérez-Tomàs, M. R. Jennings, P. A. Mawby, J. A. Covington, P. Godignon, J. Millan, and N. Mestres, Mater. Sci. Forum **556–557**, 835 (2007).
[39]A. Hartstein, T. H. Ning, and A. B. Fowler, Surf. Sci. **58**, 178 (1982).
[40]T. Zheleva, A. Lelis, G. Duscher, F. Liu, I. Levin, and M. Das, Appl. Phys. Lett. **93**, 022108 (2008)
[41]E. Pippel, J. Woltersdorf, H. Ö. Ólafsson, and E. Ö. Sveinbjörnsson, J. Appl. Phys. **97**, 034302 (2005).
[42]H. Watanabe, T. Hosoi, T. Kirino, Y. Kagei, Y. Uenishi, A. Chanthaphan, A. Yoshigoe, Y. Teraoka, and T. Shimura, Appl. Phys. Lett. **99**, 021097 (2011).
[43]A. M. Beltran, S. Schamm-Chardon, V. Mortet, M. Lefebvre, E. Bedel-Pereira, F. Cristiano, C. Strenger, V. Häublein, and A. J. Bauer, Mat. Sci. Forum **711**, 134 (2012).
[44]K.-C. Chang, Y. Cao, L. M. Porter, J. Bentley, S. Dhar, L. C. Feldman, and J. R. Williams, J. Appl. Phys. **97**, 104920 (2005).
[45]H. Saitoh, A. Seki, A. Manabe, and T. Kimoto, Mater. Sci. Forum **556–557**, 659 (2007).
[46]T. Masuda, S. Harada, T. Tsuno, Y. Namikawa, and T. Kimoto, Mater. Sci. Forum **600–603**, 695 (2009).