Real-Time Demonstration of Low-Complexity Time-Domain Chromatic Dispersion Equalization

Celestino S. Martins[*], **Sofia B. Amado**[*], **Ricardo M. Ferreira**[*], **Ali Shahpari**[*], **António L. Teixeira**[*], **Fernando P. Guiomar**[†], **Armando N. Pinto**[*]

[*]*Department of Electronics, Telecommunications and Informatics, University of Aveiro and Instituto de Telecomunicações, Campus Universitário de Santiago, 3810-193, Aveiro, Portugal*
e-mail: csmartins@av.it.pt

[†]*Dipartimento di Elettronica e Telecomunicazioni, Politecnico di Torino, Corso Duca degli Abruzzi, 24,10129 Torino, Italy*
e-mail: fernando.guiomar@polito.it

ABSTRACT

We demonstrate real-time CD equalization (CDE) for coherent optical transmission systems using a low complexity time-domain (TD) multiplierless finite-impulse response (FIR)-based equalizer, based on a field-programmable gate array (FPGA) implementation. The real-time operation is performed for a single-channel 2.5 Gb/s QPSK optical signal with a performance penalty of only ∼0.15 dB with respect to the maximum performance. The hardware complexity is also evaluated in terms of occupation in a Virtex-6 FPGA-XC6VLX240T, revealing the high efficiency of the proposed CDE algorithm.

Keywords: optical communications, coherent detection, digital signal processing, real-time, hardware implementation, field-programmable gate array.

1. INTRODUCTION

The increasing capacity demand in optical networks together with advanced digital signal processing (DSP) have instigated the deployment of coherent transceivers in long-haul optical transmission systems. Linear distortions such as chromatic dispersion (CD) and polarization-dependent effects can be compensated entirely in the digital domain, highly impacting the reduction of complexity associated with coherent optical transmission systems [1]. Taking into account the requirements of power consumption and chip area, the implementation of DSP techniques for equalization of CD becomes one of the major challenges for transceivers based either on application-specific integrated circuitries (ASICs) or field-programmable gate arrays (FPGAs) [2].

The CD equalization (CDE) in digital coherent optical systems has been most commonly implemented by frequency-domain (FD) equalizers, due to their low complexity relatively to time-domain (TD) finite impulse response (FIR)-based equalizers for uncompensated long-haul fiber links, where the required equalizer order is high due to the large amount of accumulated dispersion [3]. Nevertheless, TD FIR-based equalizer is attractive for its ease of implementation, since it avoids the use of block processing from fast-fourier transform (FFT) and inverse fast-fourier transform (IFFT), thus facilitating real-time applications. Several research works have been performed to reduce the complexity of TD FIR-based equalizer [4–6]. In our previous work [4], we have proposed a reduced complexity distributive FIR-CDE (D-FIR-CDE) algorithm, which revealed significant complexity and latency gains in comparison with FD and standard TD FIR-based equalizers. In [6] we have performed the experimental validation of the D-FIR-CDE technique in dual-carrier 400G PM-16QAM transmission systems. In addition, we have proposed a multiplierless D-FIR-CDE (MD-FIR-CDE) version as an efficient hardware implementation of D-FIR-CDE [4].

In this paper, we provide real-time demonstration in a FPGA platform of CD compensation using the MD-FIR-CDE algorithm for a single-channel QPSK optical signal. The real-time MD-FIR-CDE performance is compared with the maximum performance obtained with the standard FIR-CDE and a Q^2-factor penalty of only ∼0.15 dB is achieved. Furthermore, we demonstrate the high hardware efficiency of MD-FIR-CDE.

2. Experimental Setup

Following our previous work [4, 6], where the experimental demonstration with offline data was presented, in this work we provide a real-time validation of the MD-FIR-CDE using commercially available analog-to-digital converters (ADCs) (4DSP FMC125) and an FPGA platform (Xilinx Virtex-6 FPGA). Due to the hardware limitations in terms of electrical bandwidth and sampling/processing rate, the real-time experiment is carried out for a single-channel 2.5 Gb/s QPSK optical signal. Due to the relatively low bit-rate, the impact of chromatic dispersion is emulated

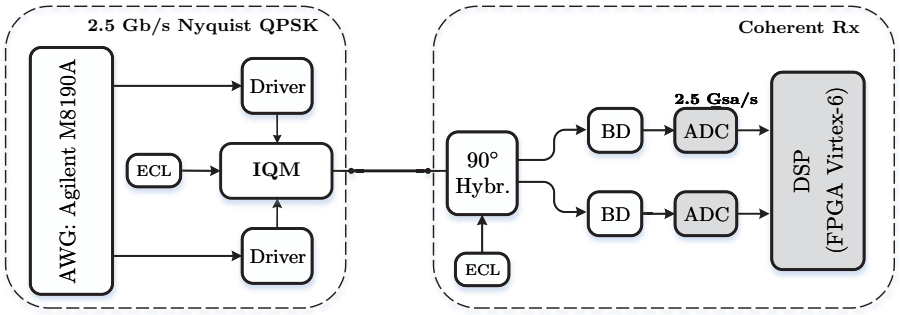

Figure 1: Experimental setup for real-time validation of the MD-FIR-CDE. The transmitted signal is a Nyquist-shaped 2.5 Gb/s QPSK optical channel.

by the transmission of a pre-distorted signal, considering a total accumulated dispersion of 1.6 μs/nm. The pre-distorted signal is engineered in MATLAB and then electrically generated by an Arbitrary Waveform Generator (AWG). Despite of the reported hardware limitations, we emphasize that this does not affect the main purpose of the real-time experiment, which aims at proving the implementation feasibility and computational efficiency of the MD-FIR-CDE algorithm.

The real-time laboratorial setup is depicted in Fig. 1. At the transmitter-side, the optical carrier is generated by an external cavity laser (ECL) (100 kHz linewidth) centered at 1549.32 nm and then modulated by an IQ modulator (IQM), which is electrically driven by a 12 Gsa/s AWG (Agilent M8190A), mapping the digitally pre-distorted 2.5 Gb/s Nyquist (0.1 roll-off factor) QPSK signal onto the optical carrier. The transmitted bits are generated by a pseudo random bit sequence (PRBS) of $2^{15}-1$. At the receiver-side, the QPSK signal is coherently detected using a $4\times90^{\circ}$ optical hybrid. A pair of balanced detectors (BD) is used to convert the received optical signal into an electrical signal. The electrical signal is converted to the digital domain using two 8-bit 1.25 Gsa/s ADCs (4DSP FMC125, 500 mV peak-to-peak) with an analog bandwidth of $\sim$2 GHz, operating in interleaving mode. The digitized I/Q signals are then sent to a Virtex-6 FPGA (ML605 evaluation board) where the real-time chromatic dispersion equalization is performed using the MD-FIR-CDE algorithm. The FPGA operating frequency is set to 156.25 MHz, which leads to a parallelization level of 16 in order to enable a real-time processing at 2.5 GSa/s. The signal is stored in the first-in first-out (FIFO) memory units with a length of 2^{15} samples and the BER is estimated taking into account the transmitted PRBS, considering 12 independent windows with 2^{15} bits. Since the required complexity for hardware implementation of the standard FIR-CDE exceeds the available resources of the Virtex-6 FPGA, the equalization of CD using the FIR-CDE architecture is performed in MATLAB. Thus, for this scenario, the FPGA is configured to collect the ADCs outputs in dedicated FIFO units, storing the received 2.5 Gb/s QPSK signal for offline post-processing in MATLAB. The real-time MD-FIR-CDE performance is then directly compared to the maximum performance obtained with the standard FIR-CDE algorithm, applied offline in MATLAB after coherent detection and digitization with the same hardware.

3.Experimental Results

Fig. 2 presents the obtained results in terms of BER versus received optical power, which is adjusted with a variable optical attenuator at the receiver end. This allows to assess the CDE performance for different signal-to-noise ratios. Both CDE algorithms are applied with $N = 83$ taps, which was found to be the minimum required for penalty-free equalization. As described in [4], the D-FIR-CDE resorts to the quantization of FIR coefficients in order achieve a reduced implementation complexity. The MD-FIR-CDE operates with 4 levels of quantization ($\Delta = 4$), following the offline results obtained in [4]. The penalty due to coefficient quantization is revealed by the gap between the two curves. Note that this performance gap tends to vanish for BER regions closer to the defined FEC limit of 1×10^{-3}. For the specific case of -42 dBm of received optical power, the penalty induced by the MD-FIR-CDE is reduced to $\sim$0.15 dB in Q^2-factor, which is in good agreement with the offline results analyzed in our previous work with offline processing [4].

In order to assess the hardware complexity of MD-FIR-CDE, we have analyzed the hardware Mapping Report generated by the Xilinx integrated synthesis environment (ISE) software tool after compiling the project. For simplicity, we quantify the complexity in terms of number of occupied slices, look up tables (LUTs), number of registers and DSP48E1s. Note that a slice can be considered as the basic element of FPGA resource usage, since

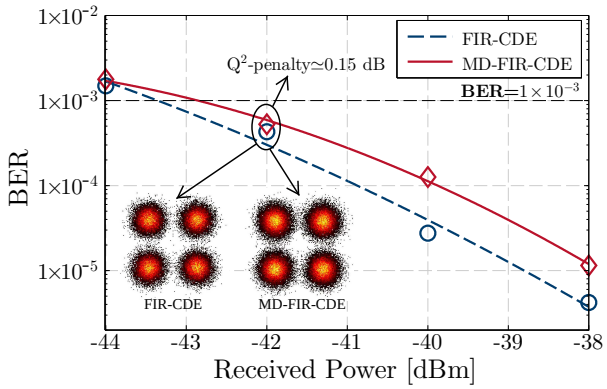

Figure 2: Real-time results of BER as a function of the received optical power after CD equalization with the MD-FIR-CDE, for $N = 83$ and $\Delta = 4$. The standard FIR-CDE applied in offline is utilized as a performance benchmark. The insets depict the obtained QPSK constellations after equalization with the FIR-CDE and MD-FIR-CDE algorithms for a fixed received power of -42 dBm.

Table 1: Hardware complexity occupation of MD-FIR-CDE in a Virtex-6 FPGA-XC6VLX240T for $\Delta = 4$.

	Slices	LUTs	Registers	DSP48E1s
MD-FIR-CDE	27%	21%	9%	0%

it is formed by a set of LUTs, registers, carry chain and multiplexers, which can be configured to form different logic circuits and DSP48E1s are used mainly in the multiplication operations. As its shown in Table 1, considering the Virtex-6 FPGA-XC6VLX240T, we have obtained an occupation of 27% of the total number of available slices, where 21% of LUTs and 9% of registers are used. In addition, we have confirmed 0% occupation of DSP48E1s, which reveals the high hardware complexity efficiency of MD-FIR-CDE ant its multiplierless operation. In contrast, the number of logic units required by the standard FIR-CDE has been found to largely surpass the available resources, thus preventing its real-time implementation in the considered FPGA platform. In accordance with the complexity analysis provided in the previous work [4, 6], these results demonstrate that the MD-FIR-CDE allows for an highly efficient FPGA implementation, also indicating that its usage on an application specific integrated circuit (ASIC) can result in significant gains both in terms of chip area and power consumption.

5. CONCLUSIONS

Using low-cost commercially available hardware, we have validated the MD-FIR-CDE in real-time mode operation, thereby demonstrating its hardware implementation feasibility and high computational efficiency. The hardware complexity of MD-FIR-CDE is shown to be highly efficient, occupying 21%, 9% and 0% of LUTs, registers and DSP48E1s, respectively. In addition the real-time performance of MD-FIR-CDE is compared with the maximum performance of FIR-CDE, revealing a reduced penalty in Q^2-factor of $\sim$0.15 dB. Finally, it is worth emphasizing that the demonstrated FIR-CDE architecture is based on a general structure that is fully modulation transparent and can also be applied to other linear equalization problems, including its potential benefit on reducing the complexity of digital backpropagation techniques for nonlinear compensation of fiber impairments, where the linear operator is known to be the largest source of complexity.

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