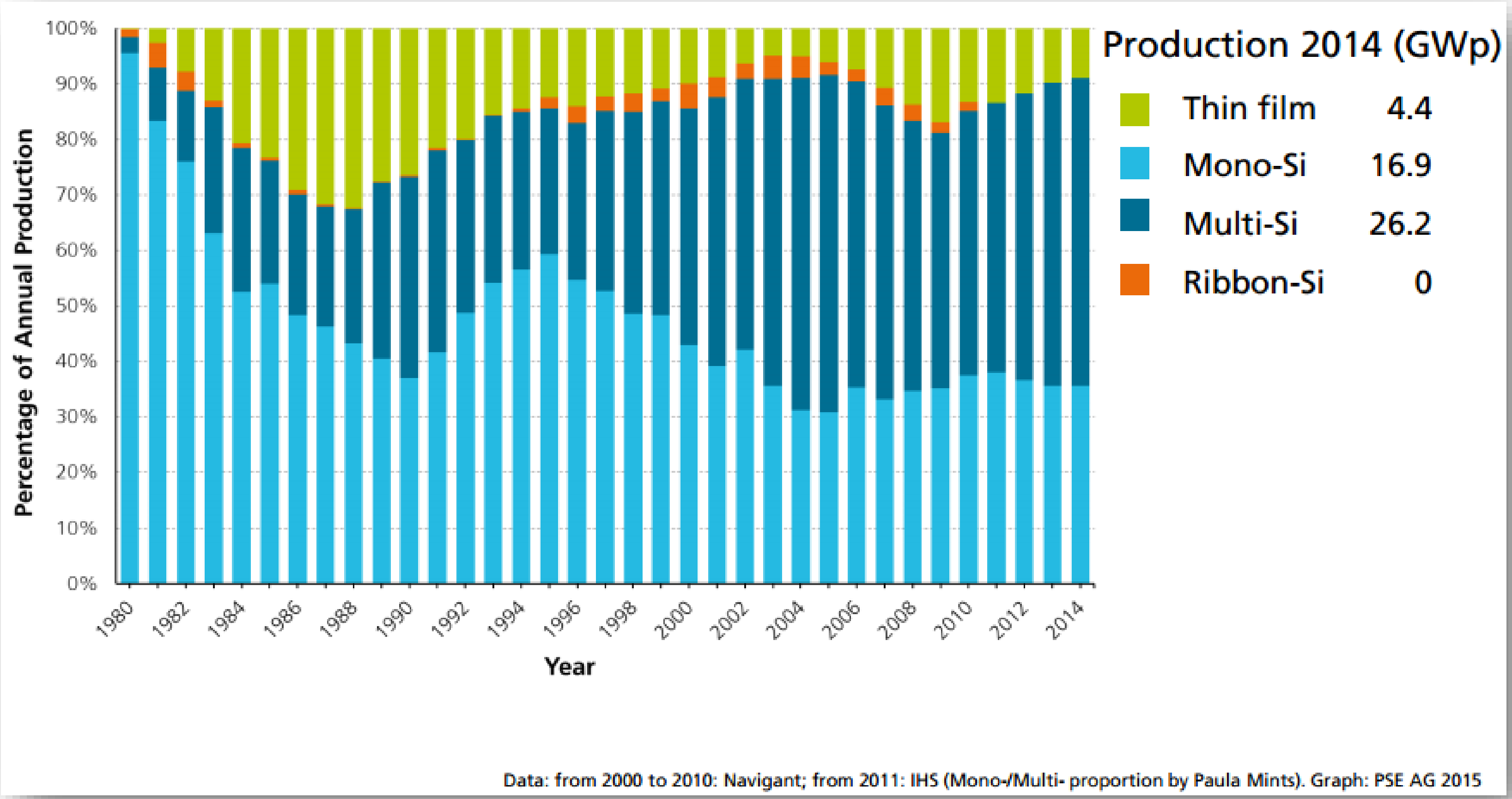
Thin epitaxial silicon foils using porous-silicon-based lift-off for photovoltaic application

Ivan Gordon

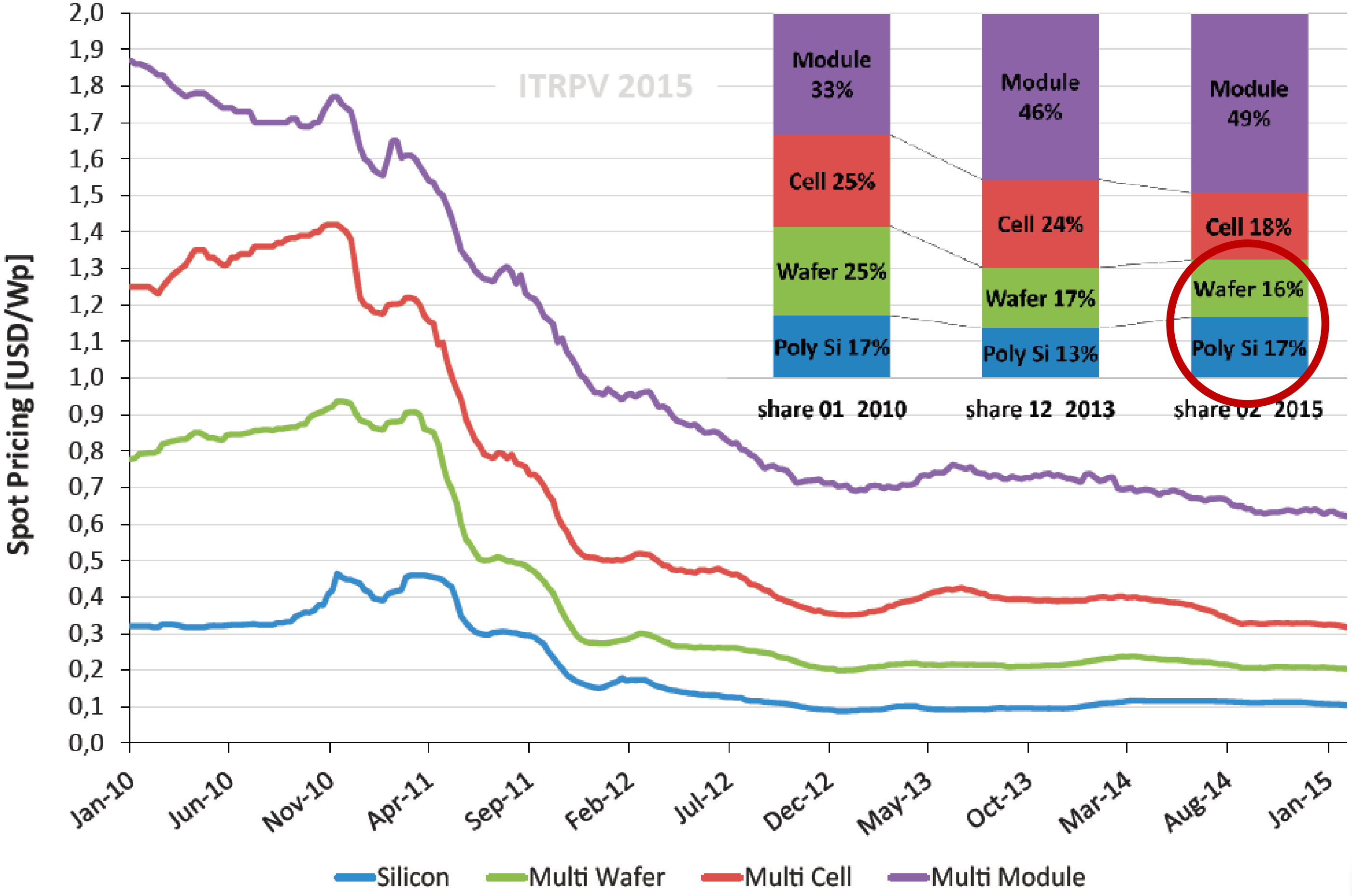
ASPIRE
INVENT
ACHIEVE

Crystalline silicon still dominates the photovoltaic market with a market share above 90%



 Photovoltaics report Fraunhofer ISE 2015

The cost of the silicon material constitutes 33% of the total Silicon PV module cost



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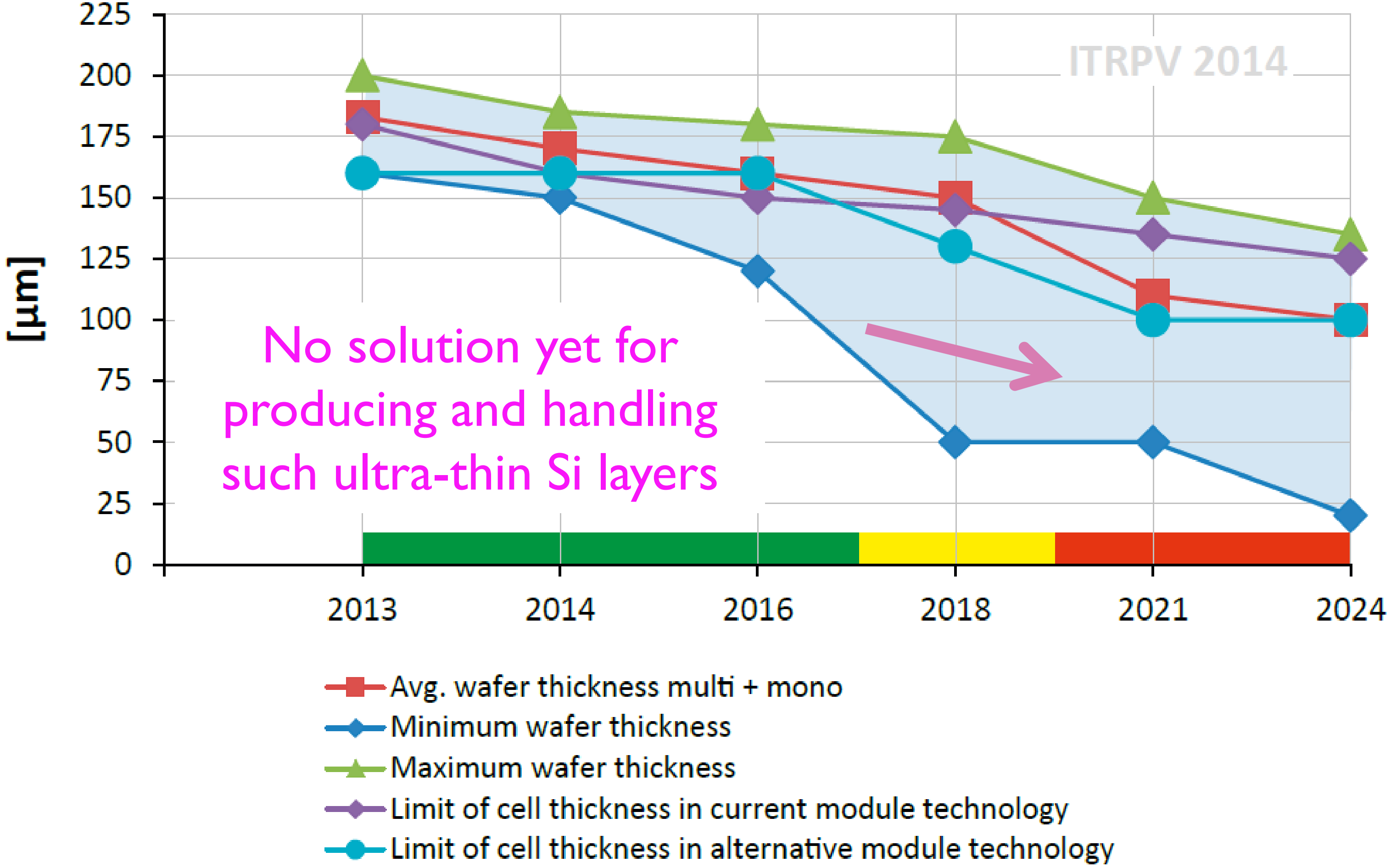
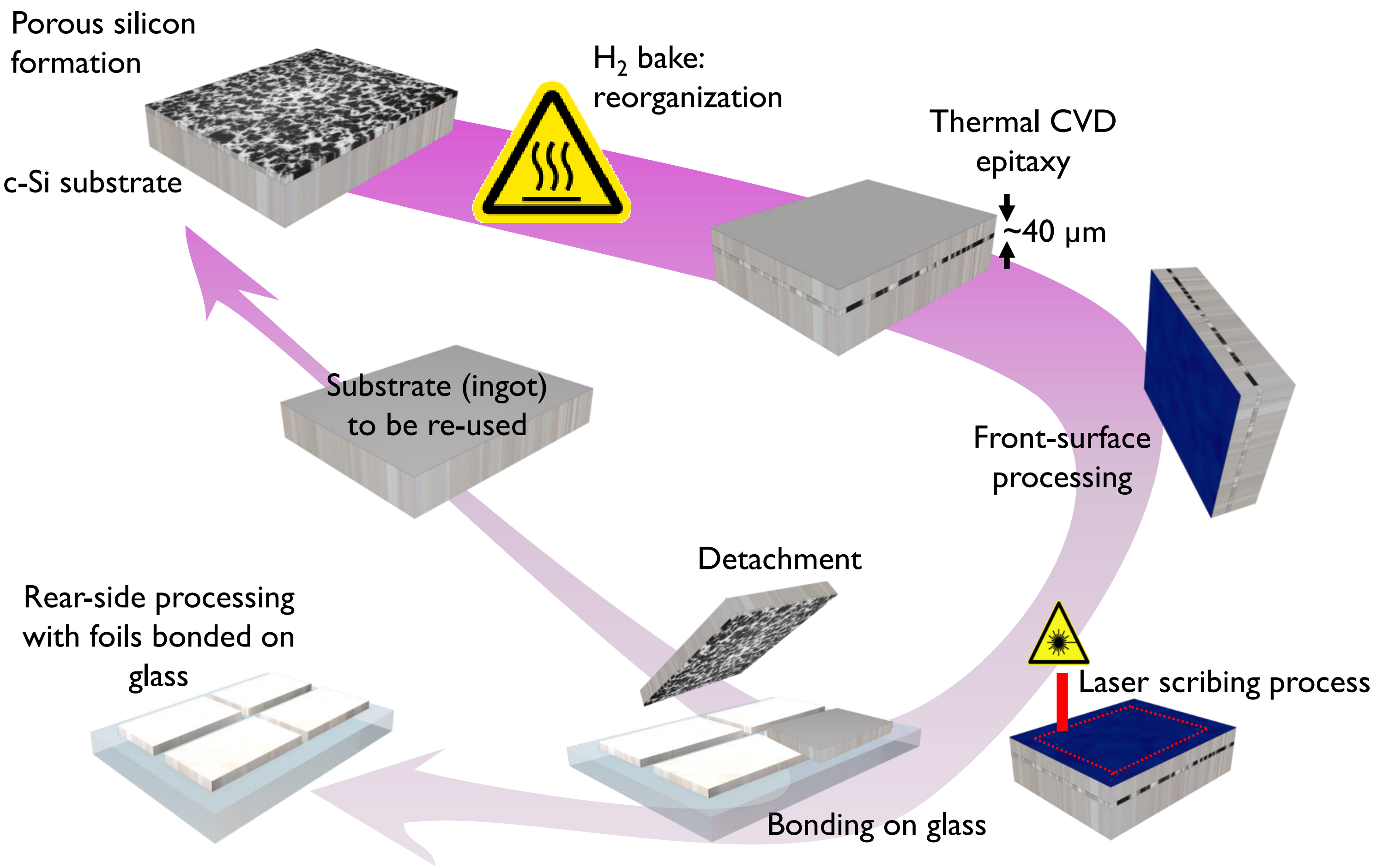
http://www.itrpv.net/

By reducing the silicon wafer thickness, the cost of Silicon PV modules can be decreased substantially



http://www.itrpv.net/

Imec's approach is based on epitaxial silicon foils



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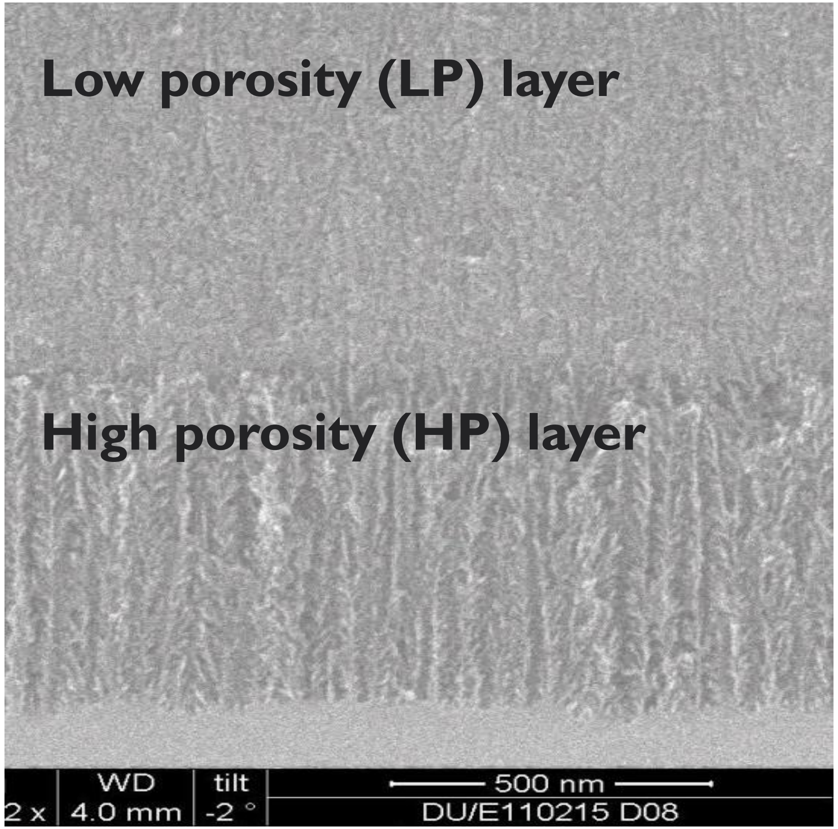
Outline

- Epitaxial foil development
- Solar cell development
- Conclusions

Epitaxial foil development

Porous silicon serves as template for epitaxy and as detachment layer

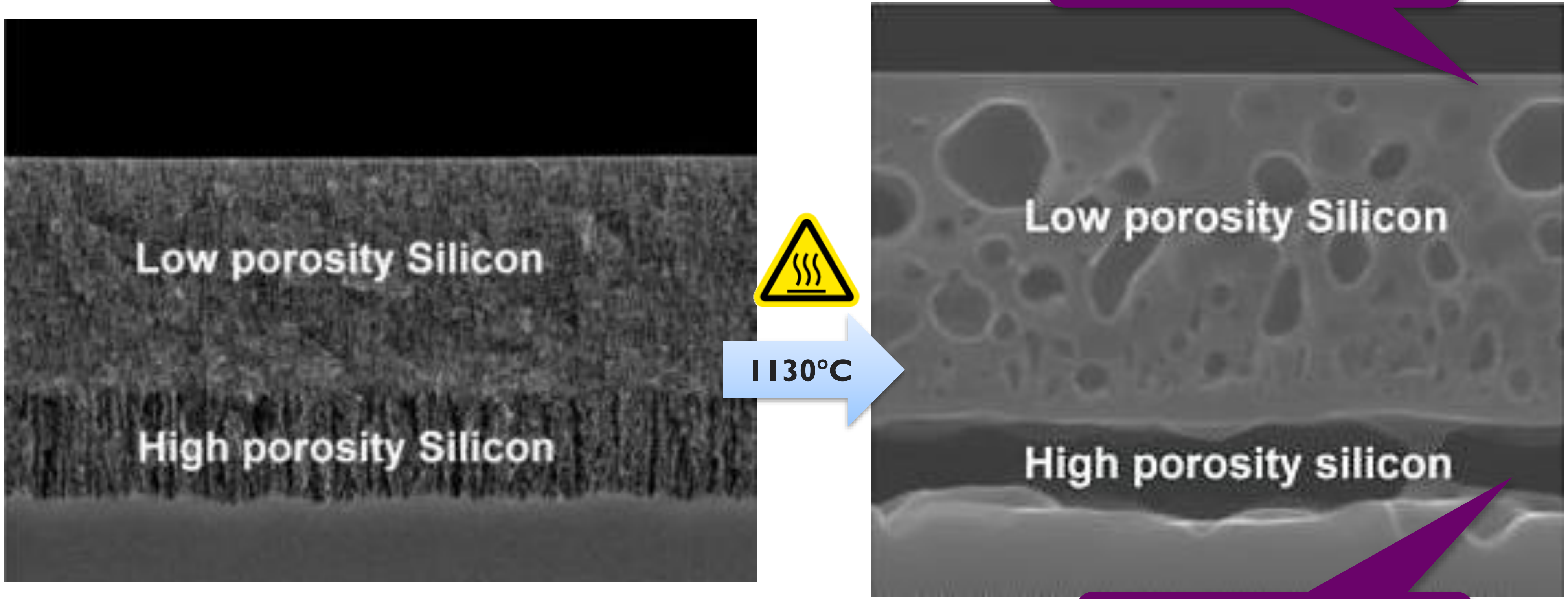


Electrochemical etching:

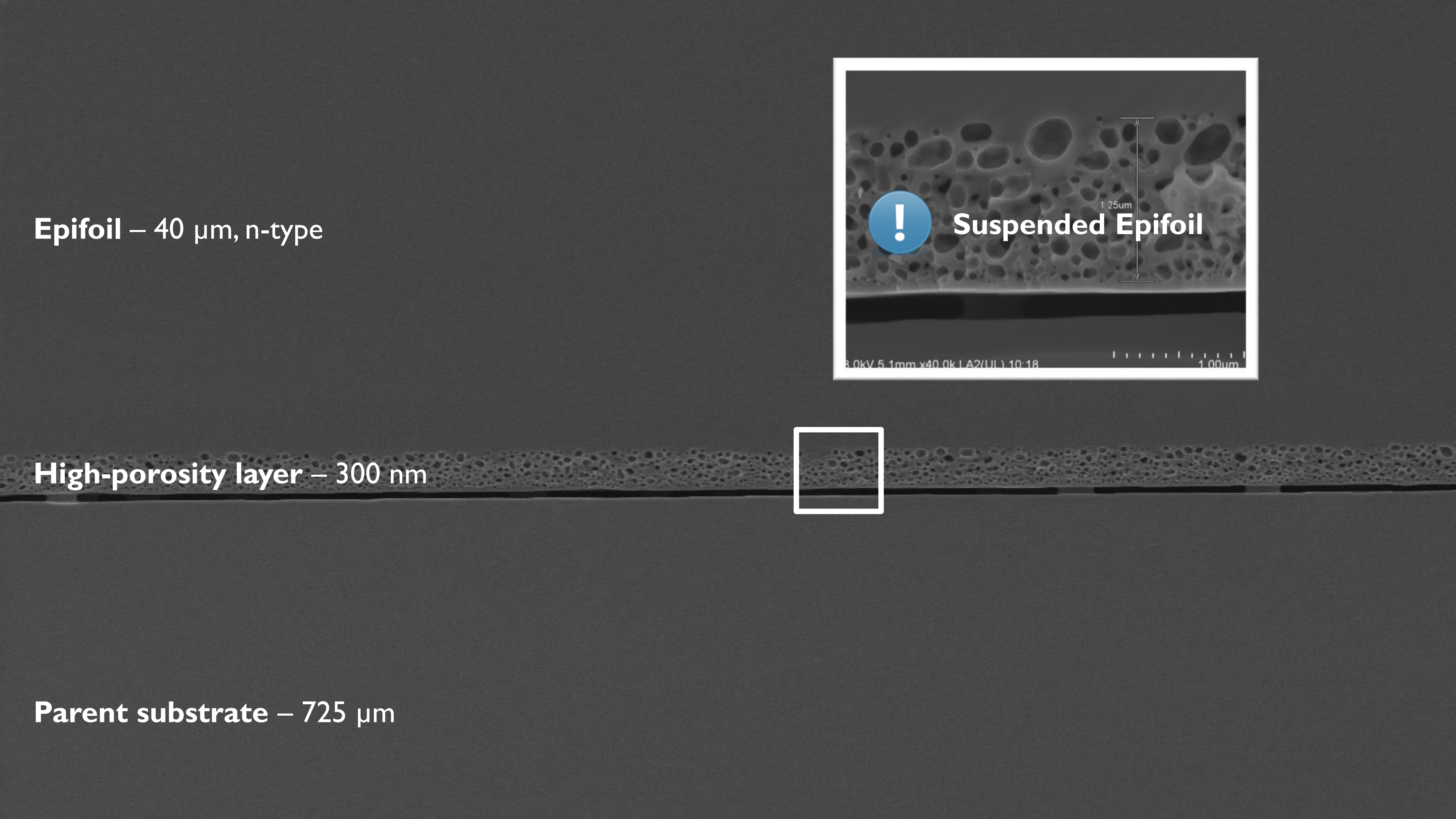
a **Low Porosity layer** (~30%)
➔ needed for epitaxy

a **High Porosity layer** (~60%)
➔ needed for detachment

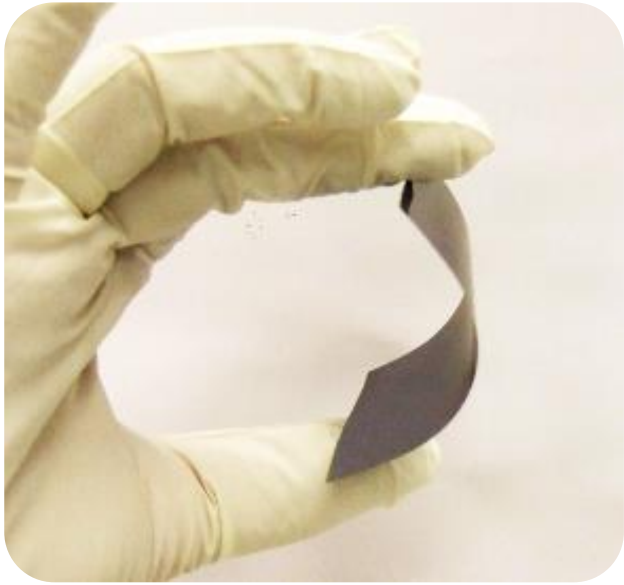
Porous silicon serves as template for epitaxy and as detachment layer



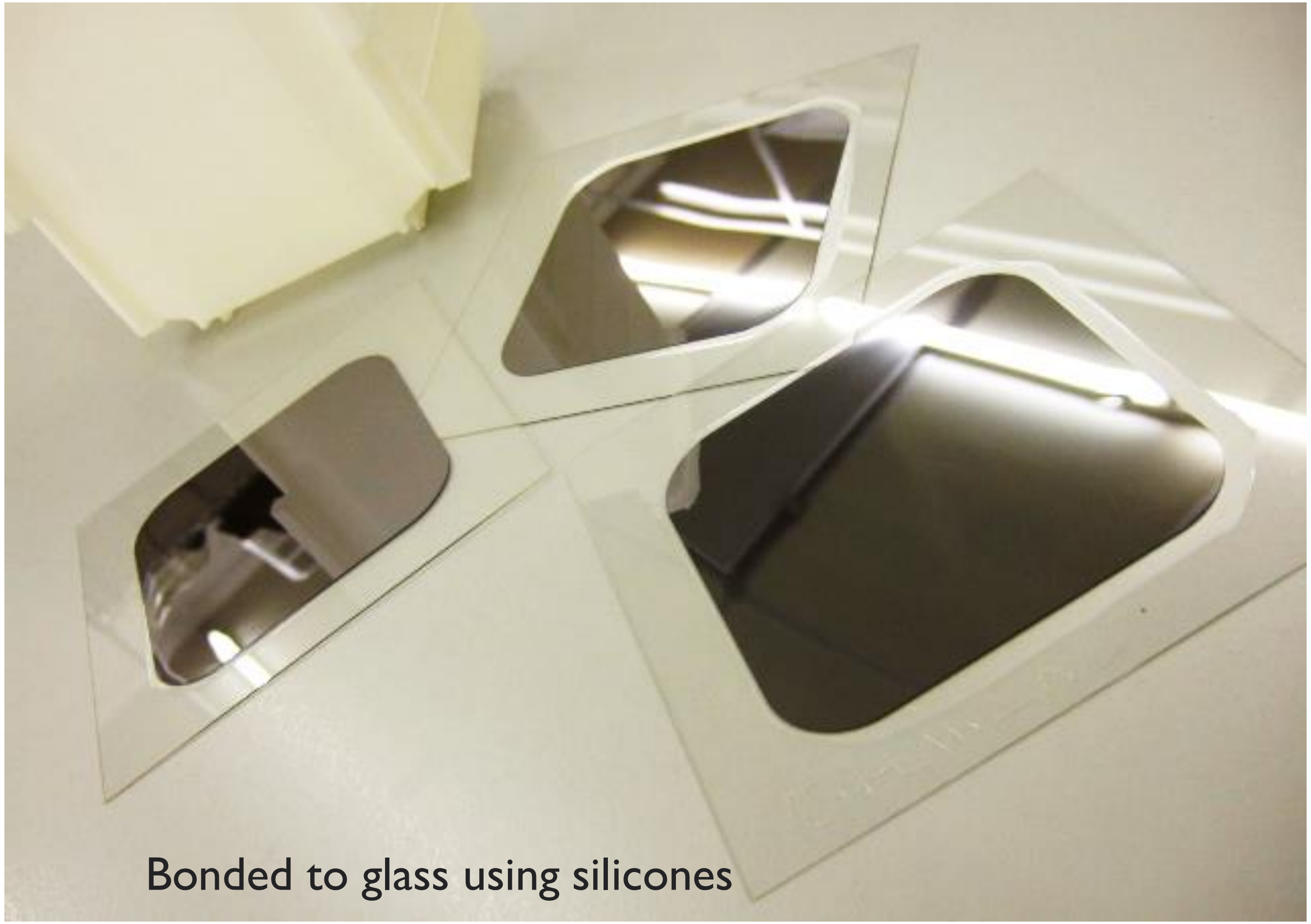
As-etched


Epifoil – 40 µm, n-type
1.25um
Suspended Epifoil
1.00um
High-porosity layer – 300 nm
Parent substrate – 725 µm

The foils can be detached from the parent substrate after epitaxial growth



Freestanding



Bonded to glass using silicones

We use the minority carrier lifetime as measure for the material quality of the epitaxial foils

The quality of the epifoil material depends on:

- The quality of the porous Si template for epitaxy
- The epitaxial deposition process itself
- The detachment process (quality of separation layer)

Lifetime measurements:

- Quasi Steady State PhotoConductance (QSSPC)
- Photolumicescence mapping (PL)

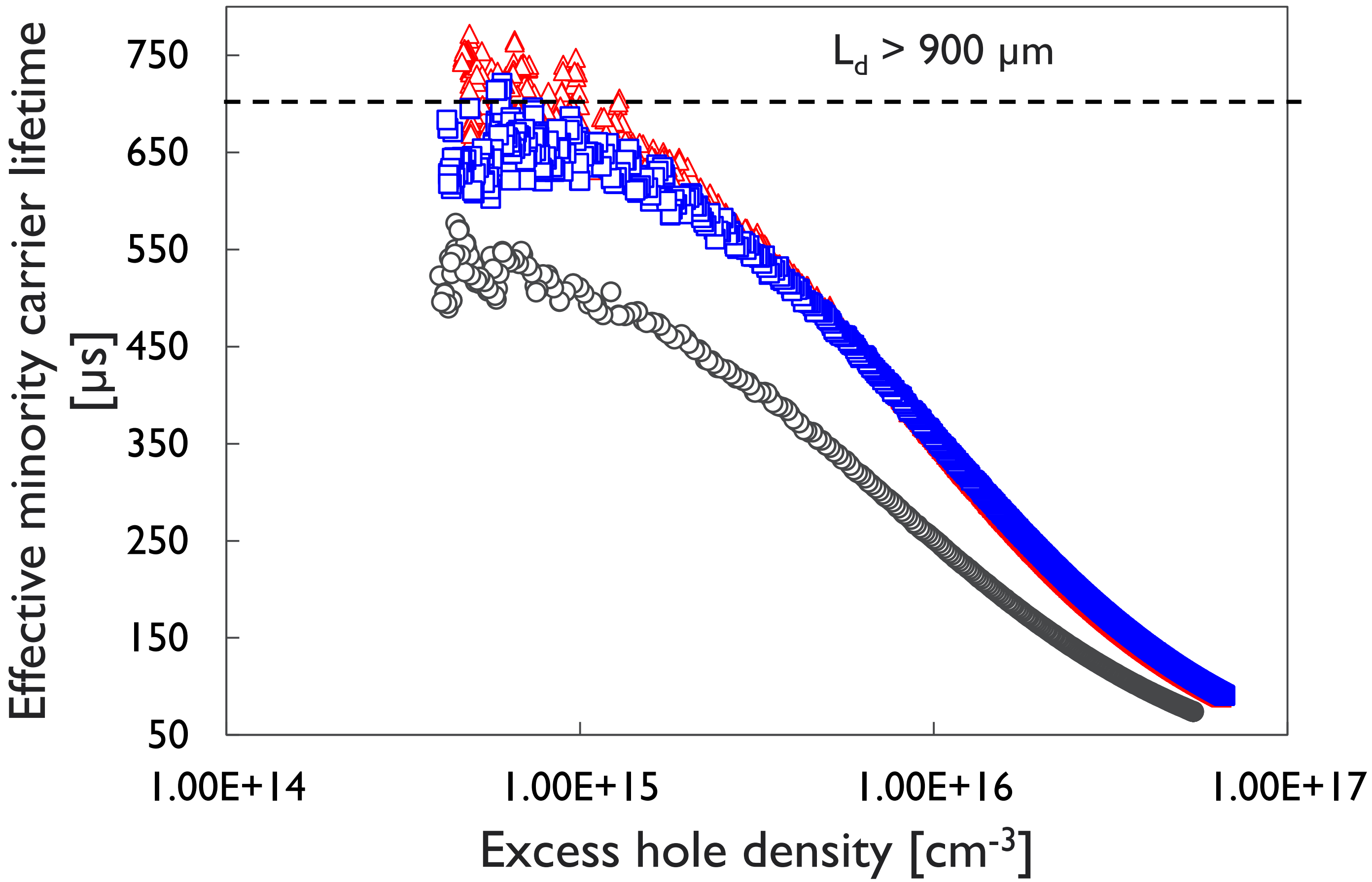
Applied on 5cm x 5cm foils double side textured foils (random pyramids)

We use the minority carrier lifetime as measure for the material quality of the epitaxial foils

- Laser scribing
- Detachment
- HF-dip
- TMAH etching (seed removal)
- $H_2SO_4 + H_2O_2$
- HF-dip
- a-Si i/n+ front-side
- a-Si i/n+ rear-side
- PL+QSSPC measurement

Applied on 5cm x 5cm foils
double side textured foils
(random pyramids)

High lifetimes have been obtained corresponding to bulk diffusion lengths of more than 25 times the layer thickness



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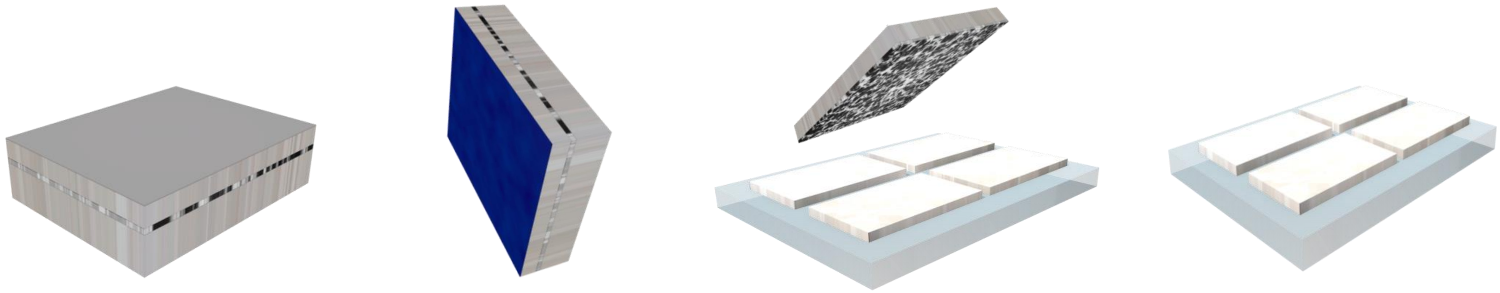
Solar cell development

From epitaxial silicon foils to devices on glass



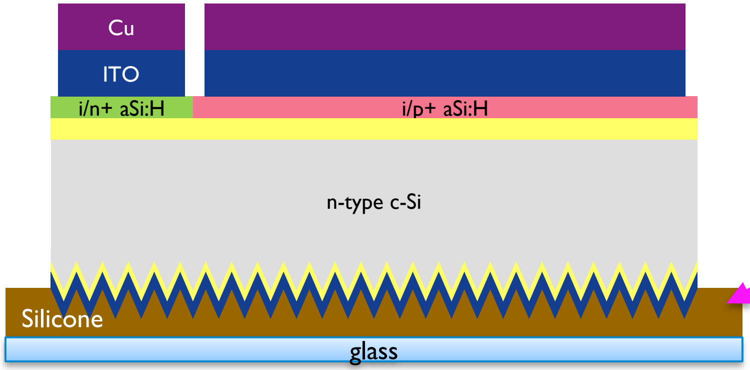
Thermal CVD epitaxy

Front-surface processing

Bonding on glass and detachment

Rear-side processing with foils bonded on glass

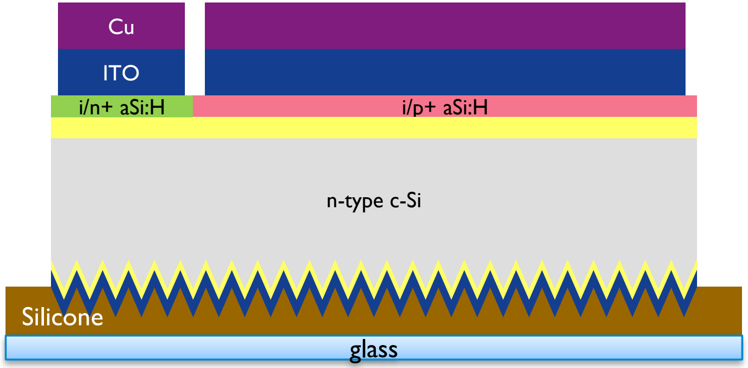
Targeted cell structure based on a-Si heterojunction and back contacts (SHJ-IBC)



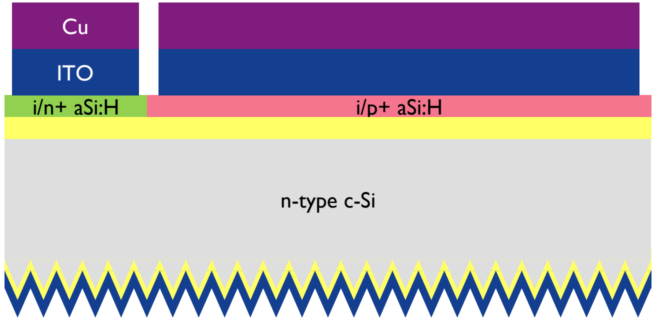
Presence of silicones can lead to problems when using PECVD to grow the a-Si layers

An SHJ-IBC cell process compatible with presence of silicones was developed successfully on Fz wafers of regular thickness

Bonded



Freestanding



Excellent surface passivation despite presence of silicones

Type	Jsc [mA/cm²]	Voc [mV]	FF [%]	Eta [%]
Bonded (silicones)	40.8	**734**	73.1	21.7
Freestanding	41.8	**730**	74.5	22.6

Cell area: 3.97cm²
FZ (200 µm, 3Ω-cm)

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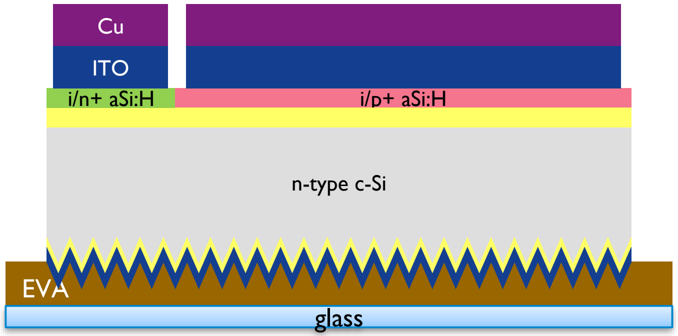
The SHJ-IBC cell process was also demonstrated on ultra-thin silicon Fz wafers



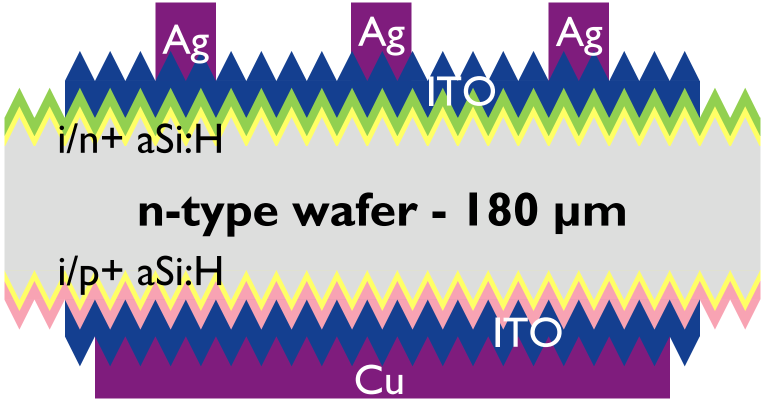
In this experiment, the bonding was done by EVA instead of silicones

Starting thickness [um]	Jsc [mA/cm²]	Voc [mV]	FF [%]	Eta [%]
190	39.9	724	71.6	20.7
56	38.5	737	69.2	19.6

Cell area: 3.97cm²
FZ wafers of various thickness

Slight decrease in efficiency for thin cells due to lower Jsc and FF

To test the quality of our epitaxial foils at device level we developed a simple freestanding cell process



Type	Jsc [mA/cm²]	Voc [mV]	FF [%]	Eta [%]
Cz – 180 um	36.5	729	73.3	19.5

- Texturing
- i/n+ aSi:H deposition front
- i/p+ aSi:H deposition rear
- ITO deposition front
- ITO deposition rear
- Cu deposition rear (e-beam)
- Ag low-T screenprinting

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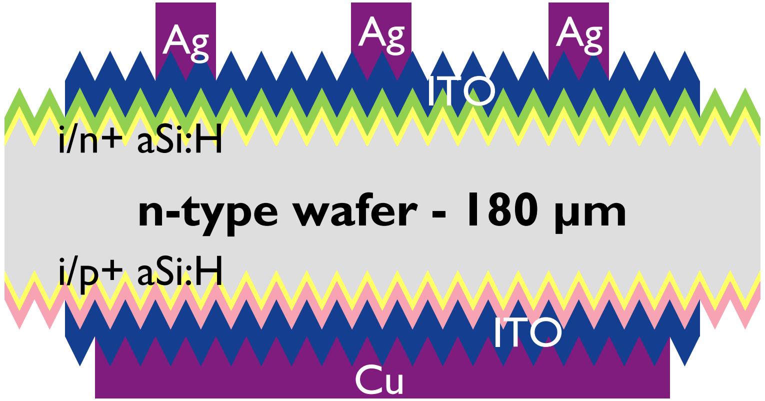
First freestanding cells made from epitaxial foils confirm the high electronic quality of the silicon foils



Type	Jsc [mA/cm²]	Voc [mV]	FF [%]	Eta [%]
Cz – 180 um	36.5	729	73.3	19.5
Foil – 40 um	34.0	662	68.0	**15.3**
Foil – 40 um	34.7	**715**	40.4	10.0

Cell area: 4 cm^2

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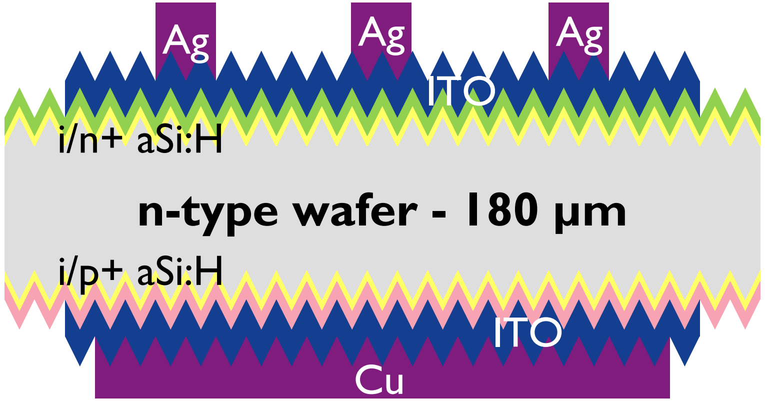

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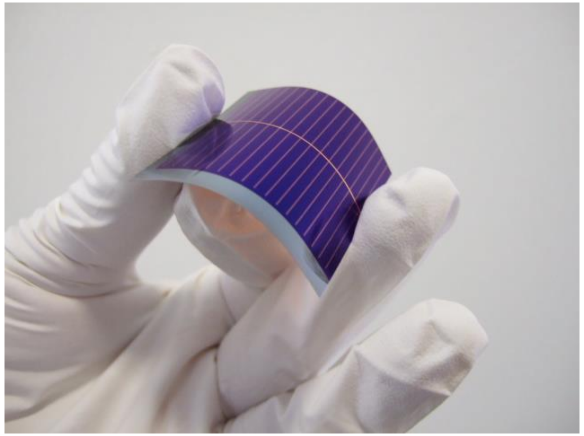
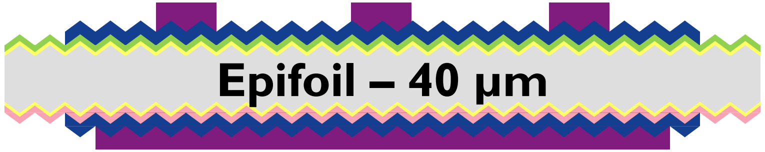


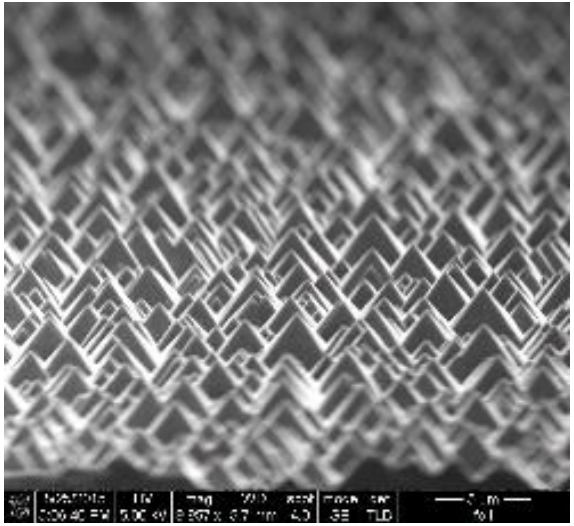
Cell area: 4 cm^2

Light in-coupling is very important for solar cells based on thin silicon foils

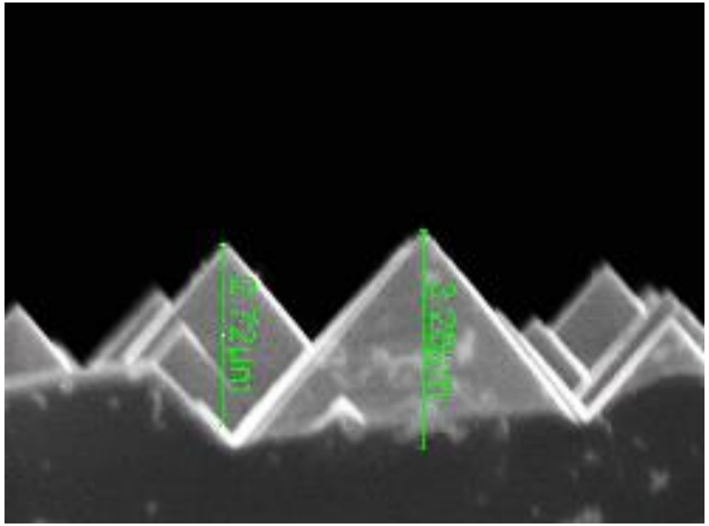


Surface texturing is mandatory to get good light in-coupling

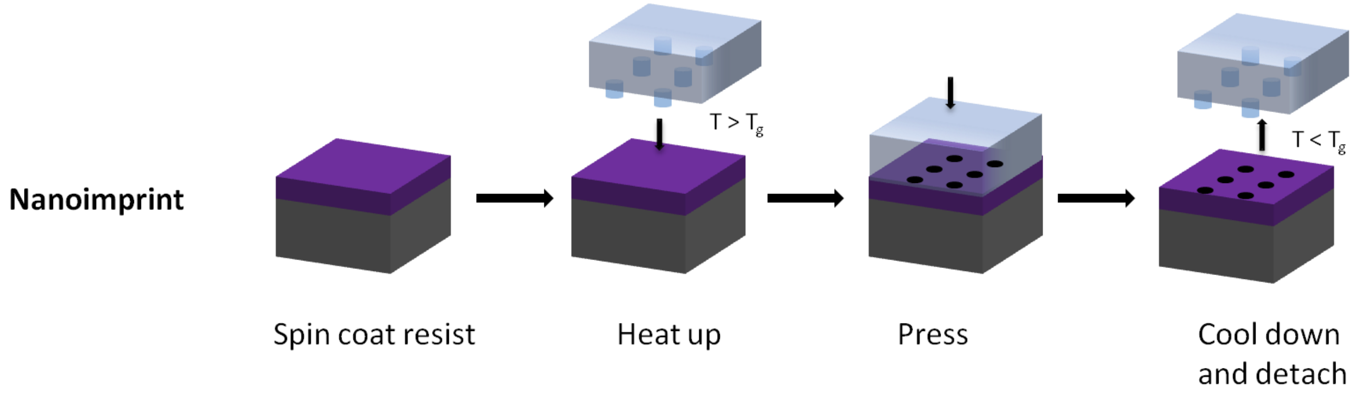
Random pyramid texturing of epitaxial silicon foils is possible

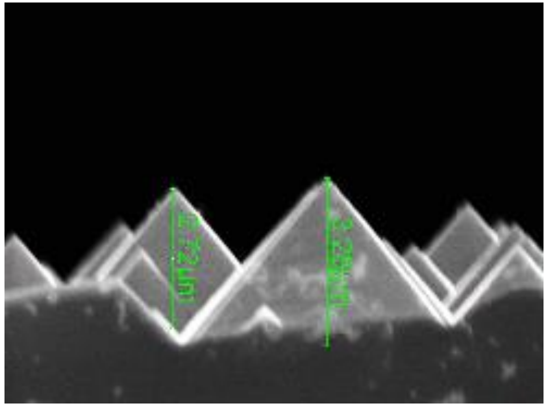


However: 3-5 um of silicon gets etched on each side

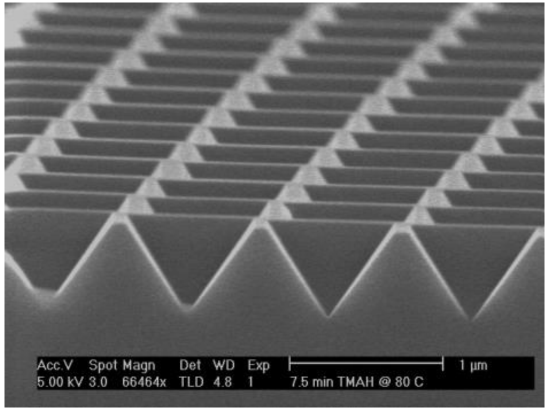


Inverted nano-pyramids made by nano-imprint lithography are an alternative to random pyramid texture leading to less silicon removal



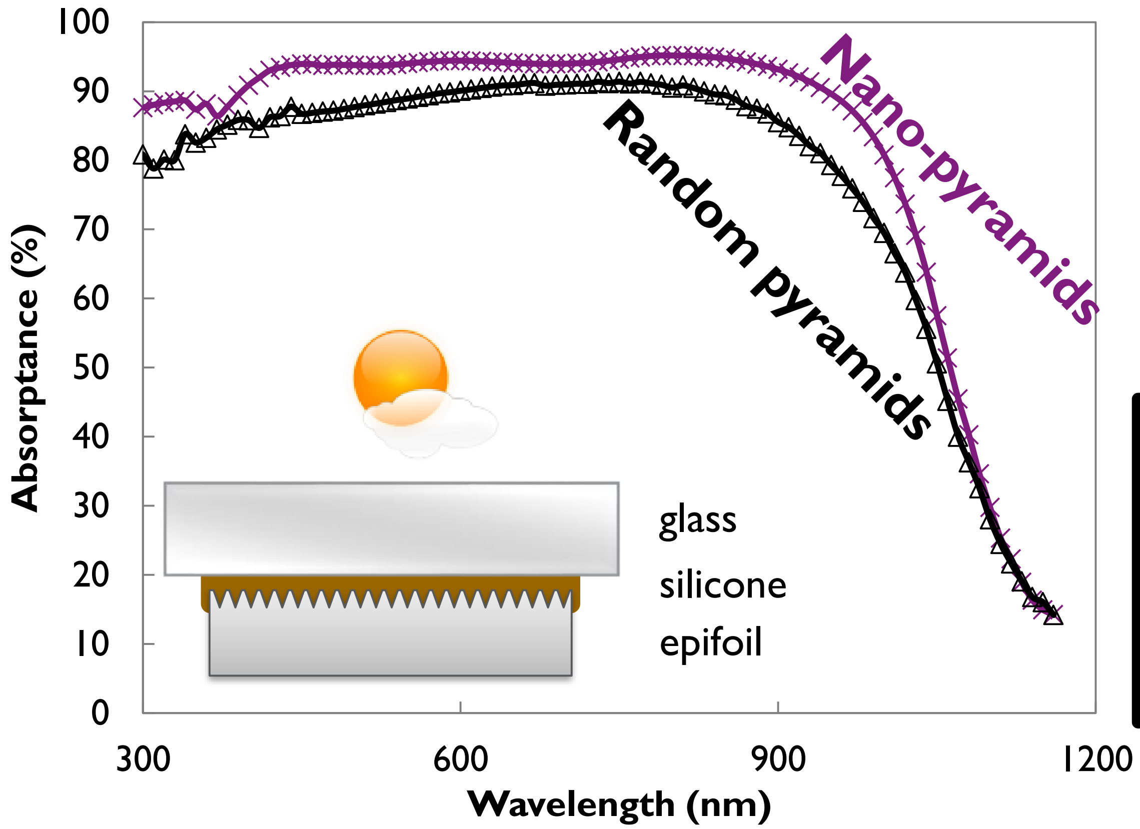


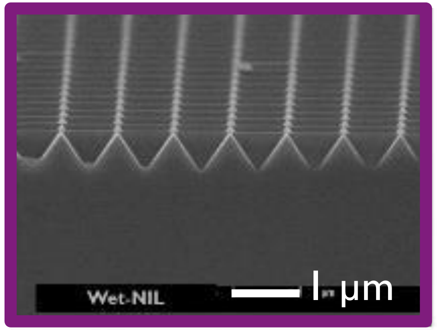
Random pyramids via KOH etching:
3-5 um Si removal

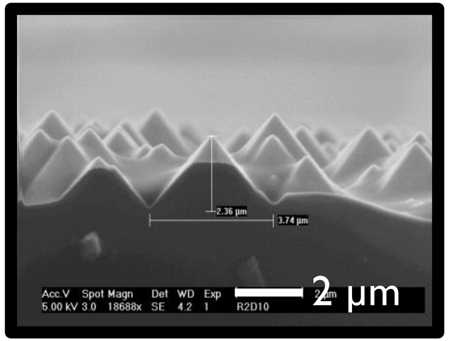


Inverted nano-pyramids by nano-imprint:
0.5 um Si removal

Inverted nano-pyramids can optically outperform standard random pyramid texture







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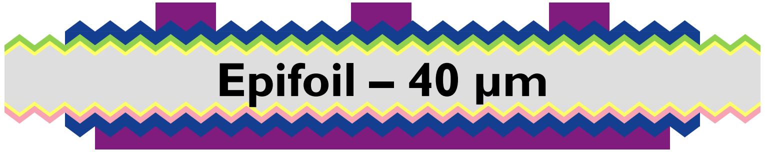
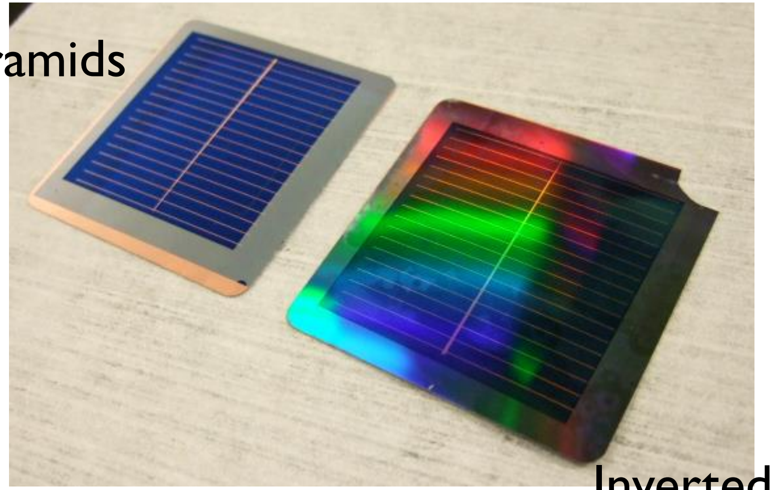
Experiment performed in collaboration with the company Obducat

Inverted nano-pyramids lead to higher Jsc values than random pyramids in freestanding cells made from thin foils



Random pyramids



Inverted nano-pyramids

Type	Jsc [mA/cm²]	Voc [mV]	FF [%]	Eta [%]
Random pyramids	**34.2**	670	47.2	10.8
Inverted nano-pyramids	**35.6**	664	48.6	11.5

CONCLUSIONS

Conclusions

- Porous-silicon based lift-off in combination with epiaxial silicon deposition can produce ultrathin silicon foils
- The resulting foils show minority carrier diffusion lengths which are 25 times as high as the foil thickness
- An SHJ-IBC cell process for silicon bonded to glass using silicones was developed leading to very high efficiencies and Voc values
- First cells with a simple cell structure were made from the epitaxial foils leading to efficiencies up to 15.3%
- Inverted nano-pyramids made by nano-imprint lithography can lead to higher Jsc values than random pyramids in cells made from epitaxial foils

Acknowledgements

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