Thin epitaxial silicon foils using porous-silicon-based lift-off for photovoltaic application

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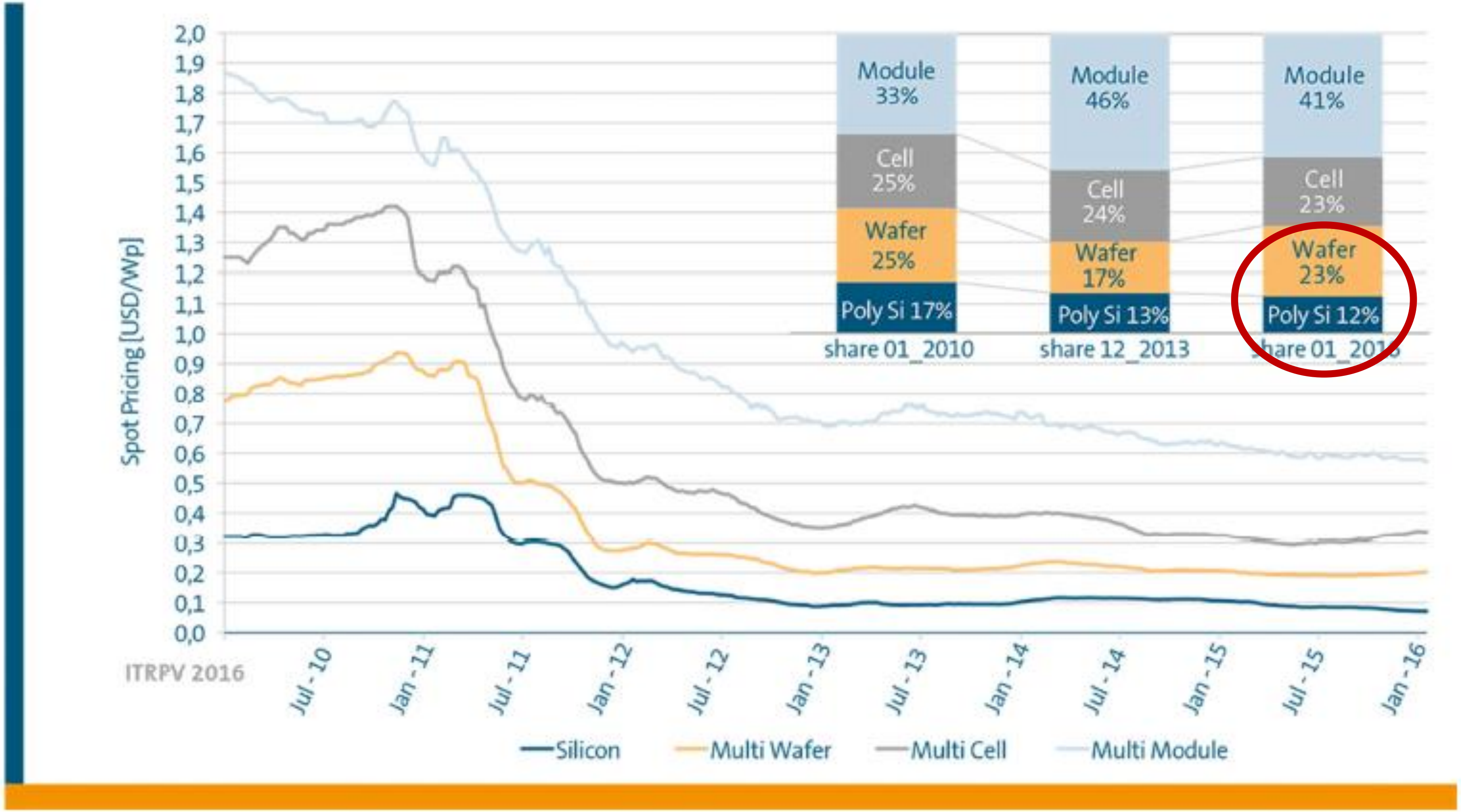
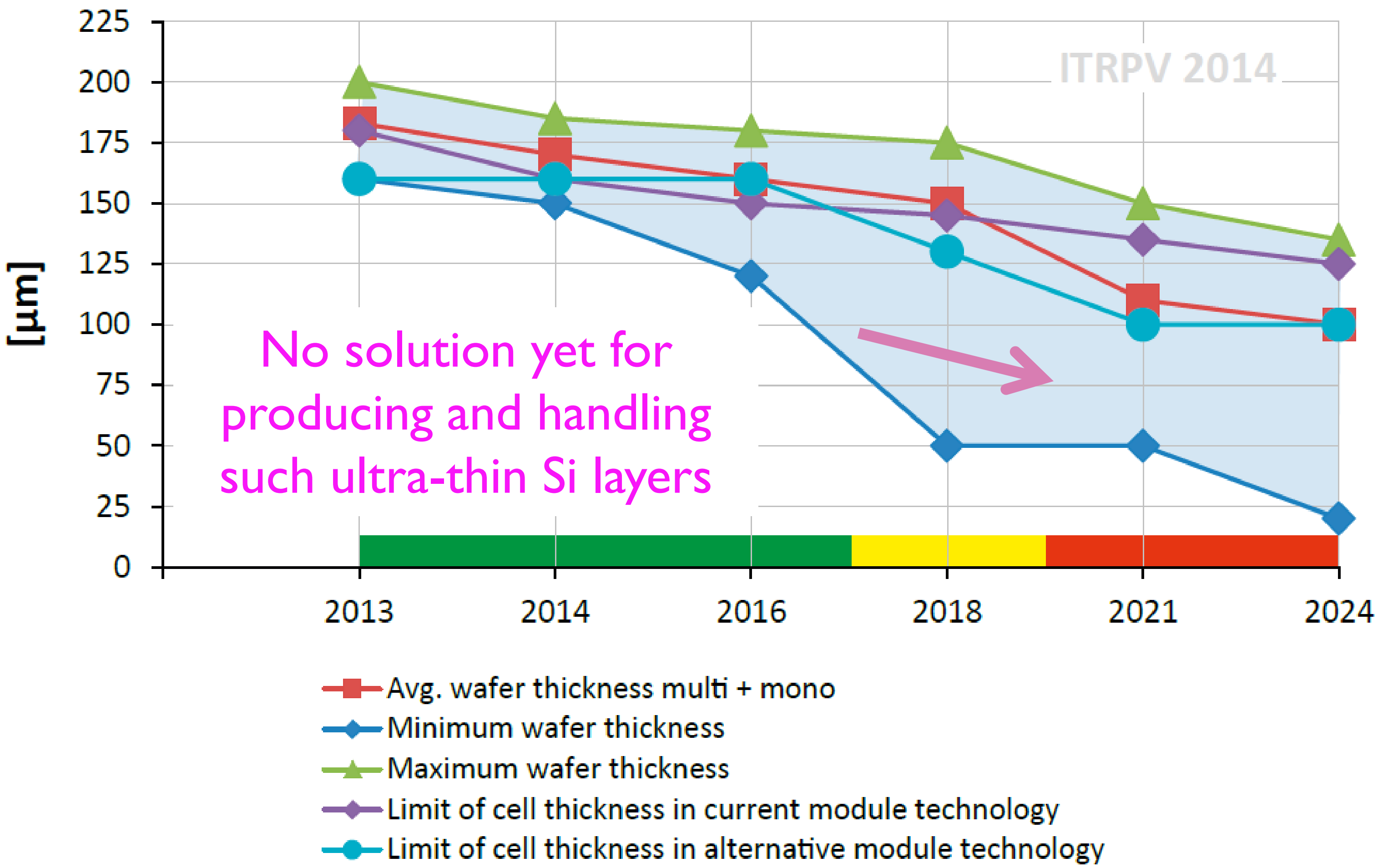
The cost of the silicon material constitutes 35% of the total Silicon PV module cost

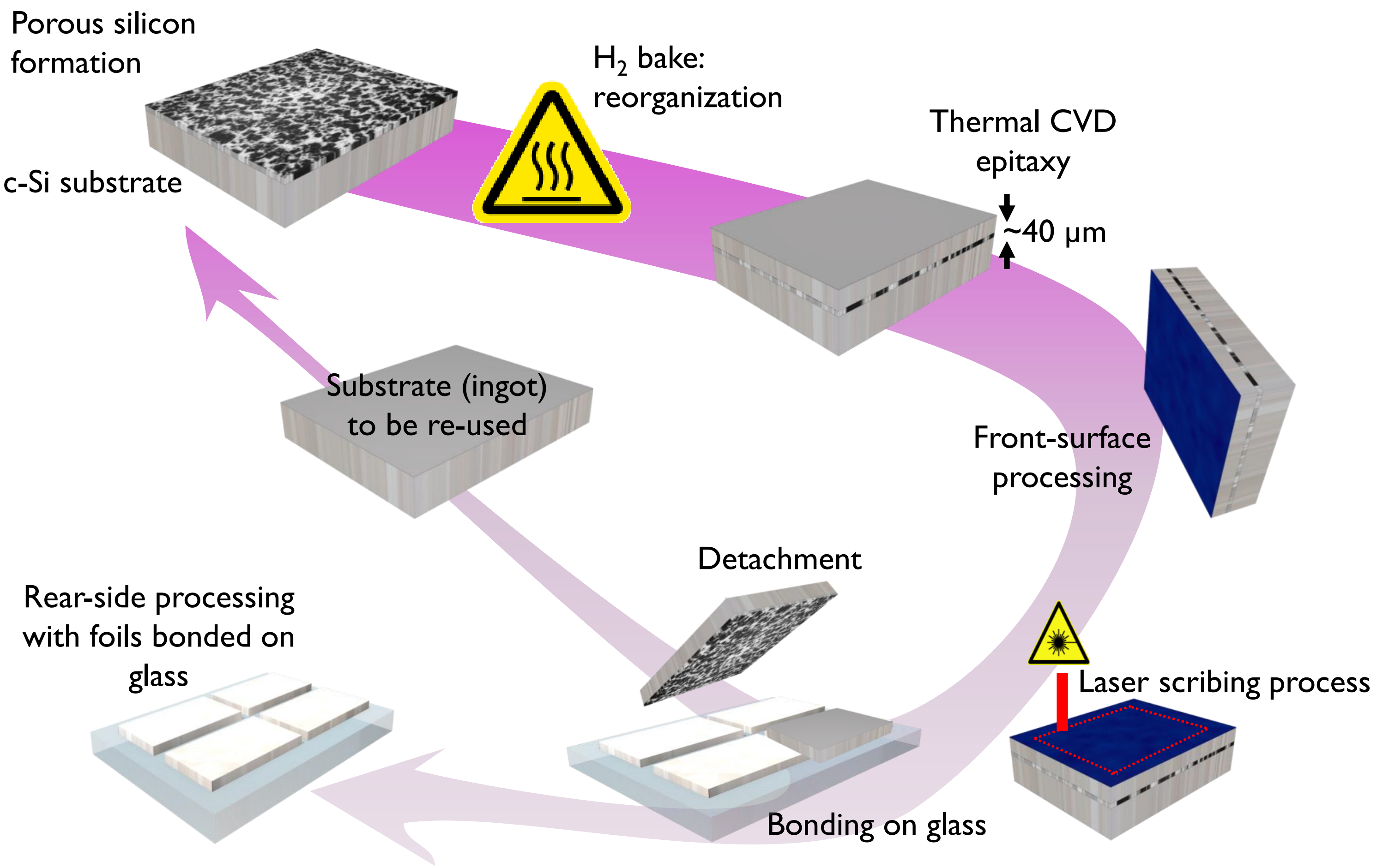


http://www.itrpv.net/

By reducing the silicon wafer thickness, the cost of Silicon PV modules can be decreased substantially



Imec's approach is based on epitaxial silicon foils

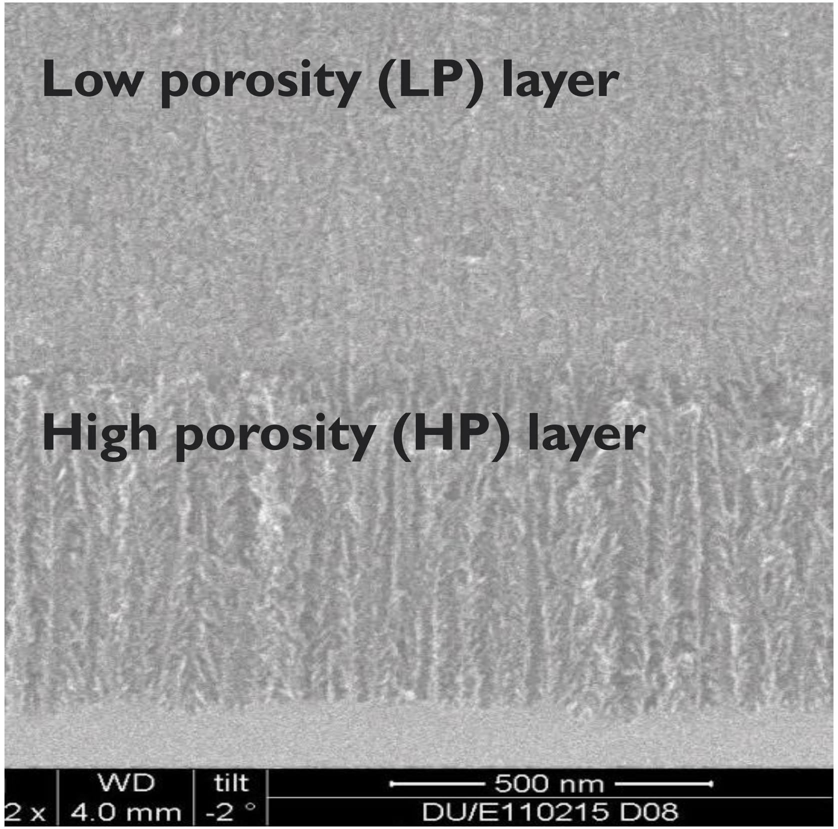


Outline

- Epitaxial foil development
- Solar cell development
- Conclusions

Epitaxial foil development

Porous silicon serves as template for epitaxy and as detachment layer

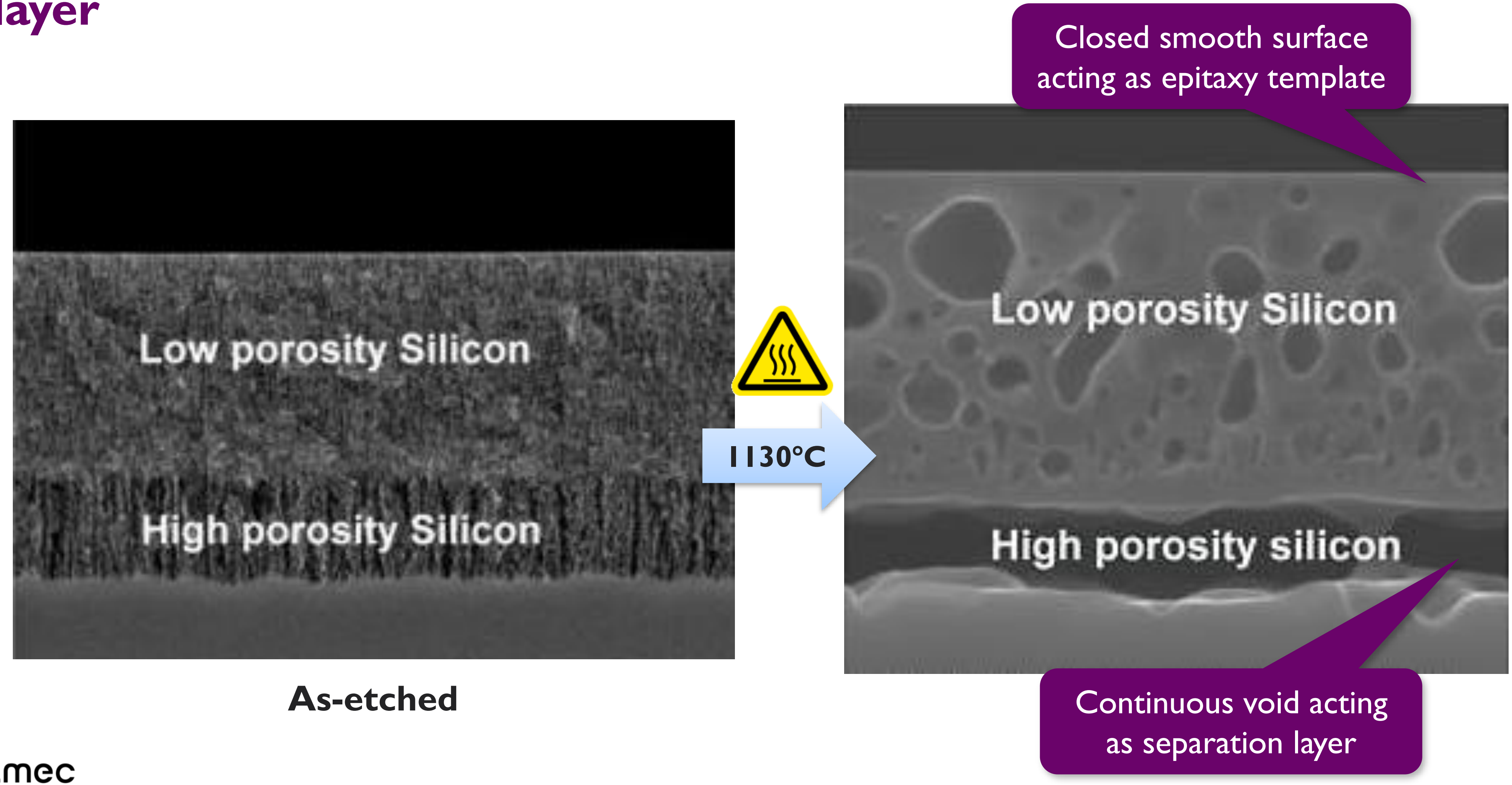


Electrochemical etching:

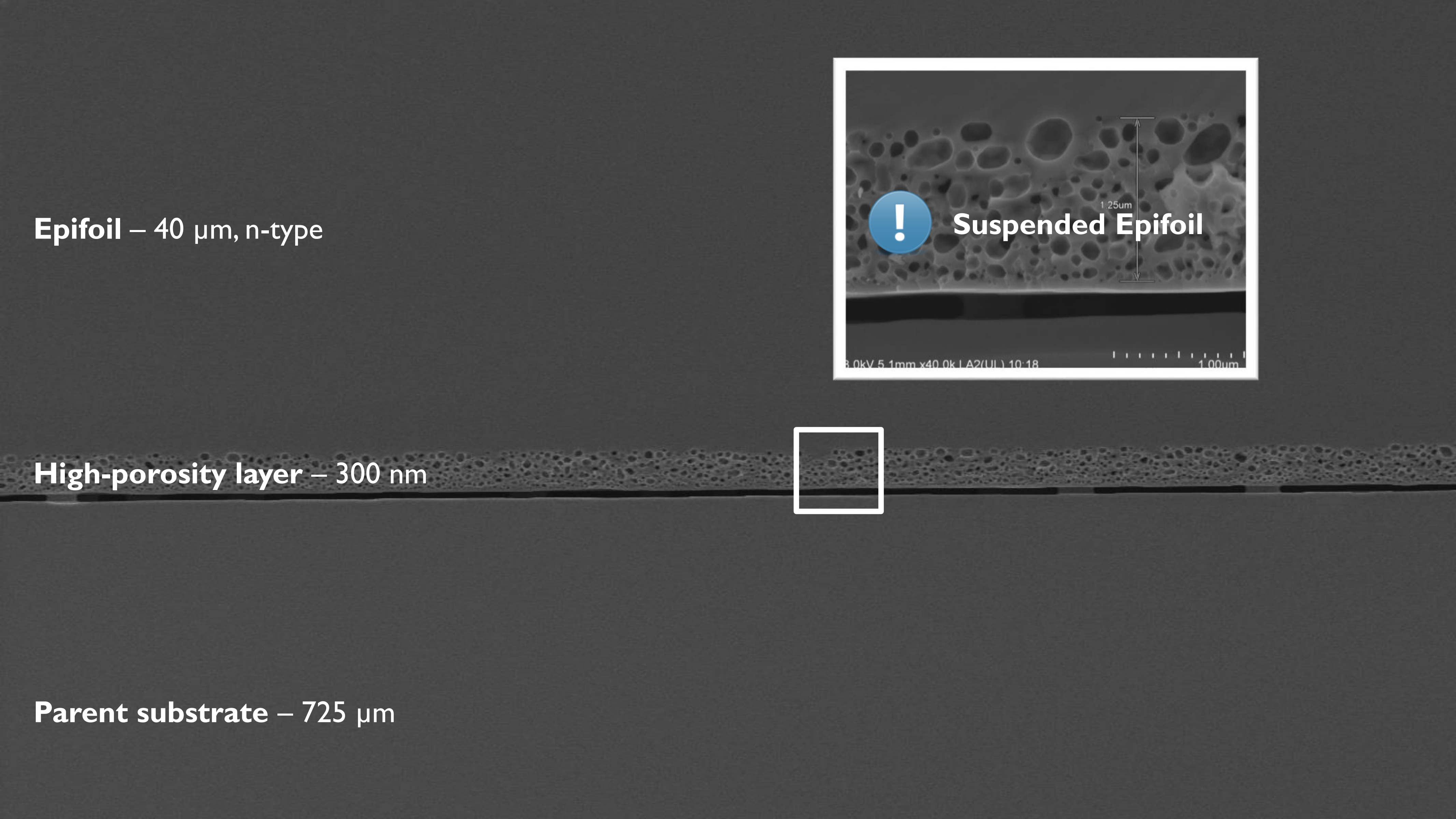
a **Low Porosity layer** (~30%)
➔ needed for epitaxy

a **High Porosity layer** (~60%)
➔ needed for detachment

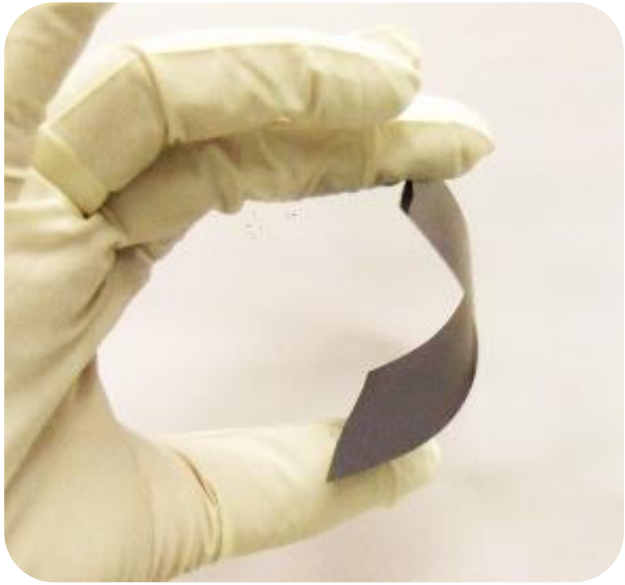
Porous silicon serves as template for epitaxy and as detachment layer



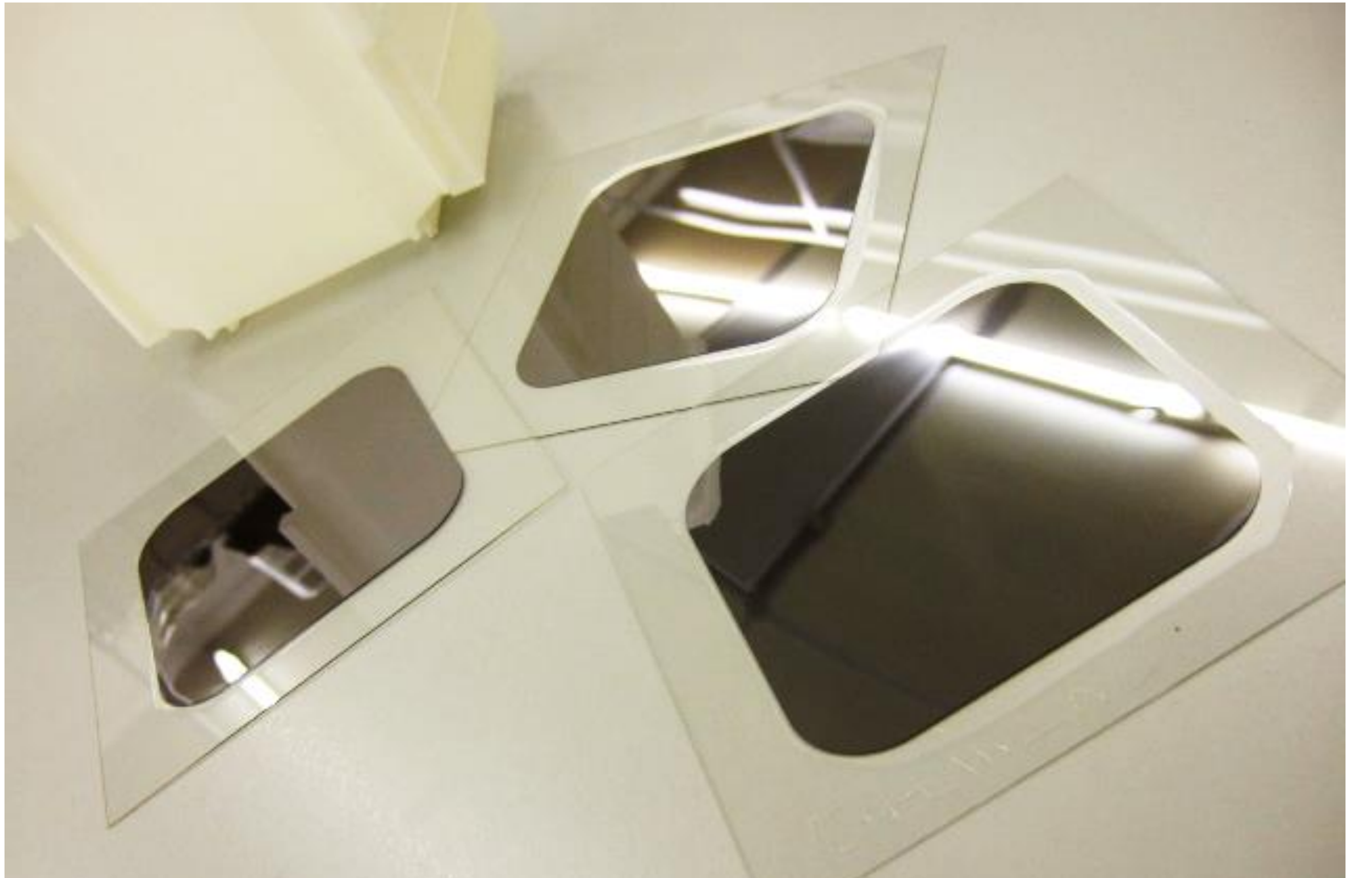
As-etched


Epifoil – 40 µm, n-type
High-porosity layer – 300 nm
Parent substrate – 725 µm
Suspended Epifoil
1.25um
1.00um

The foils can be detached from the parent substrate after epitaxial growth

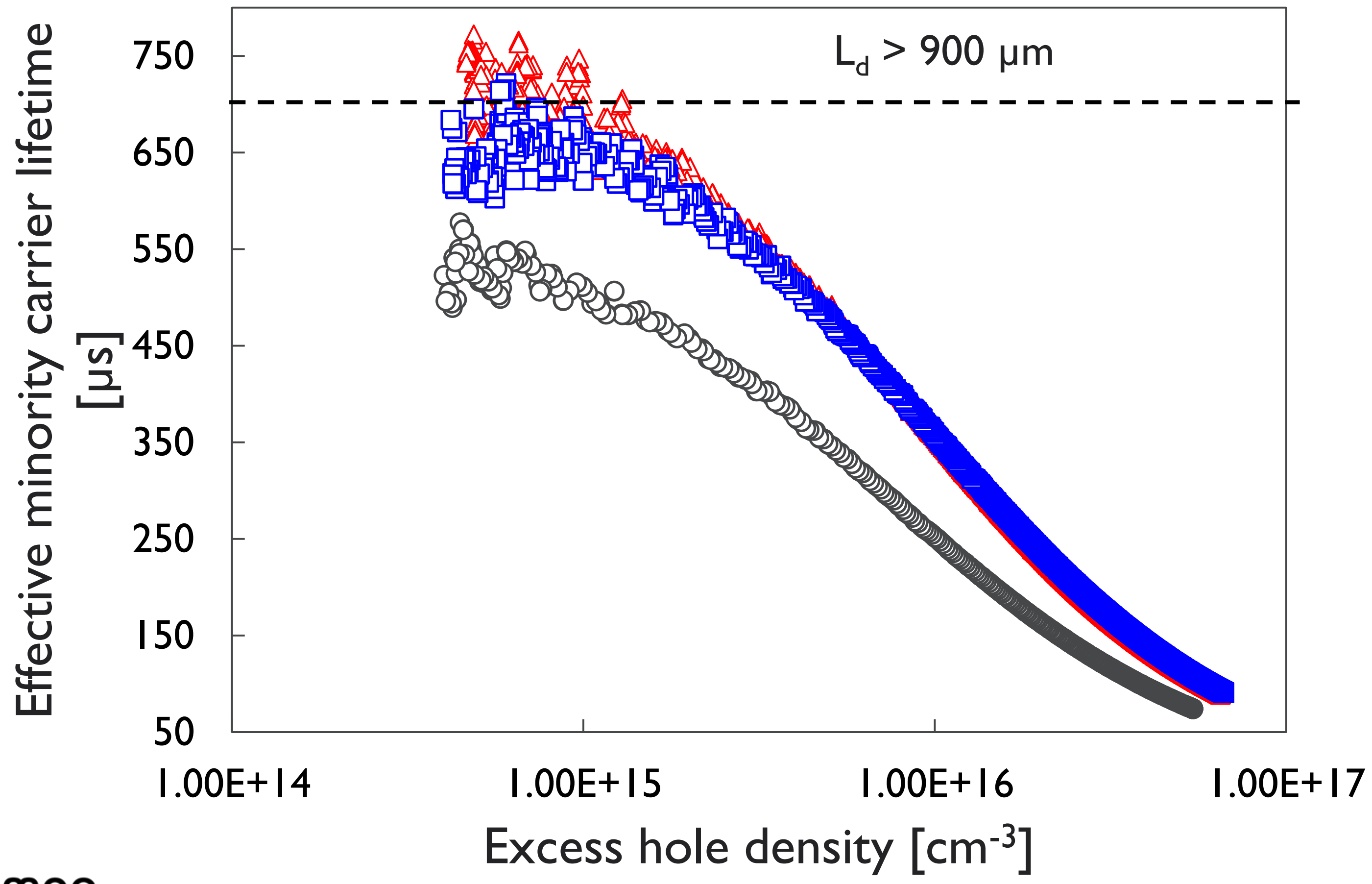


Freestanding

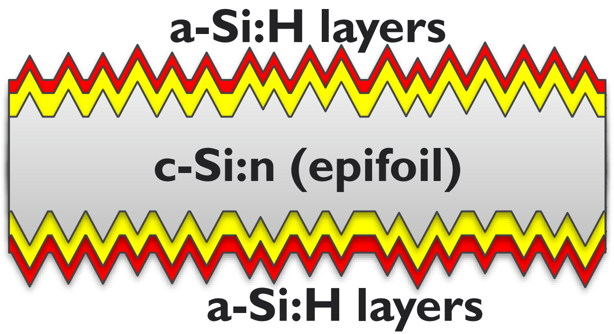


Bonded to glass using silicones

High lifetimes have been obtained corresponding to bulk diffusion lengths of more than 25 times the layer thickness



Measurement configuration:



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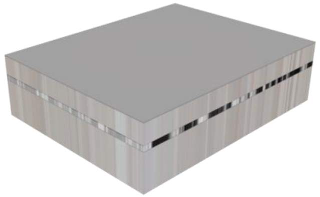
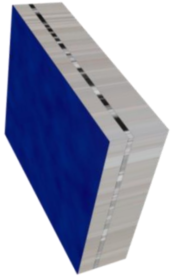
Solar cell development

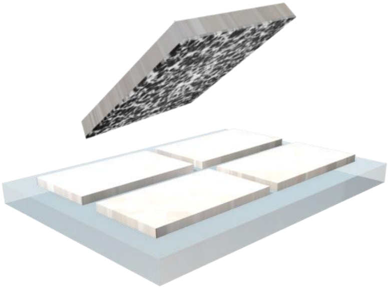
From epitaxial silicon foils to devices on glass



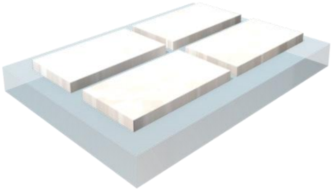
Thermal CVD epitaxy



Front-surface processing

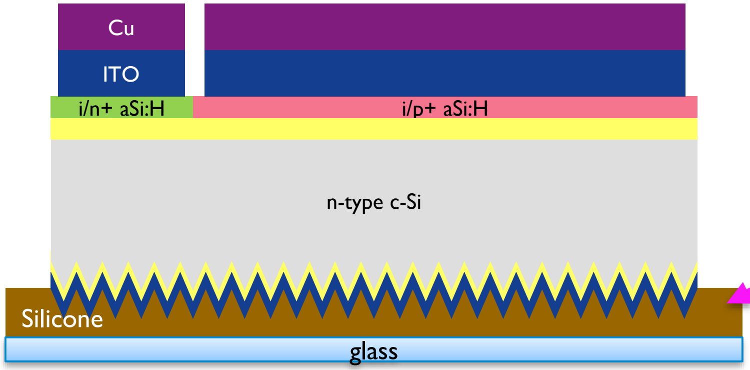


Bonding on glass and detachment



Rear-side processing with foils bonded on glass

Targeted cell structure based on a-Si heterojunction and back contacts (SHJ-IBC)



Presence of silicones can lead to problems when using PECVD to grow the a-Si layers

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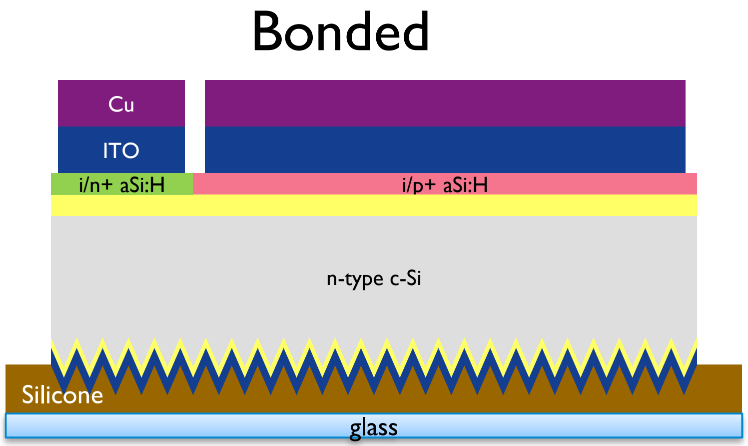
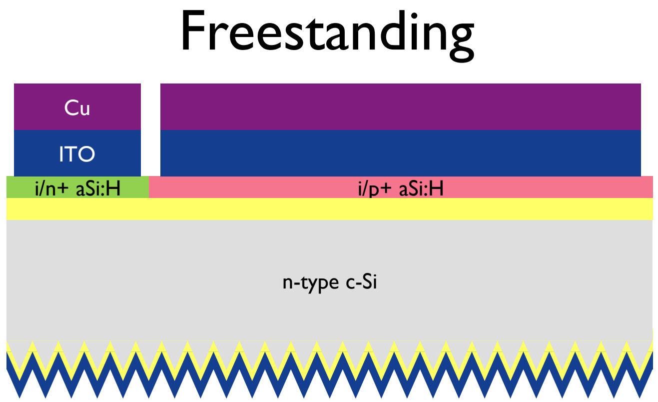
An SHJ-IBC cell process compatible with presence of silicones was developed successfully on Fz wafers of regular thickness



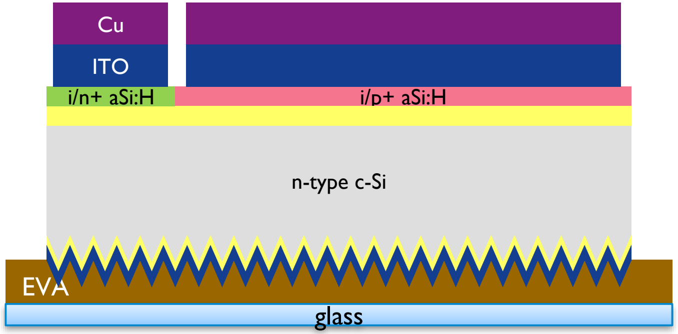


Excellent surface passivation despite presence of silicones

Type	Jsc [mA/cm²]	Voc [mV]	FF [%]	Eta [%]
Bonded (silicones)	40.8	**734**	73.1	**21.7**
Freestanding	41.6	**730**	75.3	**22.9**

Cell area: 3.97cm^2
FZ (200 μm, 3Ω-cm)

The SHJ-IBC cell process was also demonstrated on ultra-thin silicon Fz wafers



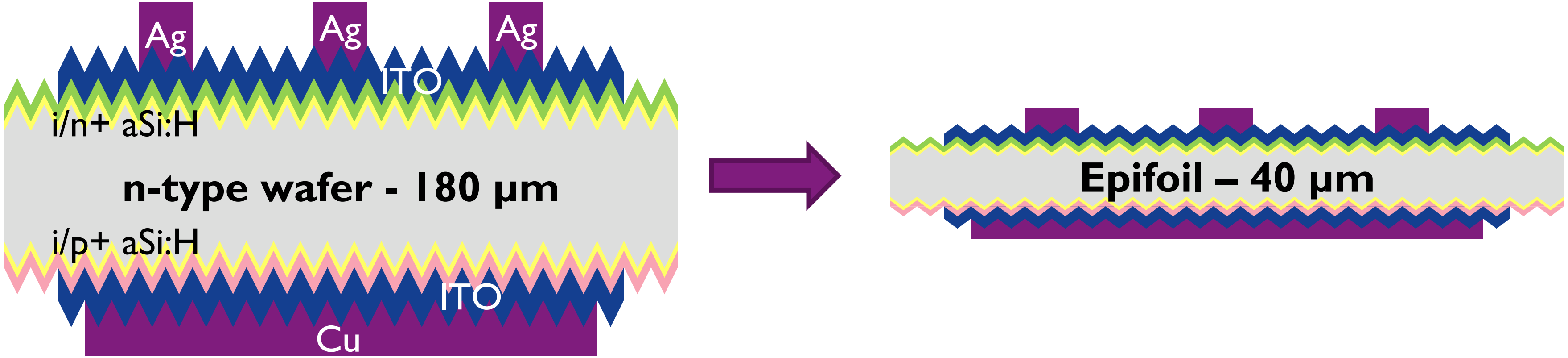
In this experiment, the bonding was done by EVA instead of silicones

Starting thickness [um]	Jsc [mA/cm²]	Voc [mV]	FF [%]	Eta [%]
190	39.9	**724**	71.6	**20.7**
56	38.5	**737**	69.2	**19.6**

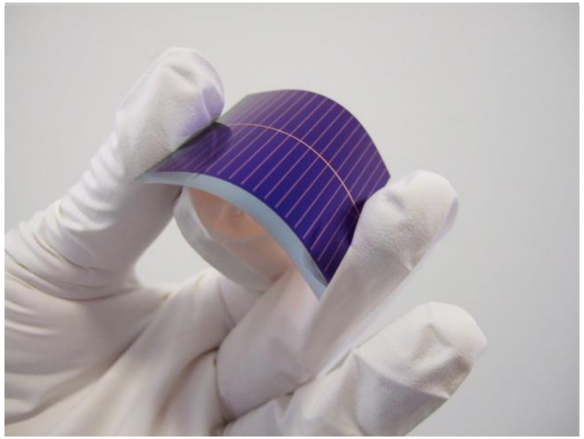
Cell area: 3.97cm^2
FZ wafers of various thickness

Slight decrease in efficiency for thin cells due to lower Jsc and FF

To test the quality of our epitaxial foils at device level we developed a simple freestanding cell process



Type	Jsc [mA/cm^2]	Voc [mV]	FF [%]	Eta [%]
Cz – 180 um	36.5	729	73.3	19.5
Foil – 40 um	34.0	662	68.0	**15.3**
Foil – 40 um	34.7	**715**	40.4	10.0



Cell area: 4 cm^2

CONCLUSIONS

Conclusions

- Porous-silicon based lift-off in combination with epiaxial silicon deposition can produce ultrathin silicon foils

- The resulting foils show minority carrier diffusion lengths which are 25 times as high as the foil thickness

- An SHJ-IBC cell process for silicon bonded to glass using silicones was developed leading to efficiencies close to 22% on regular wafers and to efficiencies close to 20% on ultra-thin wafers

- First cells with a simple cell structure were made from the epitaxial foils leading to efficiencies up to 15.3%

Acknowledgements

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