Silicon heterojunction interdigitated back-contact solar cells bonded to glass with efficiency >21%

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Abstract

Previously, IMEC proposed the i^2-module concept which allows to process silicon heterojunction interdigitated back-contact (SHJ-IBC) cells on thin (<50 μm) Si wafers at module level. This concept includes the bonding of the thin wafer early on to the module cover glass, which delivers mechanical support to the wafer and thus significantly improves the production yield. In this work, we test silicone and EVA bonding agents and prove them to be resistant to all rear side processes, including wet and plasma processes. Moreover, a lift-off process using a sacrificial SiO_x layer has been developed for emitter patterning to replace conventional lithography. The optimized process steps are demonstrated by the fabrication of SHJ-IBC cells on 6-inch 190 μm-thick wafers. Efficiencies up to 22.6% have been achieved on reference freestanding wafers. Excellent V_{oc} of 734 mv and J_{sc} of 40.8 mA/cm^2 lead to an efficiency of 21.7% on silicone-bonded cells, where the high V_{oc} indicates the process compatibility of the bonding agent. The developments that enabled such achievements and the key factors that limit the device performance are discussed in this paper.

Keywords: silicon heterojunction, solar cells, superstrate processing, interdigitated back-contact, amorphous silicon, bonding

1. Introduction

According to the silicon wafer-based photovoltaic roadmap, Si raw material cost accounts for approximately 61% of the current solar cell price [1] and 30% to 40% of the total module cost [2]. Hence, to reduce the Si consumption, fabrication of solar cells on thin (<50 μm) monocrystalline Si wafers, with as little kerf-loss as possible, is being studied by several groups [3-6]. However, such thin wafers are much more mechanically fragile than standard ~180-μm-thick wafers, which are widely used today on production lines [1]. To reduce wafer breakage and achieve high industrial production yield, proper industrial handling techniques of thin wafers are essential [7]. One possible approach is to mechanically support the thin wafer with rigid carriers during wafer transport and cell processing [8-

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12]. This is the case for the integrated interconnect-module (i^2-module) concept, proposed by IMEC [13]. The process starts with thick, highly p+ doped Czochralski wafers. A micron-thick porous Si layer is formed at the top of the wafer by electrochemical porosification. Then, monocrystalline Si foils are epitaxially grown on top of the porosified wafers [14-16]. After epitaxy, the cell processing starts by first processing the front sides of the foils while the foils remain attached to their parent substrates. Then the thin foils are detached and bonded to a module glass superstrate using an adhesive. The rear sides of the foils are now accessible and are processed to finalize the solar cells at the module level. In this way, the thin foils are mechanically supported during most of the processing steps and foil breakage can be significantly reduced, without extra bonding cost.

In the i^2-module concept, certain constraints are imposed to the cell process, particularly due to the bonding. For instance, the bonding agent used for gluing the foil to glass limits the temperature budget of the rear side process to typically 300°C [17]. This motivated us to select low-temperature (<250°C) amorphous silicon (a-Si:H) for rear side passivation and junction formation (e.g. back surface field (BSF), emitter). The potential of a-Si:H/c-Si heterojunction (SHJ) contacts was demonstrated at device level by Panasonic [18] and further substantiated recently by introducing the interdigitated back-contacted (IBC) architecture [19], [20]. Based on the SHJ-IBC technology, the world's record Si solar cell with an efficiency as high as 26.3% was recently reported by Kaneka [21].

In this study, we report the recent progress in the process development of SHJ-IBC solar cells bonded to glass. A lift-off method using a sacrificial SiO_x layer was implemented for emitter patterning to replace the conventional lithography and etching used in the past [22], [23]. In the first part of this paper, these process developments and the resulting cell design and fabrication process are described. Functional cells were achieved on freestanding and bonded n-type float zone (FZ) wafers. Two different bonding adhesives, which are also applied as encapsulants in standard Si solar cell modules, silicone and ethylene vinyl acetate (EVA), were evaluated at cell level. In the second part, the results of these cells are discussed in detail. The factors limiting the cell performance and the main losses of the cells are identified.

2. Experimental details

2.1 Solar cell design and fabrication process

All cells, with an active area of 4 cm^2, were processed on 190-μm thick n-type FZ wafers (6 inch, <100>, 3 Ω.cm). The wafers were first exposed to a H_2SO_4:H_2O_2 (4:1) mixture for 10 min to remove organic contamination remaining on the surface, followed with rinsing in deionized water and a 2 minutes treatment in diluted HF:HCl:H_2O (2:5:93). Spin drying was used to complete the cleaning sequence. A thermal oxide layer (~34 nm) was grown on both sides of the wafers at 975°C for 40 minutes. The front side was exposed to vapor HF to remove the oxide and then the wafers were textured in a 25% tetramethyl ammonium hydroxide (TMAH) based solution at 80°C for 20 min, which resulted

in approximately 10% reflectance @ 700nm. As shown in Fig. 1, a-Si:H and subsequent SiN_x depositions were performed using radio frequency plasma-enhanced chemical vapor deposition (RF-PECVD) for the front passivation and antireflection coating, respectively. Then the wafers were split into two groups depending on the bonding agents. One group was manually bonded to the module glass using silicone encapsulant. We have reported previously that plasma-silicone interaction during a-Si:H deposition has a detrimental impact on passivation quality [24]. For this reason, an Ar plasma treatment was utilized to form a more densely crosslinked layer by local modification of the exposed silicone surface [24]. The other group was manually glued to glass using EVA. Diluted TMAH (1:12 in water, 5 min, 35°C) and $HCl:H_2O_2:H_2O$ solution (1:1:5, 10 min, 20°C) were used for the post-bonding cleaning. Finally, the wafers were dipped in $HF:HCl:H_2O$ (1:1:20, 1min, 20°C). Then, the i/n+ a-Si:H layer (~32 nm) and SiO_x/a-Si:H stack (~630 nm/~26 nm) were deposited using RF-PECVD. This SiO_x layer is a sacrificial mask for the subsequent lift-off process. Photolithography and wet etching were used to define the BSF area. The emitter area was passivated by i/p+ a-Si:H (~16 nm) and patterned by a self-aligned lift-off process, which was carried out in diluted $HF:HCl:H_2O$ (2:1:20). A stack of 120 nm-thick indium-doped tin-oxide (ITO) and 3 μm-thick Cu was deposited followed by lithography patterning to form the rear side metal contact. Thermal annealing at temperatures below 200°C was applied to the finished cells in order to improve the contact behavior. Identical cells were also fabricated on freestanding wafers without bonding to glass to investigate the influence of the presence of boding agents and glass on the cell performance.

Analysis methods include photoluminescence (PL) imaging, quasi steady state photo-conductance (QSSPC), dark and light I-V, spectral response, and Suns-V_{oc} measurements. The I-V characteristics of all cells were measured at different incident light intensities ranging from dark to 1 sun and with an mask implicating a designated illumination area of 3.97 cm^2. The series resistance R_s was determined from the Bowden method [25]. The shunt resistance R_{shunt} and saturation current density J_{02} were determined from a linear fit of the dark I-V curve. The reflectance and external quantum efficiency (EQE) were measured on some of the best cells from each split. The pseudo fill factor (pFF), saturation current density J_{01}, and lifetime of finished cells were extracted from Suns-V_{oc} measurements.

2.2 Rear side patterning approach

The back contact scheme results in additional fabrication complexity mainly due to the presence of interdigitated n- and p-type a-Si:H strips. Although photolithography is widely used for patterning on laboratory scale, it is a costly technique and thus not useable for large-scale production. In addition, the photoresist can introduce contamination during emitter patterning, which may affect both carrier transport and passivation quality at the a-Si:H/c-Si heterointerface [27]. This is particularly true for our bonded cells, as it is difficult to completely remove the photoresist on the bonding agent (e.g. silicone) during resist strip. Possible resist residues may lead to emitter passivation issues during the subsequent i/p+ a-Si:H deposition. To minimize this detrimental impact, a thick SiO_x layer (~630 nm) was

deposited on i/n+ a-Si:H prior to BSF lithography. Such a layer can cap the exposed bonding agent and may reduce the interaction between resist and bonding agent. After BSF patterning, the emitter patterning was performed by a lift-off process using this sacrificial SiO_x layer, which also allowed to avoid one step of photolithography and alignment.

It is widely acknowledged that a sufficiently thick a-Si:H layer is needed to prevent passivation degradation during ITO sputtering [28], [29]. As such, the lift-off has to be a rapid process since the doped a-Si:H layer can be etched in diluted HF:HCl:H_2O (2:1:20), which is the etchant used for the lift-off process. In our case, the etching rates were measured to be approximately 3.1 nm/hour and 1.8 nm/hour for blanket n+ and p+ a-Si:H layers, respectively. Therefore, a quite thick SiO_x sacrificial mask (~630 nm) with a large number of pinholes was used (see Fig. 3a). With the aid of these pinholes, HF based etchants can easily penetrate through the SiO_x layer in spite of the presence of a i/p+ a-Si:H layer on top (see Fig. 3b). In this way, the etching of SiO_x can be realized not only from the sidewalls but also through the pinholes (Fig. 3c), significantly reducing the lift-off duration.

3. Results and discussion

3.1 J_{sc}

Table I shows the best cell parameters from each split, including the cells on freestanding wafers, silicone-bonded and EVA-bonded wafers. For the cells before anneal, a reduction of ΔJ_{sc} = 1.1 mA/cm^2 is observed on silicone bonded wafers with respect to freestanding wafers. This is one of the main factors that limits the cell efficiency on silicone bonded wafers. Fig. 4 compares the EQE spectra for the freestanding cells with the bonded cells. The EQE of freestanding cells, which is overall higher than that of the bonded cells in a wide wavelength range from 400 to 1200 nm, is 7% higher in the range between 500 to 1100 nm as there is no reflectance due to glass at the front side. In the short wavelength range (280 – 400 nm), the EQE of silicone bonded cells is lower due to the increased reflectance and also the absorption losses in glass and silicone [30]. Nevertheless, a high J_{sc} of 41.2 mA/cm^2 has been achieved on silicone bonded cells.

For the cells on EVA bonded wafers, the best J_{sc} is 40.7 mA/cm^2, which is 0.5 mA/cm^2 lower than that of silicone bonded cells. As shown in Fig. 4, this difference is due to the pronounced light absorption loss at short wavelength (280 – 400 nm) caused by the UV blocker contained in EVA in spite of the slightly higher EQE in the wavelength range of 1000 to 1200 nm.

A reduction of J_{sc} is observed after thermal anneal in air at temperatures below 200°C, regardless of the bonding agents. Fig. 5 shows the EQE spectra and reflection of the silicone bonded cells before and after anneal, respectively. We notice that there is a decrease of EQE at long wavelengths (1000 – 1200 nm) after anneal. Such loss is not related to the reflectance, but probably due to the parasitic absorption in the rear side ITO layer. This result confirms the earlier findings [22], where the increased absorbance

of c-Si(n)/a-Si:H/ITO at infrared range was found to be induced by the activation of free carriers during annealing [31].

3.2 V_{oc}

Excellent surface passivation of the Si wafer is required to achieve high V_{oc}. For the bonded wafers, the passivation at the rear side of the wafers is critical because all the wet/dry process steps should be performed in presence of the bonding agent. According to the literature, dramatic passivation degradation of a-Si:H on bonded wafers was observed if no special care was taken [32]. We also reported that the silicone adhesive PV-6100 (Dow Corning) has detrimental impact on passivation quality because of the issue of surface contamination due to its interaction with wet chemicals and plasma [22-24]. Therefore, an alternative silicone and EVA encapsulants were used in this work because these bonding agents were found to be more resistant to different chemicals used in solar cell wet processing as well as to the plasma processes. In addition, an optimized cleaning sequence was applied to bonded wafers prior to deposition of a-Si:H for BSF passivation [22]. As shown in Fig. 6 (a), uniform passivation with effective minority carrier lifetime of 10 ms was achieved on a silicone bonded wafer after i/n+ a-Si:H (BSF) deposition as a result of the process adaptations mentioned above. The subsequently-deposited SiO_x hard mask (~630 nm) also cappped the exposed bonding agents during BSF lithography, wet etching, and i/p+ a-Si:H deposition steps, which further reduced the interaction of chemicals/plasma and bonding agents. The lift-off process was implemented for emitter patterning to replace the previously used lithography [23], [33]. For this, the rear side of the bonded wafer was passivated first with i/n+ a-Si:H and patterned using a milder etchant of dilute TMAH. In this way, the rough and porous wafer surface induced by wet etching of i/p+ a-Si:H using $BHF/HNO_3/H_2O$ solutions is prevented [23]. Consequently, the passivation quality after emitter i/p+ a-Si:H deposition has been significantly improved (see Fig. 6 (b)) compared to previously reported results [23]. An implied V_{oc} (iV_{oc}) was calculated from the excess carrier density generated at 1 sun illumination in open-circuit condition and estimated to be 745 mV using the following equations:

$$iV_{oc} = \frac{kT}{q} ln\left(\frac{\Delta n(\Delta n+N_D)}{{n_i}^2}\right) \tag{1}$$

where k is the Boltzmann constant, T is the temperature, q is the elementary electric charge, Δn is the excess carrier concentration, n_i is the intrinsic carrier concentration and N_D is the doping concentration of the wafer.

The best V_{oc} values of 734 mV and 724 mV obtained for the cells on silicone and EVA bonded wafers after anneal are similar to the V_{oc} of 730 mV obtained after anneal on reference freestanding cells. This suggests that the influence of bonding agents on the surface passivation has been minimized. However, such V_{oc} is still lower than the calculated iV_{oc} of 745 mV, which indicates passivation degradation during

the metallization steps (i.e. ITO sputtering, Cu deposition). It is also worth to notice that the V_{oc} values of freestanding cells were reduced after anneal while the V_{oc} values of bonded cells were increased. In order to explain this difference, the evolution of the effective minority carrier lifetimes of device wafers are shown in Fig. 7. The overall lower lifetimes of finished freestanding and bonded cells with respect to those of wafers after lift-off confirm the losses in passivation during metallization steps. For the bonded cells, the effective lifetime at low injection level slightly decreases whereas the effective lifetime at high injection level (Δn >5×10^{15} cm^{-3}) increases after anneal. However, for the freestanding cells, the lifetime reduces more dramatically at low injection level. Contrary to the improved lifetime of bonded cells after anneal, no apparent improvement of lifetime at high injection level is observed. Such findings may explain the different anneal behaviors since V_{oc} is mainly affected by Auger recombination at high injection level.

3.3 Fill factor

The efficiencies of all cells are mainly limited by moderate FF values (≤70.4%). Thermal anneals yield a significant improvement of FF regardless of bonding agent. A breakdown analysis was done to investigate the FF loss mechanisms [34], [35]. The difference between measured FF and ideal FF (FF_0) indicates the FF loss of a solar cell related to series resistance R_s, shunt resistance R_{shunt}, as well as recombination currents J_{02}. FF_0 is calculated according to [36] as:

$$FF_0 = \frac{v_{oc} - ln(v_{oc}+0.72)}{V_{oc}+1}, where\ v_{oc} = \frac{V_{oc}}{kT} \quad (2)$$

where k is the Boltzmann constant and T is the temperature. The absolute FF losses arising from R_s (ΔFF_{Rs}) and R_{shunt} (ΔFF_{Rshunt}) are estimated by Equation (3) and (4), respectively, as described below:

$$\Delta FF_{R_s} = \frac{J_{mpp}^2 R_s}{V_{oc} J_{sc}} \quad (3)$$

$$\Delta FF_{R_{shunt}} = \frac{\left(V_{mpp} + J_{mpp} R_s\right)^2}{R_{shunt} V_{oc} J_{sc}} \quad (4)$$

where current density J_{mpp} and voltage V_{mpp} at maximum power point are extracted from the light I-V measurements. Equation (5) specifies the FF loss resulting from recombination currents J_{02}.

$$\Delta FF_{J_{02}} = FF_0 - pFF - \Delta FF_{R_{shunt}} \quad (5)$$

where pFF is the series resistance-free fill factor taken from suns-V_{oc} measurements. The absolute FF loss of a freestanding cell before and after anneal is calculated and illustrated in Fig. 8. The FF measured

from light I-V measurements is primarily affected by R_s. Thermal annealing leads to a drastic decrease of R_s from 2.8 Ω.cm^2 to 1.6 Ω.cm^2 and thus corresponding ΔFF_{Rs} reduces from 13.5% to 7.9%. ΔFF_{Rshunt} is approximate 0.6% and remains identical after anneal. As we discussed previously, an anneal also results in surface passivation degradation (see Fig.7 left). So the FF loss due to recombination currents J_{02} slightly increases from 0.4% to 1.8%. Hence, the combination of these factors leads to the improvement of FF after thermal anneal. A similar improvement of FF mainly due to the decrease of R_s was also observed on bonded cells.

4. Conclusion

An integration process for large scale module-level processing of SHJ-IBC cells is presented. Efficiencies of 22.6% and 21.7% were achieved on freestanding and silicone bonded wafers, respectively, which shows the high potential of the i^2-module concept. In terms of J_{sc}, the silicone encapsulant is found to be better than EVA due to much less parasitic light absorption losses at short wavelengths. The high V_{oc} values of 734 mV and 724 mV obtained on silicone and EVA bonded cells reveal that the impact of bonding agents on surface passivation is minimal. The current device efficiencies are mainly limited by low fill factor values. Investigation of the FF loss mechanisms indicates series resistance as the major limiting factor. Thermal anneals performed on the finished cells yield a significant improvement of the fill factor by reducing the series resistance**.**

Acknowledgement

The authors would like to thank the financial support of imec's industrial affiliation program for Si-PV. This work was also partially funded by Kuwait Foundation for the Advancement of Sciences under project code: P115-15EE-01. The research has received funding from the European Union's Seventh Programme for research, technological development and demonstration under grant agreements n° 609788 (Cheetah), and also funding from the European Union's Horizon 2020 research and innovation programme under the Marie Sklodowska-Curie grant agreement No 657270. The authors gratefully acknowledge Joachim John for the spectral response measurements and Yiming Yang for the SEM measurements.

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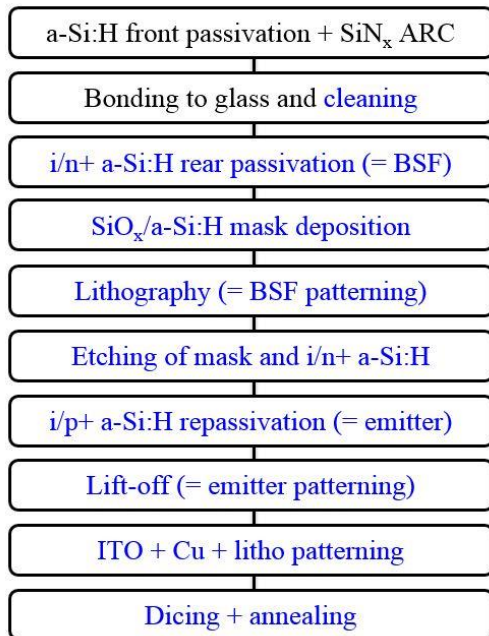

Fig. 1. Integration process flow of SHJ-IBC cells on bonded wafers used in this work [26]. All the rear side process steps (in blue text) are performed in presence of bonding agent.

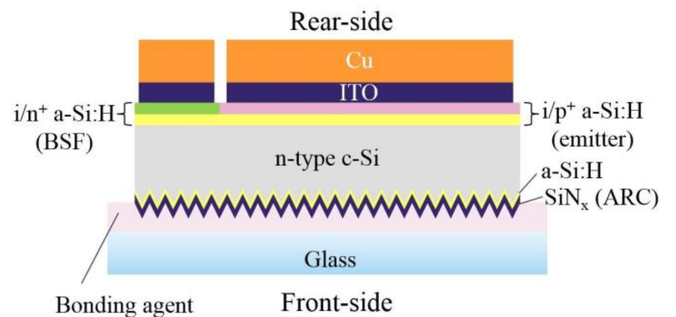

Fig.2. Schematic of the bonded SHJ-IBC solar cell architecture (not drawn to scale).

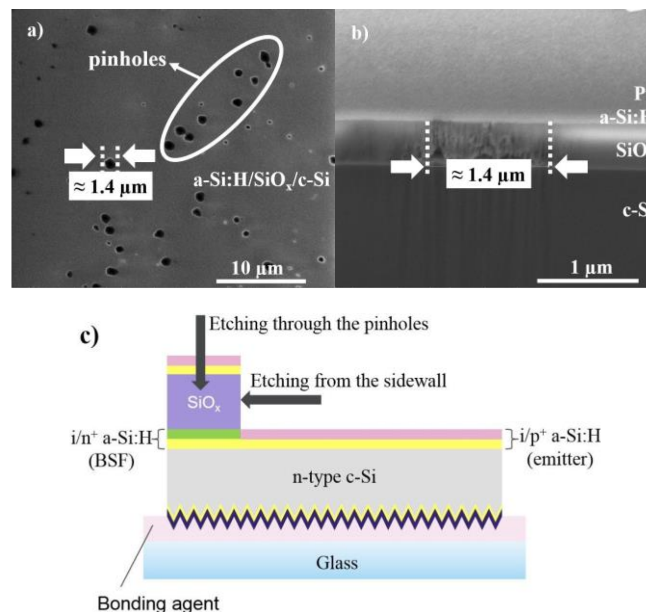

Fig. 3. a) Top-view and b) cross-section SEM micrographs of the sample a-Si:H/SiO_x/c-Si after 2-min treatment in HF:HCl:H_2O (1:1:20). Penetration of the HF based etchant through pinholes is possible in spite of the a-Si:H layer on top of SiO_x. Fig.3. c) illustrates the scheme of the device after emitter i/p+ a-Si:H passivation, which is followed by lift-off process.

TABLE I

PARAMTERS OF BEST CELLS ON FREESTANDING AND BONDED WAFERS

Bonding	ANNEAL	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF (%)	η (%)
freestanding	before	42.3	735	69.7	21.5
	after	41.8	730	74.8	22.6
silicone	before	41.2	727	70.4	21.0
	after	40.8	734	73.1	21.7
EVA	before	40.7	718	68.6	20.0
	after	39.9	724	71.6	20.7

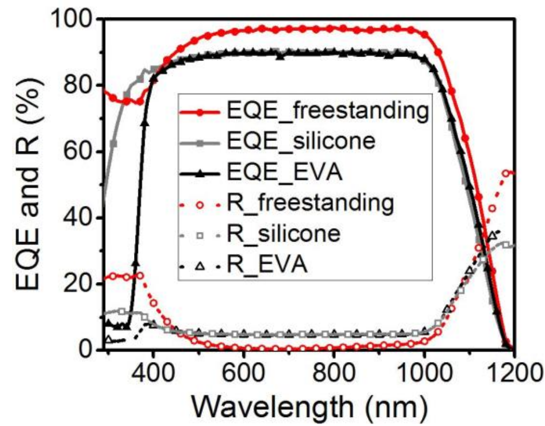

Fig. 4. Comparison of EQE spectra (lines and closed symbols) and reflection (dots and open symbols) of cells on a freestanding wafer and on bonded wafers.

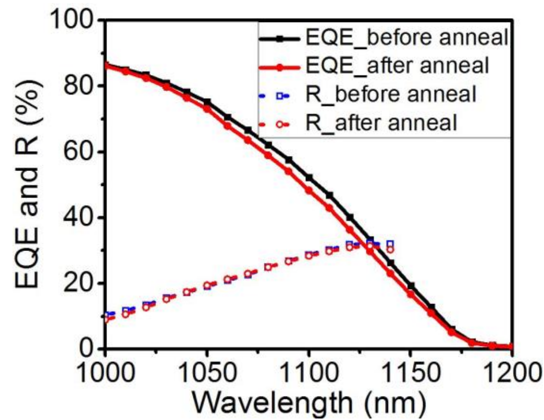

Fig. 5. EQE spectra (lines and closed symbols) and reflection (dots and open symbols) of a cell on a silicon bonded wafer before and after anneal.

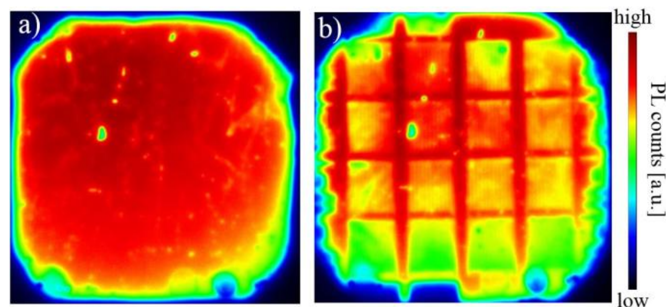

Fig .6. Uncalibrated PL images of silicone bonded device wafers. The measurements are taken after (a) i/n+ a-Si:H (BSF) passivation; (b) i/p+ a-Si:H (emitter) passivation.

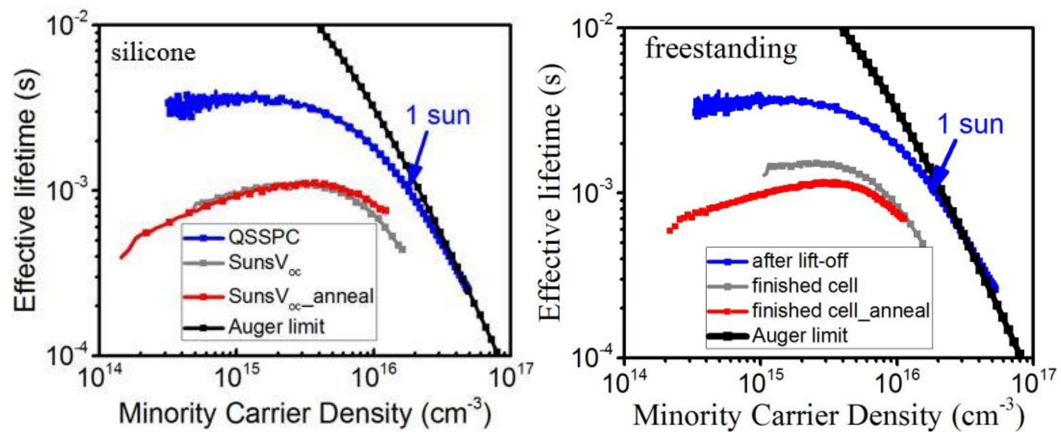

Fig 7 Measured injection dependent effective minority carrier lifetimes using QSSPC for the silicone bonded wafer (left) and freestanding wafer (right) after lift-off (all intrinsic and doped a-Si:H layers are present). The lifetimes of the finished device before and after anneal were extracted from Suns-V_{oc} measurements.

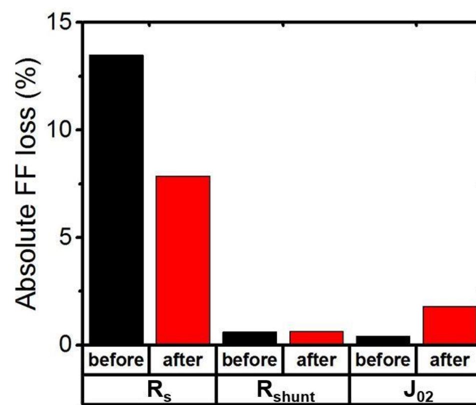

Fig. 8. Calculated absolute FF loss of a freestanding cell before and after anneal. The loss mechanisms via series resistance, shunt resistance, and J_{02} recombination are included.