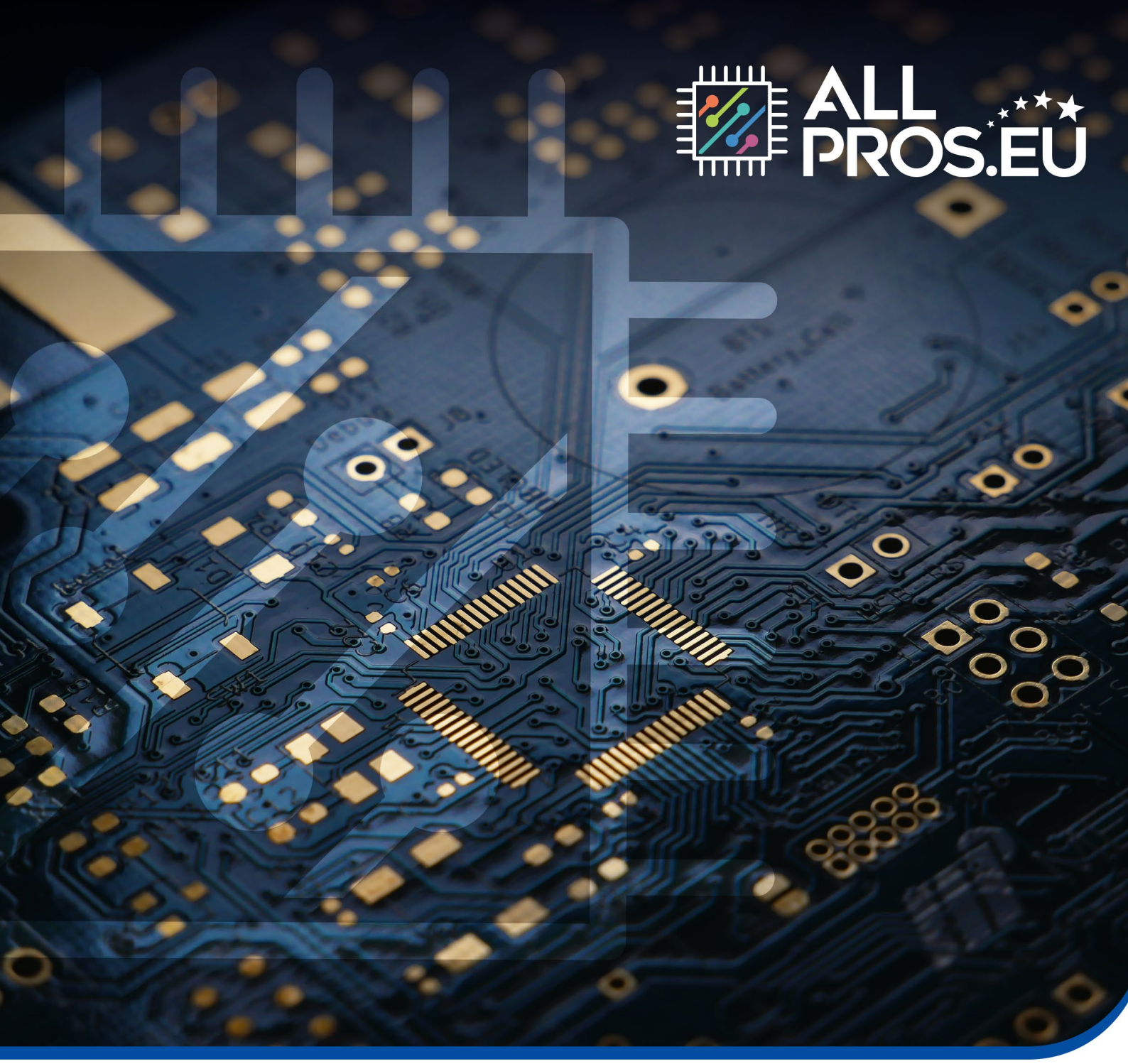

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POLICY BRIEF

The European Chip Ecosystem and Open Source Silicon

Funded by the European Union

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ABSTRACT

This policy brief introduces the open source silicon approach in terms of its importance for semiconductor research and development as well as its industrial integration in Europe. The background of this approach and its relations to the semiconductor value chain are investigated in an overview of the open source silicon landscape. The strengths and weaknesses of open source silicon and their implications for Europe's strategic opportunities are consequently examined: a SWOT analysis will form the basis for concrete policy recommendations on the potential of open source silicon to strengthen Europe's semiconductor ecosystem. Here, a focus lies on research and development as well as on start-ups and SMEs in Europe.

TERMINOLOGY

AI	Artificial Intelligence	**ISA**	Instruction Set Architecture
Alliance	European Alliance on Processors and Semiconductor Technologies	**KPI**	Key Performance Indicator
ALLPROS.eu	Secretariat for the European Alliance on Processors and Semiconductor Technologies CSA project	**LE**	Large Enterprises
CSA	Coordination and Support Action	**PDK**	Process Design Kit
DEP	Digital Europe Programme	**R&D**	Research and Development
EC	European Commission	**R&I**	Research and Innovation
EDA	Electronic Design Automation	**SME**	Small and Medium-sized Enterprise
EU	European Union	**SWOT**	Analysis considering strengths, weaknesses, opportunities and threats of a research subject
FET	Future Emerging Technologies	**TWGs**	Thematic Working Groups
HE	Horizon Europe	**OSH**	Open Source Hardware
HPC	High Performance Computing	**OSS**	Open Source Software
IPCEI	Important Project of Common European Interest	**WP**	Work Package
IC	Integrated Circuit ("Chip")		

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EXECUTIVE SUMMARY

The fundamental importance of semiconductor technologies across various industries, including AI-driven sectors, underscores the need for Europe to reduce its strategic dependencies in the chip sector. In response, there is a growing focus on the open source approach, particularly through open source silicon, to enhance European sovereignty and innovation in semiconductor research and development. This policy brief explores the significance of open source silicon in semiconductor R&D and its integration within the European industrial landscape. It delves into the background of this approach, its relevance within the semiconductor value chain, and its potential to strengthen Europe's semiconductor industry. The brief employs a SWOT analysis to assess the strengths and weaknesses of open source silicon and its implications for Europe. Based on a combination of targeted research, expert interviews, and insights from ALLPROS.eu workshops and webinars, this brief offers valuable insights into how the open source silicon approach can contribute to addressing Europe's semiconductor challenges and fostering innovation.

INTRODUCTION

Europe's semiconductor or "chip" ecosystem faced geoeconomic crises and geopolitical tensions in recent years such as the disruptions of supply chains in the wake of the COVID-19 pandemic and increased trade disputes.[1] It is semiconductor technologies that provide the foundation for sustaining and growing many industries: not only digital and directly dependent industries such as the healthcare or automotive industry, but also in the future a broader range of allied sectors. Because the role of artificial intelligence (AI) is becoming increasingly critical across sectors, strategic dependencies in the area of semiconductors, which are fundamental to AI technologies, is in turn an increasing risk for Europe. As a result of this fundamental role combined with recent geopolitical events, it has become imperative for the European Union to reduce strategic dependencies in the chip sector.

In a similar way that the open source approach has strengthened the software industry, there is now a focus on this approach for reinforcing the hardware industry in an international context, in particular in the area of semiconductor research and development: through open source silicon. By this rationale, open source hardware is highly relevant to increasing European sovereignty in the field of processors and semiconductor technologies: it can strengthen domestic innovative semiconductor capacities bottom-up and mitigate dependencies on supplying regions.[2] In particular, research and academia as well as smaller companies benefit from the accessibility, flexibility, and interoperability that open source silicon brings to this highly specialised and complex ecosystem. But since the approach is still nascent at its core, start-ups and SMEs need to be supported by EC actions in terms of legal certainty and dedicated R&D incentives when it comes to scaling up innovation.

This policy brief aims to explain the open source silicon approach in terms of its importance for semiconductor research and development as well as its industrial integration in Europe. It will examine the background of this approach and how it relates to the semiconductor value chain, as well as its weaknesses and strengths and their consequences for Europe: After an overview of the open source silicon landscape, a SWOT analysis will be presented to identify how the approach of open source silicon can be leveraged to strengthen the European semiconductor industry. The knowledge production process at the basis of this brief involved targeted research, expert interviews and insights gained from ALLPROS.eu workshops and webinars.

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1. E.g., see: Tan (2023). **China slaps export curbs on chipmaking metals in tech war warning tu U.S., Europe**. CNBC. For the respective geopolitical relevance see also: Webb (2023). **In a World Awash in Data, Geopolitics is All About Chips**. Bloomberg.
2. EC Working Group on OSH and OSS (2022). **Recommendations and roadmap for European sovereignty on open source hardware, software and RISC-V Technologies**.

BACKGROUND

Various policies for fostering sovereignty in the digital sectors seem to be in contradiction with each other when it comes to their stance on open technologies. On the one hand, there are policies that concentrate on the race for closed innovation through patenting strategies; on the other hand, there is an approach that adheres to the rationale of technological openness. However, the history of digitalisation in the European Union has, on closer examination, outgrown this dichotomy, which spurs and expands global competition, enabling it to create a level playing field for European actors. In recent decades, open technologies have introduced competitive advantages to both open source as well as proprietary products, which in turn has led to greater economic capacity for industrial adoption.[3]

The rising role of open source hardware

Open source software (OSS) has played a significant role in the European and international private and public sectors in the past two decades. The implementation of openness principles in competitive digital markets is now slowly taking off in the open source hardware (OSH) space. This is particularly visible in the field of semiconductors and processor technologies: this complex environment has been significantly enhanced and stimulated by open source silicon. Most notably, the prominent and open RISC-V standard has generated a large open source trend in the semiconductor domain. Numerous start-ups basing their innovative efforts to a large extent on these open chip architectures have emerged in Europe and around the world.[4] Open source approaches offer new opportunities for the highly interdependent stakeholders within the semiconductor ecosystem.

In light of the European Chips Act and further legislative acts that seek to mitigate certain strategic dependencies in critical digital industries, it is important to be ahead of this open source silicon curve that is embraced around the globe. Leveraging this open innovation is instrumental to expanding and strengthening the regional ecosystem and boosting Europe's industry in areas where its potential is not yet being realised, such as chip design capacities. Recognising this opportunity, various initiatives on the EU level are generating roadmaps, analyses, reports and recommendations that jointly aim to develop a consistent strategy to integrate heterogeneous practices within the open source silicon landscape in Europe.[5] This strategic use of technological openness, combined with Europe's inventive power, can help overcome disadvantages that have already materialised in the chips sector. This open approach is, thus, strategically relevant when it comes to strengthening the sovereignty of Europe's semiconductor industry and to mitigating dependencies.

3. Blind et al. (2021). **The impact of Open Source Software and Hardware on technological independence, competitiveness and innovation in the EU economy**. Final Study Report.
4. See: EE Times (2023). **Silicon 100: Startups Worth Watching in 2023**, but also start-up **members within the RISC-V foundation**.
5. For instance, the HE initiated TRISTAN consortium is working on unified application strategies for European semiconductor technologies on the basis of RISC-V, see: Horizon Europe (2023). **Together for RISc-V Technology and ApplicatioNs**.

A focus on open source silicon

In the chip sector, the term "open source silicon"[6] is used in a colloquial manner to refer to open source, i.e. disclosed and publicly accessible hardware designs and components in integrated circuit (IC) design processes by the means of software.[7] This means that while open source silicon is understood as OSH, it still involves software (see Figure 1).[8] Furthermore, it can refer to the openness of semiconductor manufacturing requirements and hardware components necessary for chip integration in general. "Open" here refers to the freedom to access, use, modify, and distribute these designs or technologies. The term can also include the absence of royalty fees or licensing fees. Synonyms exist, including "free hardware (design)"[9] or "free and open source silicon"[10], indicating the above-mentioned freedoms. To create an inclusive understanding of strategies to bridge the gap between academia and industry, open source silicon is understood more broadly in this document, so that absence from royalty or licensing fees may or may not be designated.

While OSS has already become ubiquitous, OSH's increased popularity and industrial relevance is a more recent phenomenon. Within OSH, open source silicon is growing rapidly, especially since the release of RISC-V in 2015 – a free and open instruction set architecture (ISA) standard that has fueled innovation in the field.[11] Additionally, OSS innovation and trends are spilling over into the open source silicon field, as advances in OSS not only inspire software and hardware engineers working in chip design, but are also instrumental to the various pieces of software involved in chip design. This new wave of innovation led to the emergence of start-ups and technologies worldwide, including free and open source as well as proprietary cores. The integration of RISC-V and related open solutions is often seen as a catalyst for innovation.

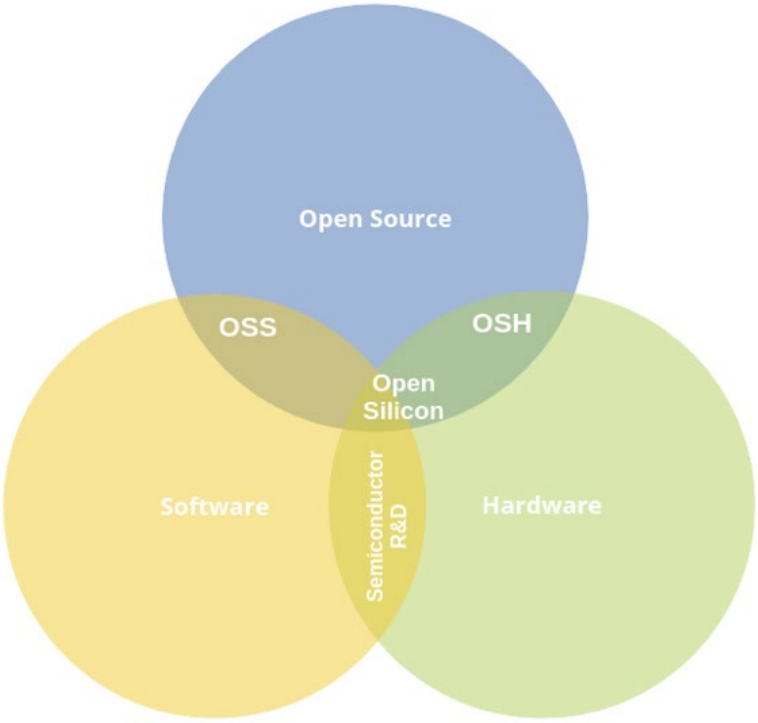

Figure 1 - Open source silicon within software and hardware domains

6. Often shortened to "open silicon". The term is to be distinguished from an US-based chip design company Open-Silicon, now part of SiFive.
7. This does not mean that all semiconductor technologies and components that are referred to with "open source silicon" are actually primarily based on the material of silicon. Other materials could also be used, such as gallium nitride (GaN) and silicon carbide (SiC).
8. OSH or sometimes also called OSHW is **defined by the Open Source Hardware Association** (although the organisation does not focus on silicon applications). A prominent OSH licence, CERN OHL, is provided by CERN, see: CERN Knowledge Transfer (2023). **CERN Open Hardware Licence**. It comes with a specific applicability for printed circuit boards (PCBs).
9. Stallman (n.d.) **Free Hardware and Free Hardware Designs**, Free Software Foundation.
10. See, e.g., **defined by the FOSSi foundation**.
11. Semico Research (2022). **Analyzing the RISC-V CPU Market for SIP, SoCs, AI and Design Starts**.

THE OPEN SOURCE SILICON LANDSCAPE

As already mentioned, RISC-V is a prominent constituent of open source silicon that is now making its way into the mainstream of innovation in microelectronics. However, it is meanwhile situated within, and interdependent on, a broader ecosystem that can be called the open source silicon landscape. Below is a brief overview of its main components and constituents.

Open source silicon's position in the semiconductor value chain

The general semiconductor value chain includes various production steps and inputs. Briefly, these comprise chip design, manufacturing[12] and ATP (assembly, test, and packaging)[13-14]. Chip designers rely on a multitude of R&D processes and intellectual property (IP) blocks, while chip manufacturers depend on a variety of specialised equipment, materials, chemicals, and other resources. The majority of these production steps, processes and inputs is highly specific and high-cost, which generates high barriers to entry for new entrants. The investment needed in semiconductor R&D, for example, is very high compared to other sectors.[15] Although Europe is particularly strong in inputs such as equipment and chemicals, as well as innovative research conducted in leading Research and Technology Organisations (RTOs), strategic weaknesses are located in the production processes itself, including chip design.[16]

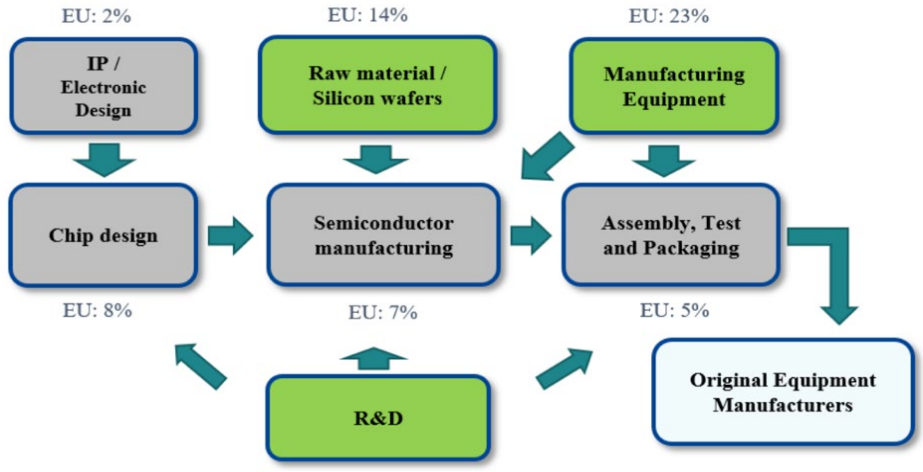

Figure 2 - Semiconductor supply chain: EU global market shares of relevant segments (source: European Chips Act)[17]

12. Manufacturing can either be conducted in-house by the design entity of the chip, as in the case of Integrated Device Manufacturers (IDMs) or in a fab. A "fab" is a single fabrication plant of a company specialised in the fabrication of chips, i.e., a foundry. In contrast, a company that specialises in chip design and outsources all manufacturing processes is called "fabless".
13. ATP can either be conducted in-house by IDMs, in-house by foundries, or by a specialised company. This company model is called Outsourced Semiconductor Assembly and Test (OSAT).
14. For an introduction to the semiconductor value chain, see: Baisakova & Kleinhans (2020). **The Global Semiconductor Value Chain: A Technology Primer for Policy Makers**. Policy Brief. SNV Berlin.
15. In 2020, the semiconductor industry allocated about 15 percent of its revenue on R&D. For an in-depth understanding of the semiconductor value chain's characteristics, see: Hess & Kleinhans (2021). **Understanding the global chip shortages**. Policy Brief. SNV Berlin.
16. For a thorough analysis, see: Kleinhans (2021). **The lack of semiconductor manufacturing in Europe**. Policy Brief. SNV Berlin.
17. EC (2022). **European Chips Act: Communication, Regulation, Joint Undertaking and Recommendation**.

Within the value chain, the open source silicon landscape essentially encompasses the field of chip design. Different architectures, standards, IP cores, and pieces of software are needed to deliver a valid design.

Electronic design automation (EDA) tools are used for simulating the behaviour of the intended chip architecture and design on the basis of its representation in a hardware description language, such as Verilog. These same EDA tools are also instrumental for designing the individual chip, and for verifying the logical and physical composition of the chip.

After the completion of these steps, the design is transferred to production adjusted to a specialised blueprint, a so-called process design kit (PDK). The PDK is provided by the manufacturing entity i.e., foundry and contains essential design rules, data, and libraries. The overall chip design flow is indicated in Figure 3.

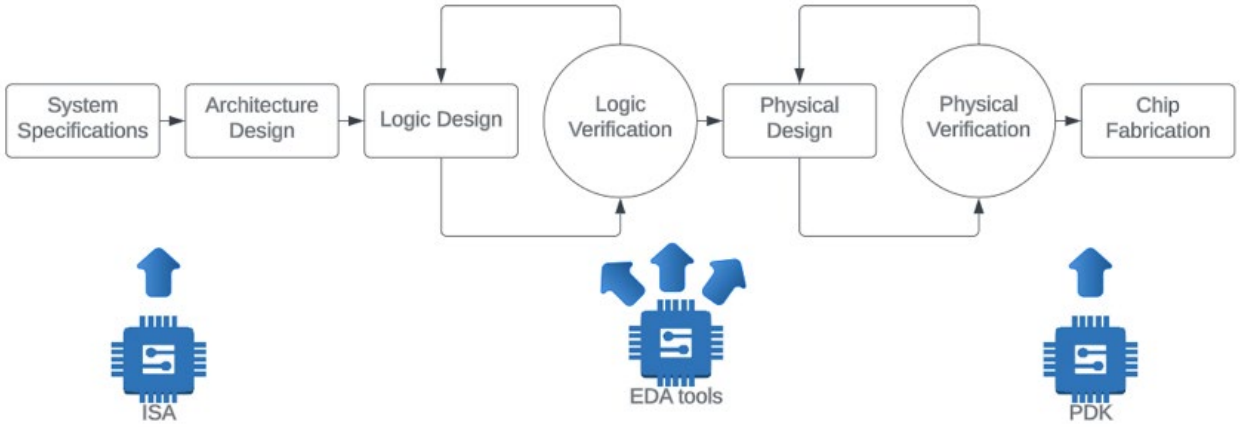

Figure 3 - The chip design process steps and tools in the design of processors[18]

After this brief overview of the production steps of the semiconductor value chain that are relevant to the approach of open source silicon, key components of the open source silicon landscape are outlined in the following.[19]

Here, their degree of maturity of open source solutions, their profitability, and relevance for education and skills, is addressed.

18. The presentation of the process design steps follows the detailed overview of Any Silicon (n.d.): **Chip Design**.

19. The open source silicon landscape's components follow the publications of the PULP project at ETH Zurich, in particular: Gürkaynak (2023). **Special session on RISC-V and OSH. Presentation**.

Main components of the open source silicon landscape

Open Instruction Set Architectures (ISAs)

- Maturity of open source solutions: **high**
- Profitability of open source solutions: **high**
- Relevance for education and skills: **high**

The RISC-V ISA, which is giving open source silicon development a big boost at the moment, was developed at the University of California in 2010 and made accessible to the OS community and the public since 2015. Its popularity has been increasing and its community growing ever since. It is based on the principle of a reduced instruction set computer (RISC), striving for simplicity, modularity, and extensibility. The standard is accessible licence- and royalty-free and allows for the design, integration, and modification of RISC-V-based processors.[20] The diverse ecosystem emerging from it unites engineers from various backgrounds, both hardware and software, that customise and advance applications for different fields, including low-power processing and high-performance computing (HPC). Large enterprises as well as leading research institutions actively support the ecosystem.[21] Universities are adopting this ISA for educational purposes, allowing for up-to-date and highly applied research scenarios that help to attract talent.[22] Innovation that is based on the RISC-V ISA can be both OS and proprietary, since the standard is open to all and does not exclude commercialising.

Open Electronic Design Automation (EDA) tools

- Maturity of open source solutions: **low**
- Profitability of open source solutions: **low-moderate**
- Relevance for education and skills: **high**

Open EDA tools refer to electronic design automation tools that are open source and used for chip design, simulation, layout, and verification. They offer advantages for chip designers such as the educational support from the OS community and low barriers to entry for innovation due to their affordability. Available at no or low cost, this difference is significant given that proprietary EDA tools' licensing costs are often five to ten times the general IT infrastructure costs for smaller companies, and are also substantial even for large enterprises.[23] Most open EDA tools are still only at the level of modelling design rather than physical design.[24] For this purpose, specific hardware description languages (HDLs) are used that enable a representation of the future chip. Prominent examples of open EDA tools include OpenROAD and Verilator. Many EDA processes covered in the design step such as processes done with simulators are still dependent on proprietary software that is provided by an oligopoly of three companies (Synopsys, Cadence, and Mentor/Siemens). European incentives for open innovation in the EDA domain are therefore advocated for in the community of semiconductor R&D.[25]

20. While the RISC-V ISA itself is only a design architecture open to be implemented in hardware, the actual implementations integrating it can be open or closed. Since the standard is foundational to various open source silicon components and, when it comes to the concept of open source silicon, broadly discussed at the moment it was given a stand-alone category here.
21. See, e.g.: Infineon (2023). **Leading Semiconductor Industry Players Join Forces to Accelerate RISC-V**.
22. RISC-V International (n.d.). **RISC-V technical specifications**.
23. Gopal et al. (2022). **Economics of EDA on AWS: License Cost Optimization**. Aws blog.
24. This level is referred to as the register transfer level (RTL).
25. An impression of this community feedback was received in the semi-structured interview process on the basis of this policy brief. For an overview of open EDA tools for different purposes, see: Any Silicon (n.d.). **The Ultimate Guide to Open Source EDA Tools**, and Payne (2020). **EDA Open Source and Free Tools Wiki**. SemiWiki.

Open Process Design Kits (PDKs)

- Maturity of open source solutions: **low**
- Profitability of open source solutions: **low**
- Relevance for education and skills: **high**

With the trend of chip design being opened up more in general, the number of initiatives where chip designers and fabs are working together to open up PDKs is increasing too: while the maturity of open source solutions is still low, a subtle trend toward the opening of PDKs can be observed. In an international and industrial context, the releases of the GlobalFoundries PDKs are historically influential. Google recently started a program around open PDKs in a joint initiative with Efabless, SkyWater, and GlobalFoundries that fosters the design process of chips and covers manufacturing costs for students and OS developers.[26]

It was received positively by OSH developers, and other stakeholders of the European semiconductor ecosystem. For instance, Antmicro actively participated in the program. When it comes to R&D initiatives in Europe, the Leibniz Institute for High Performance Microelectronics (IHP) recently opened one of its PDKs which will be integrated in research and education modules. The hope is that the release will inspire similar initiatives aiming at research or educational impact.[27]

Open Intellectual Property blocks

- Maturity of open source solutions: **low**
- Profitability of open source solutions: **low-moderate**
- Relevance for education and skills: **high**

An existing bottleneck to use OSH assets for innovation in European research and development are IP blocks as required inputs. These can be soft IP (initial design steps and requirements such as code, simulation models, tools) or hard IP (subsequent design steps and requirements such as masks or analogue blocks). The majority of open source silicon is situated in the domain of soft IP at the moment. The trend of specialisation in semiconductor innovation increases the amount and complexity of IP blocks needed for designing chips in various integrations such as chiplets. For instance, these blocks are necessary for the system's peripherals but can also be relevant for specific processor applications.

Not only are IP blocks traditionally closed but also dependent on closed tools and PDKs. This creates high licensing costs as well as dependencies on suppliers and foundries' non-disclosure agreements (NDAs) that can be significant access barriers for small companies and research projects interested in chip design. The technical functions of the IP in question are non-transparent, creating difficulties for engineers when it comes to the verification of processes closely related to the IP.[28] Activities targeted at the improvement of interoperability, accessibility, modularity, and reusability of IP blocks are therefore already encouraged by researchers and developers, including the EC-initiated thematic working group on OSS, OSH and RISC-V.[29] A starting point to tackle the bottleneck of closed hard IP would be more open EDA tools as well as the open access to the foundries' PDKs.

By and large, the open source silicon approach constitutes a key enabler in chip design that is reinforced by an active R&D community. The advantages that open source brings in the semiconductor ecosystem when it comes to talent and competition, education, and mitigation of costly dependencies are already recognised by policy and funding in Europe. However, at the European level, there is also a need for strategic incentives for open innovation in this domain to compensate for existing bottlenecks and increase interoperability in the landscape. The most critical bottlenecks reported by open source silicon experts during the knowledge acquisition process in interviews and webinars were the degrees of openness of EDA tools and PDKs that constitute further difficulties for small entities.

26. This is called the OpenMPW shuttle program. For more information, see: Google (2022). **GlobalFoundries joins Google's open source silicon initiative**. Google OS Blog.
27. See the release of IHP's PDK: IHP (2022). **IHP Open Source PDK**.
28. Bailey (2023). **IP Becoming More Complex, More Costly**. Semiconductor Engineering.
29. See: EC Working Group on OSH and OSS (2022). **Recommendations and roadmap for European sovereignty on open source hardware, software and RISC-V Technologies**. A detailed list on open IPs required for System on Chip (SoC) designs is given on pp. 42f.

STRATEGIC OPEN INNOVATION AND GEOPOLITICS

In recent years, geopolitics has led to complex international scenarios directed at the economic decoupling of regions.[30] This included siloed research and technology developments accompanied by international trade policy and foreign policy interventions. Intense trade conflicts exist in particular between China and the US.[31] However, the EU is also acknowledging China as a systemic rival whose "clear goal is a systemic change of the international order with China at its centre".[32]

Hence, the EU is increasingly involved in these trade disputes, e.g., through restricting the supply of equipment to China,[33] to which China has responded with export restrictions on materials which are essential for the EU's semiconductor industry.[34] Overall, these geopolitical developments led to a paradigmatic shift in the international collaboration within the semiconductor value chain.

The Chinese government highlighted ambitious goals concerning the domestic semiconductor industry in its Made in China 2025 strategy[35] concerning an independent domestic supply chain, as well as governmental incentives in its "State Council Notice on the Publication of Certain Policies to Promote the High-Quality Development of the Integrated Circuit Industry and the Software Industry in the New Period".[36] These strategies are backed by a governmental investment plan established in 2014, incorporated in the China Integrated Circuit Industry Investment Fund ("the Big Fund").

It raised nearly fifty billion USD to serve investments in the domestic semiconductor sector and contributed to the success of the state's strongest foundry SMIC.[37] Although these strategies have been successful when it comes to increasing the share of global sales, the industry is still very dependent on the import of tools and equipment from the US and Europe. The Chinese foundry SMIC is not able to keep up with the leading edge in manufacturing and was affected by several U.S. export controls.[38] However, China is still investing strongly in early innovation of its domestic semiconductor ecosystem, especially in the chip design sector which is thought to enable high revenue.[39]

While the Quadrilateral Security Dialogue's (Quad) trade share with China has increased,[40] long-standing trade partnerships and cooperations between international regions and geographically-concentrated industries have been eroded in strategic sectors such as the chip industry. In response to China's quests for technological dominance in the chip sector and its unfair behaviour in international competition, new geoeconomic alliances and agreements have been formed, especially between the United States, India, Japan, and Europe.[41]

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30. World Economic Forum (2019). **The rise of techno-nationalism - and the paradox at its core**.
31. Robinson (2023). **US mulls retaliation for China blacklisting Micron without evidence of security threat**. The Register.
32. EC (2023). **Speech by President von der Leyen on EU-China relations to the Mercator Institute for China Studies and the European Policy Centre**.
33. Haeck (2023). **Dutch slap new restrictions on chips exports to China**. Politico.
34. Aarup et al. (2023). **China's threat on mineral exports knocks EU off balance**. Politico.
35. PRC State Council (2015); Etcetera Language Group, Inc. (2022). **Notice of the State Council on the Publication of "Made in China 2025"**. CSET.
36. PRC State Council (2020); Etcetera Language Group, Inc. (2020). **State Council Notice on the Publication of Certain Policies to Promote the High Quality Development of the Integrated Circuit Industry and the Software Industry in the New Period**. CSET.
37. Liu & White (2022). **China's Big Fund corruption probe casts shadow over chip sector**. Financial Times. As reported in the article, the fund was under state investigation for corruption.
38. Lee & Kleinhans (2021). **Mapping China's semiconductor ecosystem in a global context**. SNV Berlin.
39. Hess et al. (2023). **Who is funding the chips of the future?** SNV Berlin.
40. Economist Intelligence (2023). **Conflict over Taiwan: assessing exposure in Asia**. EIU Report.
41. See, e.g., the **EU-US Trade and Technology Council (TTC)** as well as the **EU-India TTC**. India and the US are **moving closer together**, and Japan and EU recently declared new strategic cooperations in semiconductor areas: Nussey (2023). **EU, Japan to deepen chip cooperation, Breton says**. Reuters.

Internationally, regions that are leading in the international semiconductor ecosystem foster government-backed investment and policy strategies on this issue that has been set against a backdrop of increasing tensions due to supply shortages and the trade conflicts. These strategies focus on providing subsidies of several tens of billions USD to increase national or regional sovereignty and competitiveness.[42] While the initiatives include standardisation- and patent-oriented strategies, they also promote strategic open innovation related to the semiconductor ecosystem, especially with respect to R&D initiatives.

The growing importance of open source silicon is recognised by the regions highly active in semiconductor R&D. China was a relatively late adopter of open source, but has since recognised the relevance of open source to its technological sovereignty and is making strong strategic use of it. When it comes to the chip sector, it grasped the opportunity to adopt RISC-V for broad industrial R&D in open source silicon and now invests heavily in an innovative infrastructure of open source silicon.[43] Furthermore, open source silicon is utilised to counterbalance the significant U.S. export controls that China faces at the moment and to grow an independent domestic semiconductor ecosystem.[44] The Chinese government is systematically subsidising this and is deploying dedicated public-private partnerships within the sector to spur innovation and increase self-reliance.[45]

In the US, incentives for open source silicon are not only provided on an industrial level (see open PDK section above), but also on a government level. On the one hand, the Creating Helpful Incentives to Produce Semiconductors and Science Act (CHIPS for America Act) has the objective of reshoring and near-shoring manufacturing and innovative R&D processes that are considered relevant for its supply chain resilience.[46] It takes into account the benefits of open source and open science for the domestic semiconductor ecosystem.[47]

For instance, within the scope of a Request for Information (RFI), the Act's implementation strategy reflects methods to provide free and open access to important inputs and processes, such as EDA tools and IP. It recognises the accelerating role of openness in R&D as well as in lowering market entry barriers for small, fabless companies.[48] In light of China's OS efforts in its domestic chip sector, however, the US is partly considering ways to limit its OS developments to like-minded international partners, e.g., through export controls on open design platforms.[49]

In contrast, the U.S. Department of Defense's (DoD) Research Agency, DARPA, has been betting on open source silicon for longer in various projects. While its POSH project, for instance, funds the development of open source hardware IP and respective symbolic verification tools,[50] its toolbox initiative is targeted to facilitate easy access to tools and IP at low cost for DARPA funded research programs. It involves several open source silicon stakeholders, such as SiFive. Although knowledge sharing is accelerated within the toolbox infrastructure, the use of corresponding knowledge may be subject to non-disclosure agreements (NDAs) and is not considered open source as such.[51]

India[52] aims at enabling a broad domestic infrastructure around RISC-V, leading to a strong OSH innovation ecosystem, and is providing support on the governmental level. The Ministry of Electronics and Information Technology officially fosters efforts to grow a large open source silicon talent pool, and to boost chip design capacities in India. The undertakings include the establishment of the Digital India RISC-V (DIR-V) programme that is to support Indian start-ups and bridge the gap from academia to commercialisation.[53]

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42. An overview of international semiconductor incentives and fab announcements (as of 2022) is provided by the U.S. Semiconductor Industry Association (2022): **Global Semiconductor Incentives**.
43. Shah (2023). **How China is Building an Open National Chip Plan Around RISC-V**. HPCwire.
44. Hess et al. (2023). **Who is funding the chips of the future?** SNV Berlin.
45. Arcesati & Meinhardt (2021). **China bets on open-source technologies to boost domestic innovation**. Merics.
46. The White House (2022). **FACT SHEET: CHIPS and Science Act Will Lower Costs, Create Jobs, Strengthen Supply Chains, and Counter China**.
47. NIST. U.S. Department of Commerce (2023). **A Vision Strategy for the National Semiconductor Technology Center**. CHIPS Research and Development Office.
48. NIST. U.S. Department of Commerce (2022). **Incentives, Infrastructure, and Research and Development Needs to Support a Strong Domestic Semiconductor Industry**. Summary of Responses to Request for Information.
49. Congressional Research Service (2023). **Frequently Asked Questions: CHIPS Act of 2022 Provisions and Implementation**.
50. Lim (n.d.) **Posh Open Source Hardware (POSH)**. DARPA.
51. DARPA (n.d.) **DARPA Toolbox Initiative**.
52. See, e.g., Indian Institute of Technology Madras (2023). **SHAKTI**. Open Source Processor Development Ecosystem.
53. Economic Times Telecom. **RISC-V becoming a global movement with India as leading player: MoS IT**, and: Jain (2023). **Open-Source Movement in India Gets Hardware Update**. Analytics India Mag.

The UK's National Semiconductor Strategy is focusing more on deepening significant existing strengths than mitigating weaknesses. While ensuring the important role of IP supplier and chip designer Arm, the UK also explicitly supports the broad uptake of and community-building around the RISC-V standard, especially regarding education, R&D and security by design approaches.[54]

In the context of Europe's digital sovereignty goals[55] and aligned with its goal of Open Strategic Autonomy, Europe is seizing the opportunity that open source silicon provides: The European Chips Act (pillar I)[56] focuses on the intensification of joint collaboration within Europe, with a focus on the integration of the RISC-V standard and openly-accessible research. Concrete capacity-building actions, i.e., the Chips for Europe Initiative, are enabled through the Chips Joint Undertaking (Chips JU) that absorbs the entities and activities of the current Key Digital Technologies Joint Undertaking (KDT JU). It combines Horizon Europe (HE) and Digital Europe Programme (DEP) efforts as well as resources of Member States and third countries.[57]

The EC already initiates and funds several foundational R&D projects through HE that integrate or even focus on RISC-V, such as the European Processor Initiative (EPI)[58] or the TRISTAN consortium that enables joint efforts of large enterprises.[59] Furthermore, a design platform foreseen by the Act is enabling a large-scale design infrastructure for integrated semiconductor technologies and is to include open source design solutions. Its access is intended to be open, non-discriminatory, and transparent.[60]

Overall, numerous regions that are relevant to various inputs, processes or steps in the value chain of semiconductor technologies focus on reinforcing strategies that build on R&D and industry support. They recognise the important role of open source in this hardware domain for increasing resilience and fostering national or regional R&I activities on open source silicon.

For the EU, it seems clear that regional chip sovereignty should be led by openness angles in OSH innovation areas that are already mature, such as RISC-V. In integrating openness in its reinforcement strategies in a geopolitical context, the EU is aware of the significance of international cooperation within a highly complex and interdependent value chain. It focuses on collaborations and alliances that share its democratic understanding, working together with allies and partners in this field to advance common interests and ensure fundamental democratic values and ethical standards.

54. UK Department for Science, Innovation & Technology (2023). **National Semiconductor Strategy**.
55. These goals are set in the EC's 2030 Digital Compass and include an intended 20% share of the global "cutting-edge and sustainable" semiconductor production in the EU by 2030. See: EC (2021). **Europe's Digital Decade: digital targets for 2030**.
56. The Chips Act outlines three pillars: the Chips for Europe initiative, the security of supply, and monitoring and crisis. Since open source silicon is instrumental to capacity building and R&D advances, it is tied to pillar I.
57. EC (2022). **European Chips Act: Communication, Regulation, Joint Undertaking and Recommendation**.
58. See the **European Processor Initiative** (2022).
59. Horizon Europe (2023). **Together for RISc-V Technology and ApplicatioNs**.
60. EC (2022). **Proposal for a Regulation establishing a framework of measures for strengthening Europe's semiconductor ecosystem (Chips Act)**.

OPEN SOURCE SILICON UNDER THE SWOT LENS

Besides semi-structured interviews as well as webinars with relevant experts, this policy brief's recommendations are based on a SWOT analysis of open source silicon for strengthening the European semiconductor ecosystem. The main takeaways from this knowledge gathering are that the open source silicon approach brings significant strengths in enhancing the academic sector and thus in reinforcing the foundation of innovation in the industry. This is primarily a result of open source silicon providing a catalyst for innovation in the production step of chip design. However, it must be pointed out that this area of OSH is still nascent and therefore often lags behind leading-edge proprietary tools or processes. Nevertheless, it offers a large potential for high-level integrations, which should be recognised as strategically relevant. Forming the foundation of the concrete recommendations, this section briefly explains the opportunities and threats that are derived from strengths and weaknesses.

SWOT analysis	**Beneficial – open source silicon as a strategy for strengthening the EU semiconductor ecosystem**	**Adverse – open source silicon as a strategy for strengthening the EU semiconductor ecosystem**
Internal (structural-organisational, within Europe's semiconductor ecosystem)	**Strengths** • Research and skills advantages by OSH and open science dynamics (academic support) • Research and education benefits of open source silicon components (e.g., PDKs) • Innovation boost by academic and industrial OS community support and OS ecosystem • Competition increase in the chip ecosystem • Low cost and low access barriers to innovation • Simplicity and interoperability of designs • Security through transparency (possible source code analysis and open data) • Less affected by geopolitical tensions	**Weaknesses** • Legal expertise needed for small players • Lack of mature industry IP • Lack of clear business cases in early stage OSH • Insufficient OSH-specific industry support • Unforeseen security, maintenance and compliance needs posed by OSH and its R&D dynamics • Unforeseen market dynamics • Women are underrepresented in the semiconductor industry and open source
External (contextual, focus on Europe within the global value chain)	**Opportunities** • Boosting the academic foundation of the EU semiconductor ecosystem (talent and innovation) • Research and education opportunities by open source silicon (e.g., PDKs) • Supporting academia-industry exchange through OSH within the EU • Lowering and sharing of costs (R&D, community support) • Novel licensing schemes for hardware innovation • Progress in security • Support of small players, i.e. start-ups and SMEs (cost, compliance, interoperability, etc.) • Windows for European innovation advances (analogies with OSS) • Strengthening like-minded cooperations by open source silicon initiatives within policy frameworks such as TTCs • Finding reasonable positions for EU within geopolitical tensions • Synergies of European Chips Act and open source silicon in international collaboration with alliance partners	**Threats** • Falling short of a OSH critical mass to scale up innovation • Market dynamics weakening the EU standpoint within the global value chain due to innovation head start by other regions integrating open source silicon • Missing the opportunity to attract more women to the sector • Unrecognised and unaddressed security, maintenance and interoperability requirements
Derived policy considerations	**Steps for policy and funding** • Incentivise R&D openness • Foster security through transparency • Strongly collaborate with like-minded regions • Create early industrial support	**Steps for policy and funding** • Monitor and address new maintenance and compliance needs • Create legal certainty through research, funding, and policy • Aim at critical mass in OSH • Encourage women in STEM and encourage openness regarding diversity

Table 1 - SWOT analysis, one degree of abstraction: Open source silicon for EU sovereignty in the semiconductor industry

Key opportunities relevant to open source silicon strategies

An industry similar in size and maturity of the OSS ecosystem has not yet emerged in OSH. The ventures that are mature enough to reach the mainstream stages, such as RISC-V, are still in the early stages of their development. However, in expert circles, the phenomenon of OSH is described as being at a stage similar to that of OSS twenty years ago.[61] In order to achieve network effects by opening and initiating overt exchange of innovation inputs rooted in open source, it is relevant to take advantage of the broad collaboration, participation and community of OS dynamics and to nurture and cultivate them institutionally at European universities and research institutes.

Boosting semiconductor R&D in Europe

On the one hand, key opportunities that should be exploited include recognising the important role of open source silicon to support and extend semiconductor R&D in Europe. Being situated within a broader open science framework, open source silicon enables both the support of the open source community as well as the academic community, accelerating development and revision of ideas by both collaborative and competitive means. The open source approach in the semiconductor field enables a significant lowering of barriers to entry in research and development, with prospects for easier market entry once the approach is taken from the academic lab to the fab. This is instrumental in improving the attractiveness of studies relevant to innovation in the processor and semiconductor technology sectors.

Requirements for chips are becoming ever more specialised in the age of artificial intelligence (AI) and the possibilities for combining multiple processors with different sets of special purposes for a higher-level task are on the rise. Research efforts worldwide have broadly embraced open source silicon advances due to their innovative strengths, in particular on the basis of RISC-V.[62] European academia is already an important location for open source hardware (OSH) and, more specifically, also open source silicon-based innovation. However, on the one hand, several open source silicon components are still missing to go full speed. On the other hand, there is still a severe shortage of foundational skills in the microelectronics industry, in particular, a shortage of software engineers, and advanced systems architecture designers.[63] Open source can be beneficial for research and education since it allows for real-life examples of innovation, community support as well as low access barriers for new talent.[64]

Security through transparency

When it comes to semiconductor technology, cybersecurity and hardware security-related questions are of strategic importance throughout the industry and its stakeholders.[65] The notion of openness in hardware may evoke greater technological vulnerability to compromise attempts in some audiences. It is important to remember, however, that open source silicon is located primarily in the chip design step. This production step is characterised by a low level of national security risks, including cybersecurity and hardware security risks. In contrast, it comes with a high level of geoeconomic competitiveness dimensions.[66]

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61. See, e.g.: Davis (2022). RISC-V in Europe: **The Road to an Open Source HPC Stack**. Barcelona Supercomputing Center.
62. See: EC Working Group on OSH and OSS (2022). **Recommendations and roadmap for European sovereignty on open source hardware, software and RISC-V Technologies**.
63. For more detail see: Coulon et al. (2022). **Yearly Monitoring Report 2022**. METIS.
64. Often it is the heritage in tradition and sincere commitment of universities that allows projects to be continuously nurtured and to create long-term breeding grounds for an enrichment of activities as well as for a transfer of knowledge of academic discoveries into industrial projects. However, the open source character is in general such a strong advantage, because it also allows a high speed and flexibility of innovation. Traditions are important but are constantly revised in OSS and OSH by emerging trends that originate in the real world and allow a realo check of conducted innovative projects. Open source enables a qualitative benchmark, which generates intense competitiveness, as research, knowledge, development and innovation are continuously verified by peer reviewers and contributing developers. This competitive strength should be recognized and exploited as a great potential for both students, researchers, developers as well as faculty and the projects they are involved in. Hence, it is important to harmonise the university context with these intrinsic open source features – to cultivate a vibrant research base that is open to competitive exchange with the industry as well as application-specific feedback from the open source community. This could be also achieved by adjusting university quality standards to modern requirements. Often, for instance, papers are in the spotlight when it comes to making academic success visible. However, aligned with the strengths as well as benchmarks of open source, other achievements such as completed projects should be considered equally important KPIs.
65. Blind et al. (2021). **The impact of Open Source Software and Hardware on technological independence, competitiveness and innovation in the EU economy. Final Study Report**.
66. According to Kleinhans, it is mainly the ATP production step, in particular assembly processes, that allow for the implementation of hardware-specific threats, e.g., backdoors. In the design step, threats could be specific malware – which might be discovered more likely under OS conditions. See the overview of competitiveness benefits, national security risks, and resilience reflections of the strategic dimensions of the chip value chain provided by SNV Berlin: Lee & Kleinhans (2021). **Mapping China's semiconductor ecosystem in a global context** (p.11). SNV Berlin.

Problems that OSH brings forth are rooted rather in the firmware and hardware in general than in their OS nature, thus they are also an issue of closed technologies.[67] Still, the potential of a chip being compromised is a remaining risk within the semiconductor industry that should be tackled throughout the value chain and should be thoroughly investigated, studied and considered when it comes to reinforcing Europe's semiconductor ecosystem. In comparison to software hacking attempts, exploiting vulnerabilities at a hardware level is achieved primarily in highly-targeted and mature cyber threats. This may relate to the underlying processor architecture, which should ideally prove to be particularly resilient. Notably, architectures that are disclosed upfront are subject to continuous evaluation by developers, experts and contributors. In contrast, undisclosed architectures are primarily reviewed by company internal security assessments and do not benefit from the rapid revision processes and collaborative improvements of the OS community. Hence, without these OS revision mechanisms, security issues in proprietary hardware architectures might be communicated to the end consumer later than necessary.

The subject can best be explained by contrasting two concepts: security through obscurity and security through transparency. The concept of security through obscurity relies on secrecy about the inner mechanisms, algorithms, or implementations of a system, with the assumption that it is more secure because potential attackers cannot see the design and its details. However, this concept constitutes only a weak form of security because it relies solely on keeping the design secret, which can be compromised as soon as the details are accidentally or intentionally unveiled. On the other hand, the concept of security through transparency refers to technologies that are transparent by design – i.e. open source to a significant degree – and thereby enabling the public examination and third-party review as an important source of security. This openness allows OS communities composed of experts from different stakeholder groups such as academia or industry to be part of a thorough auditing and peer review process of the system's design and code. This not only ensures an accelerated and broad identification of vulnerabilities but also increases public awareness and trust in the systems. Indeed, open source silicon offers the possibility of qualitative feedback and collective quality assessment and control through the collaborative dynamics associated with the approach.[68]

Bottom-up industrial reinforcement

The general modularity and interoperability of open source is also characteristic for the open source silicon approach. A further opportunity is, hence, that this promotes the bottom-up strengthening of the industry from a macroeconomic perspective. In the current era where chiplets are becoming ever more paramount and higher interoperability and embedding requirements must be met, open source is particularly important to innovation. Open access to knowledge, community support as well as lower barriers to enter an innovation segment and the market in general comes with many opportunities for smaller players such as start-ups and SMEs.[69]

New niches in the landscape can be easily recognised, openly communicated and covered by smaller players such as research projects that develop a business case, start-ups, scale-ups and SMEs. If Europe has a strong OSH ecosystem, these industrial players can move faster on such opportunities overall, and build quickly and in a complementary way on the existing ecosystem. Without being tied to a proprietary vendor, companies can purchase licences from several vendors and be more flexible to develop and customise their own IP while also increasing interoperability in the ecosystem.

After start-up phases and early innovation stages have been accelerated by open source, European start-ups and SMEs can seek best practices to expand market share and scale up. Since open source silicon creates new challenges in terms of different compliance issues, however, legal uncertainties need to be addressed strategically by expertise provided by coordinated entities.

67. See, e.g.: Davis (2022). RISC-V in Europe: The Road to an Open Sour See, e.g., the recent Zenbleed bug of AMD's x86 processor family, affecting Ryzen and Epyc Zen 2 chips: Ormandy (2023). **Zenbleed**. In contrast, it was discovered and discussed by the OS community. OS security repositories are very valuable for cybersecurity, such as: Google (n.d.) **Security Research. Project**. ce HPC Stack. Barcelona Supercomputing Center.
68. Goldmann (2023). **How Secure Are RISC-V Chips?** Semiconductor Engineering.
69. While this policy brief focuses on smaller players, i.e. start-ups and SMEs, open source silicon is also beneficial to large enterprises. Especially in vertical industries where the design requirements are expected to increase significantly in the upcoming decades, such as automotive, the cost effectiveness of the open source silicon approach reinforces domestic industries. See for more information on chiplets as well as applications for verticals: EC Working Group on OSH and OSS (2022). **Recommendations and roadmap for European sovereignty on open source hardware, software and RISC-V Technologies**.

Threats relevant to open source silicon strategies

An opaque gap between academia and industry

As indicated in the SWOT analysis, several threats should be considered and mitigated. Market dynamics can weaken the EU's position in the global value chain if the open source silicon strengths remain untapped by domestic industrial uptake while other regions gain an edge in innovation by integrating them. Obstacles to integration should be identified and overcome. Although several European universities and research institutes are at the leading edge of open source silicon research,[70] and some European SMEs are taking up the research results at scale, many innovations based on the research are carried out elsewhere.

Start-ups are emerging around the world but European start-ups are sometimes struggling to integrate the open source approach in their product portfolio due to a lack of local legal expertise, fragmentation of solutions or struggles with commercialising. In contrast, China-based start-ups are flourishing by adapting quickly and successfully to the new innovation scheme enabled by open source silicon, strengthening China's national competitiveness.[71] The existing gap between academia and industry, i.e. commercialisation in Europe, should not be left opaque but should be analysed in-depth. Some challenges are already identifiable and need to be addressed ad-hoc in this course.

Missing the opportunity to attract more women to the sector

Gender disparity at an academic level is, from an international perspective, particularly evident in STEM study fields and related professions,[72] resulting in a tremendous amount of talent and innovation at risk of remaining unrealised. As of 2022, in its global monitoring of the annual progress of the Sustainable Development Goals (SDGs), the United Nations report a share of only 35 percent women in STEM studies and only 20 percent of women in science and engineering professions. Consequently, this underrepresentation of women in STEM fields has significant economic implications that also materialise in the semiconductor industry.

According to survey results by Accenture and GSA, only 10-15 percent of technical positions and only 13 percent of executive positions are held by women in the international semiconductor industry in 2022.[73] The lack of gender diversity in the industry, in particular the underrepresentation of women leads to a loss of valuable talent and ideas, which hinders innovation and slows down digital sovereignty overall. This is surprising, since the role of women in the technological history of computation and semiconductor development – thus the formation of silicon valley was decisive.[74] However, this role is not elucidated and emphasised enough.

70. Leading research in open source silicon approaches, often with a focus on low-power or a focus on HPC is done, e.g., at the University of Bologna, at ETH Zurich, at the University of Turin, at the Barcelona Supercomputing Center (BSC), at the University of Cambridge, and at CERN.
71. Shah (2023). **How China is Building an Open National Chip Plan Around RISC-V**. HPCwire.
72. UN Women (2022). **Progress on the Sustainable Development Goals: The gender snapshot 2022**.
73. Accenture (2023). **Unlocking the Value of Women in Semiconductor** as well as **GSA Brief: Women in the semiconductor industry 2022**.
74. See, e.g., Hempel (2016). **A women's history of silicon valley**. Wired.

Similarly, women are underrepresented in open source.[75] For instance, women's participation in various OSS communities only represent a proportion between 4 and 14 percent.[76] Several efforts have been made to identify the reasons for this or to provide incentives for more women in open source, e.g., through competitions. One key issue is that the culture of open source is still too discouraging for women.[77] Hence, a threat of open source silicon is that it fails to mobilise and motivate women, adding an additional disincentive for more women in the ecosystem. Therefore, a broader theme of openness and diversity should be encouraged in the integration of open source silicon and open source in general to ensure that the approach is successfully inclusive. This can be achieved, for instance, by creating synergies with the realisation of open science that is allowing for cultural changes in universities, and in which women participate more strongly.[78]

Failing to build a critical mass in OSH and open source silicon

Failing to build a critical mass in OSH and open source silicon can be a threat to European semiconductor sovereignty strategies because it hampers collaboration, interoperability and innovative roots. Furthermore, alternative open technologies to third party IP can support building a robust domestic ecosystem that is open to R&I impetus from active academic projects. Such a failure could be the case when open source projects are not continued, repositories not maintained and collaborative communities not incentivised enough. Fostering a critical mass in OSH and open source silicon can be achieved by communities, organisations, and environments that mediate between public entities, industry, and academia. Their efforts to track needs and best practices, monitor developments and risks, recognise new windows of opportunity and study the complex legal challenges of open source are highly relevant for controlling these threats.

In the following section, detailed advice for increasing European chip sovereignty by an open approach refers to how to shape efforts that are based on and informed by these main opportunities that the EC should seize, and threats that the EC should be aware of when developing policy and funding strategies that integrate open source silicon. These recommendations complement key points of the more specific technical requirements outlined in the OSS and OSH roadmap, and highlight a multi-stakeholder R&I path shaped by education and skills.[79]

75. Grzegorzewska (2021). **There are fewer women in open source than in the ICT sector overall**. EC Open Source Observatory (OSOR).
76. Trinkenreich et al. (2022). **Women's Participation in OSS: A survey of the Literature**. ACM.
77. Trinkenreich et al. (2022). **Women's Participation in OSS: A survey of the Literature**. ACM.
78. Murphy et al. (2020). **Open science, communal culture, and women's participation in the movement to improve science. PNAS. Psychological and Cognitive Science**.
79. EC Working Group on OSH and OSS (2022). **Recommendations and roadmap for European sovereignty on open source hardware, software and RISC-V Technologies**.

RECOMMENDATIONS FOR EUROPE'S CHIP SOVEREIGNTY BY STRATEGIC OPENNESS

The following policy recommendations follow the course of insights gained within the first stakeholder engagement within ALLPROS.eu, a series of expert interviews, and are derived from the SWOT analysis. While the overarching topic is related to why and how open source silicon can be used to strengthen innovation in the European semiconductor ecosystem, areas were highlighted that follow the emerging synergies of ALLPROS.eu. For instance, ALLPROS.eu's joint efforts with the EC and the KDT JU elaborated a shared focus on skills. This important focus, backed by insights gained within the semi-structured interview process and webinars, is embraced and related to open source silicon in the following recommendations, to enable a bottom-up approach for Europe's chip sovereignty through strategic openness that is rooted in education.

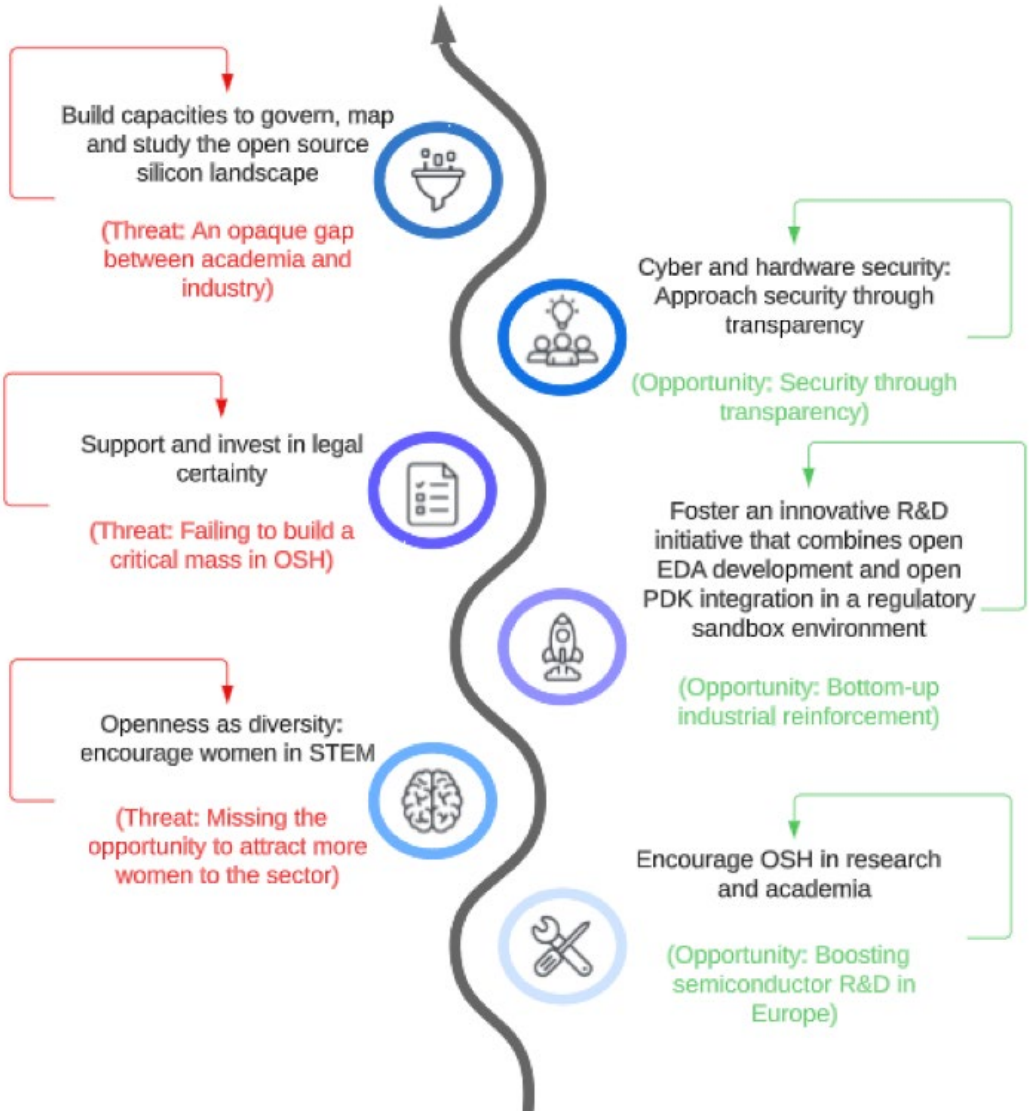

Figure 4 -Recommendations for Europe's chip sovereignty by strategic openness

1. Encourage open source hardware in research and academia

Initiatives and frameworks providing funding and policies for open source silicon and OSH at European research institutions should be overall encouraged.

Research, academia, and education as a stakeholder group with major impact for OSH innovation and in the European semiconductor sector should be accompanied by state-of-the-art funding and support strategies. Initiatives and frameworks providing funding and policies for open source silicon and OSH at European research institutions should be overall encouraged.[80] Within the framework of open source and synergies achieved through international collaboration, initiatives should also be realised in European universities by public-private partnerships that aim to involve universities for triple helix oriented R&I activities enabled by the EU's Chips for Europe initiative and associated programmes. Existing EU frameworks focussing on open innovation concepts that are rooted in research, academia and education should be supported to build synergies with these initiatives.[81]

It is important for European universities to approach related graduate studies, such as microelectronics or embedded systems related fields, with the application-tied approach of OSH to leverage and successfully integrate these advantages. To that end, the EC should encourage research and education stakeholders to integrate open source in the academic curriculum.[82] RISC-V is allowing this to be realised in the design of processors, and universities are increasingly adopting the RISC-V ISA already. The EC and relevant research programs funded by the EC, for instance during HE, should encourage the use of RISC-V in research, academia and education. Within funding and policy frameworks, incentives at the academic level should be considered to motivate OS integration in an open ecosystem of higher education, such as awards for research organisations, groups, and individual researchers. Funding activities should be inclusive in such a way that universities that have strong ties with those in the EU should be included and international collaboration encouraged.[83]

2. Openness as diversity: Encourage women in STEM

To prevent an additional barrier to attract more women to the semiconductor sector within the implementation of open source silicon, openness has to be communicated and promoted within a strong understanding of the sociotechnical relevance of diversity. Concrete synergies should be created between women in STEM initiatives and semiconductor R&D.

80. Standardised study modules could be developed within a targeted EU policy format such as a thematic working group (TWG), which aims to define and explain the modules so that universities can easily incorporate them. These modules should include legal courses in the area of OSH licensing, commercial questions in the area of open source silicon, as well as socio-technical issues such as reflection of socially related topics, e.g., inclusive skills acquisition and sustainable manufacturing solutions.
81. A suitable format would, e.g., be EU-backed clusters of excellence at European Universities such as **LERU**.
82. Suggestions concerning a successful integration are also made by Sarancio (2023): **Supporting Open Science Hardware in Academia: Policy Recommendations for Science Funders and University Managers**. Zenodo.
83. For instance, centres of innovation at the University of Cambridge and ETH Zurich, which play a crucial role for the open source silicon network of the EU and for the research strength of the EU in the domain.

In accordance with the 2023 European year of skills,[84] and building on the triple helix concept,[85] long-term strategies integrating the approach of open source silicon should be developed to increase the talent pool in the semiconductor ecosystem. This increase in talent will consequently result in stronger innovation forces in Europe's strategic R&D

fields related to processor and semiconductor technologies. Other regions or states are successfully integrating publicly-funded initiatives with private companies providing open source silicon solutions for university R&I purposes as well as for bridging skills gaps in the microelectronics design.[86] If Europe aims to increase its market share in the semiconductor industry, however, at the same time as there is a shortage of skilled labour, it simply cannot afford to leave half of the workforce behind. To prevent an additional barrier to attract more women to the semiconductor sector within the implementation of open source silicon, openness has to be communicated and promoted within a strong understanding of the sociotechnical relevance of diversity.

Open source silicon concepts should be embedded in a broader framework of open science and open innovation relating to further key concepts such as open standards that also guides EU coordinated efforts as an overarching goal, ensuring a broad collaboration and a broad exchange of education material and, hence, reducing barriers to entry to a R&I domain.[87] The low access barriers, high community support, and competition benchmarks of open science can contribute to an openness shift in semiconductor research and industry that is targeted at an open and diverse community.

All EC incentives strengthening the sovereignty through open source incentives for research and academia should therefore be implemented in a very inclusive manner targeting open science awareness, that is encouraging women in STEM, especially in microelectronics and related fields. Concrete measures, benchmarks and expected performance targets should be defined, motivated and implemented. Based on the following starting points, they should be clarified and implemented in a pioneering spirit: On the one hand, these efforts should be aligned with existing EU endeavours on open science such as portals, working groups or projects.[88]

On the other hand, these efforts should be aligned with skills initiatives, setting defined standards when it comes to gender criteria in EC funded projects.[89] Reasons for the loss of women in the semiconductor industry and the location of most exits of women from the talent pipeline should be identified. The interventions and measures required to improve the given situation should be analysed as extensively as possible. In general, the EC should strongly foster efforts to make the semiconductor ecosystem more inclusive and diverse, and to create supportive environments that promote the role of women in STEM and semiconductors. Existing activities by various stakeholders should be reinforced and promoted.[90]

It is important to consider, however, that education, skill acquisition and inclusive knowledge cultures relevant for the domain do not start at a university level – and should be initiated at an earlier stage. Special attention should be given already at earlier levels of education to the motivation and mobilisation of female talent for STEM fields as well as science and engineering professions. EC initiatives should be intensified when it comes to promoting a technical path for girls in European primary and secondary schools, especially in Member States where this is not yet realised. This is essential for a push of Europe's innovative power in this field, especially considering the shortage of qualified professionals Europe is facing at the moment. Success stories in Europe can provide guidance in the implementation of triple helix initiatives at a secondary school or similar level.[91]

Promoting fields relevant to semiconductor R&D and open source within a triple helix approach is decisive for enhancing the participation of female students. For instance, OSH and OSS platforms that are providing application-oriented learning environments for students, including support communities and training resources could be used as a starting point.[92]

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84. EC (2023). **European Year of Skills**.
85. The triple helix concept is built on the three pillars of public, private, and academic aligned efforts. In contrast to pure PPPs, it introduces a direct exchange of demands concerning specific innovation components such as research and funding as well as collaborative schemes at the three levels of universities or research institutes, industry, and national or regional governments.
86. An inspiring example is, for instance, the cooperative R&D agreement reached between NIST, Google and SkyWater and several universities in the US, providing open source results: NIST (2022). **NIST and Google to Create New Supply of Chips for Researchers and Tech Startups**.
87. EC (n.d.). **The EU's open science policy**.
88. Important activities are, e.g., coordinated by the European Open Science Cloud (EOSC) and **published on its portal**.
89. E.g., the efforts could relate to the **EU pact for skills**.
90. E.g., Intel is setting concrete goals for women in technical and leadership positions (such as to double the number of women and underrepresented minorities in leadership roles by 2030): Intel (2023). **Corporate Responsibility Report**.
91. Here, striking examples are shown on a regional level within CERN's Expanding Your Horizons events, aiming at the motivation of female students: CERN (2022). **Expanding Your Horizons: a new generation inspired by women in science**. On a national level, Ireland's STEM Teacher Internship Programme should also be mentioned: Dublin City University (2020). **STEM Teacher Internship (STInt) Programme**.
92. Leading OS platforms in the area of education are, e.g.: Arduino (n.d.). **Arduino Education. Empower Scientists and Artists of the Future** and Raspberry Pi Foundation (n.d.). **Teachers & Educators**.

3. Foster an innovative R&D initiative that combines open EDA development and open PDK integration in a regulatory sandbox environment

The EC should initiate and fund an R&D initiative that develops, applies, and distributes open EDA tools and open PDKs for educational purposes that are not exempt from commercialisation opportunities but initially simplified in their legal requirements. Within these efforts, the EC should incentivise the release of open PDKs in Europe for educational purposes, providing up-to-date application focus to R&I.

Overall, Europe should strengthen existing efforts to leverage this window of opportunity provided by open source silicon for its regional competitiveness, and should accelerate these efforts through strategic synergies bridging the gap from scientific theory to industrial practice, bottom-up.[93] The EC should launch and fund an R&I initiative that has the goal to develop, apply, and disseminate open source tools, IP and further specifications.[94] This recommendation is in accordance with the roadmap for European sovereignty on OSH, OSS and RISC-V technologies which suggests an "approach similar to the EPI, bringing together key technology providers and users across the value chain with the goal of producing open source IP".[95]

Since they go hand in hand, the initiative should focus on both open EDA tools development and open PDKs for educational purposes, allowing for a mature, open design flow. The steady dialogue between the program's initiators, the designing and the manufacturing entities should be facilitated and encouraged. Free and open standards are strongly advocated, while outcomes of the initiative should not be exempt from the possibility of commercialisation.[96] This can be implemented in various formats, such as a specific regional lab initiative with multiple European universities with the option for industrial partnerships and early funding support. It is necessary to ensure an encouraging innovation environment that is not hindered by bureaucracy or novel legal situations. Therefore, a setup similar to a regulatory sandbox would be a suitable starting point for accelerating the industrial adoption of open source silicon-based ideas.

Foundries tend to be protective of their PDKs through strict non-disclosure agreements (NDAs) for various reasons, e.g., they can contain sensitive data or trade secrets – and, providing free and open access to PDKs simply lacks a business case for pure-play foundries. From a macroeconomic perspective, in contrast, open PDKs can help to boost the chip design sector by means of research and education. Although the PDKs released so far are not at the cutting edge of semiconductor innovation,[97] they come with great advantages for education, talent acquisition and innovation spillover effects. Because chip design brings the highest profit margin in comparison to other production steps, it is expected to enhance the industry significantly. Hence, the EC should incentivise the release of open PDKs in Europe, providing up-to-date application focus to R&I. This makes sense because the advantages of open PDKs for education and research outweigh potential disadvantages such as opening IP of foundries. Although it is likely that PDKs on the trailing rather than the leading edge will be opened in such an incentivised development, this creates value to the industry that is closely tied to education and research proceedings. The EC and related bodies should integrate these open PDKs in overall R&D capacities initiated by the Chips Act and relate them respectively to the design platform.

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93. In this domain, e.g., European consortia like **SCYLOPS**, **TRISTAN**, or **EUPILOT** combine OSH, open standards, and leading-edge microelectronics.
94. The project could be realised through **Europractice** and have a similar structural framework as the **DARPA toolbox initiative** (but focus on OSH). It should build synergies with other Europractice initiated R&D infrastructures and important European actors, such as CERN's IP and tool sharing infrastructure within the scope of the European Committee for Future Accelerators (ECFA). See: Kloukinas et al. (2023). **ECFA R&D electronics**. Presentation. CERN.
95. EC Working Group on OSH and OSS (2022). **Recommendations and roadmap for European sovereignty on open source hardware, software and RISC-V Technologies**.
96. While these design components will be open, innovation based on the components may be either open or closed. Outcomes that remain open should be encouraged if financing is provided by the EC and its subordinate bodies. While OSH usually does not lack academic contributions, industrial contributions to the European OSH space should also be encouraged.
97. While GlobalFoundries' PDK is designed for 180 nm node technology, IHP's is targeted at 130 nm node technology. In contrast, 2nm processes designed in recent years will be realistic for manufacturing from the year 2024.

4. Support and invest in legal certainty

The EC should support and invest in initiatives, resources, and capacities that lead to more legal certainty for small players that are integrating open source silicon, i.e. start-ups and SMEs.

As is the case with open source being foundational in the software industry today, open source brings a promising business perspective to the hardware and, in particular, chip industry.[98] This is well recognised by the increasing number of start-ups that build their innovation on top of existing open source silicon solutions. However, when it comes to the necessary scaling up of their production, some start-ups and SMEs that rely on open source report legal uncertainty. A lack of legal expertise for the purposes of licensing and identifying the origin and framework of open source silicon contributions in the open ecosystem, seems to be a central issue for start-ups and SMEs in adopting open solutions for semiconductor innovation. Hence, the EC should support and invest in initiatives, resources, and capacities that lead to more legal certainty for small players, i.e. start-ups and SMEs.

This should lead to legal expertise provided in a EU-coordinated manner instantiated on the national level of Member States. Already existing activities, knowledge bases and institutions should be reinforced and complemented by respective resources that are developed ad hoc.[99] Strengthening the European chip sector bottom-up requires not only broader and more inclusive academic initiatives but also requires leveraging the academic results of European research. A first step in addressing the gap between European semiconductor academia and industry[100] is to support start-ups that build on research results with the necessary legal expertise. This needs to be achieved by ensuring regulatory support targeted at open source silicon initiatives, that helps to facilitate an unbureaucratic and legally sound transition to industrial practice.

5. Cyber and hardware security: Approach security through transparency

The EC should support and invest in OSH efforts that target security through transparency (not obscurity).

Security R&D prioritises the concept of security through transparency in contrast to security by obscurity since it brings forth efficient mechanisms of error detection and correction.[101] Because of these community-based mechanisms, OS offers advantages for the security of processor and semiconductor technologies in general. By this rationale, the EC should focus on fostering transparency and disclosure of building blocks of designs in general – but also foster openness of security standards and security specific applications, such as Root of Trust (RoT) architectures.[102] Within such an open infrastructure, security controls are accelerated by the community enabling transparency and security by design. This ties in with OSS security and could be linked to existing EC efforts. In the area of OSS, EU funded projects achieved significant success that spilled over to other domains.[103]

98. Considering the past transition from innovative open source software (OSS) projects to a broader industrial uptake, as in the case of Linux and Red Hat, it should be noted that such a transition phase has taken several years to be complete.
99. These capacities should be related to the competence centres defined in pillar I of the European Chips Act in a targeted manner. See: EC (2022). **Proposal for a Regulation establishing a framework of measures for strengthening Europe's semiconductor ecosystem (Chips Act)**.
100. See e.g., Hebben (2021). **Securing European sovereignty: Key recommendations for open-source hardware and software**. Inside.
101. Goldman (2023). **How Secure Are RISC-V Chips?** Semiconductor Engineering.
102. RoT refers to verifiable and foundational security functions being conducted by particularly robust hardware, firmware, or software components. These components are built using a security by design approach and enable the realisation of further security functions in more downstream parts of the system. A promising example of open source silicon root of trust is, e.g., established by **lowRISC**.
103. EC (2020). **EU-FOSSA 2**.

In terms of general OS security, it must also be considered that projects require relevant and continuous capacities to guide a robust and secure technological development, i.e. to carry out regular security and performance audits, documentation and traceability, maintenance, and safety-essential updates. European projects, institutions, or organisations dedicated to these efforts should receive adequate financial and compliance support from the EC and downstream entities.

6. Build capacities to govern, map and study the open source silicon landscape

The EC should fund and support research projects that focus on interoperability, novel legal requirements or challenges, and keep track of open source silicon components, including measuring the impact of OSH and growth of open source silicon.

An established market in OSH is important to achieve a significant scale-up effect in the European semiconductor ecosystem. A long-term support strategy should be developed and implemented with patience in the case of new and unknown challenges, including strategic foresight so that the domestic gap between academia and industry is bridged and relevant networks and synergies can emerge and be established.

This should be induced by incentives with a focus on start-ups and industrial OSH projects and stimulated by targeted activities such as support concerning funding, legal compliance,[104] communications and outreach. To provide scale-up support on an European level and thereby to bridge from academic projects to industrial practice, long-term capacities should be initiated and put into practice that work closely with the EC.

To this end, the EC should fund and support farsighted research projects that focus on maintenance, interoperability and securing of open source silicon components. The efforts should include measuring the impact of OSH and growth of open source silicon, initiating market studies,[105] mapping the key players and activities in the domain, and conducting research and support actions targeted to describe novel legal situations and increase legal certainty. Thematic working group based studies similar to the EC Open Science Monitor case study on open hardware licences[106] should be included in this scope, but provide a focus on the industrial consequences of uncertainties for start-ups and SMEs.

In these projects, metrics should be created to measure the impact of OSH projects and continue to inform stakeholders through roadmaps, newsletters, workshops, conferences, and further forms of communication, knowledge sharing and knowledge transfer. A repository that maintains information pools (containing open tools, open PDKs, best practices, open data, IP, etc.) should be generated within these efforts and implemented in an easily accessible and identifiable manner.

104. Licensing support is, for instance, given at universities such as **ETH Zurich** when it comes to licences for EDA tools.
105. Data should be publicly accessible, e.g., in the scope of **Eurostat**.
106. Murillo et al. (2019). **Open Hardware Licences: parallels and contrasts**. Open Science Monitor Case Study for the EC.

CONCLUSIONS

In conclusion, embracing the open source approach within the domain of semiconductor and processor technologies holds immense potential across various sectors. The benefits for academia and education will amplify innovation and collaboration, resulting in accelerated advancements in Europe's semiconductor R&D. Enhanced hardware security through transparency, collective scrutiny and contribution will bolster the robustness of technologies as well as societal trust.
Moreover, the bottom-up industrial reinforcement intensified modularly through open source silicon will empower smaller players in Europe and significantly diversify the value chain. These opportunities, in turn, will be decisive for strengthening the resilience of the European industry and value chain and for collaborating with like-minded allies to better overcome difficulties and bottlenecks together.

To fully realise these opportunities, however, it is imperative to channel EC funding and initiatives and bolster research capacities towards the open source silicon landscape and open science. They need to approach open questions and needs concerning the gap between academia and industry, and support start-ups and SMEs strongly and early on.
Moreover, the active engagement of underrepresented groups, particularly women in the semiconductor industry must be proactively initiated and realised. By cultivating an inclusive environment, Europe can draw on a larger pool of talent and a change of perspectives that breaks down current barriers to enter the field.

Once these challenges are mastered, the open source silicon approach has great potential to reshape Europe's domain of semiconductor and processor technologies – unlocking innovation and strengthening industrial resilience.

BACKGROUND OF THE EXPERT OPINION

The knowledge production process underlying this policy brief involved desk research, semi-structured expert interviews and webinars. The following experts were involved in this consultation and collaboration process (in alphabetical order):

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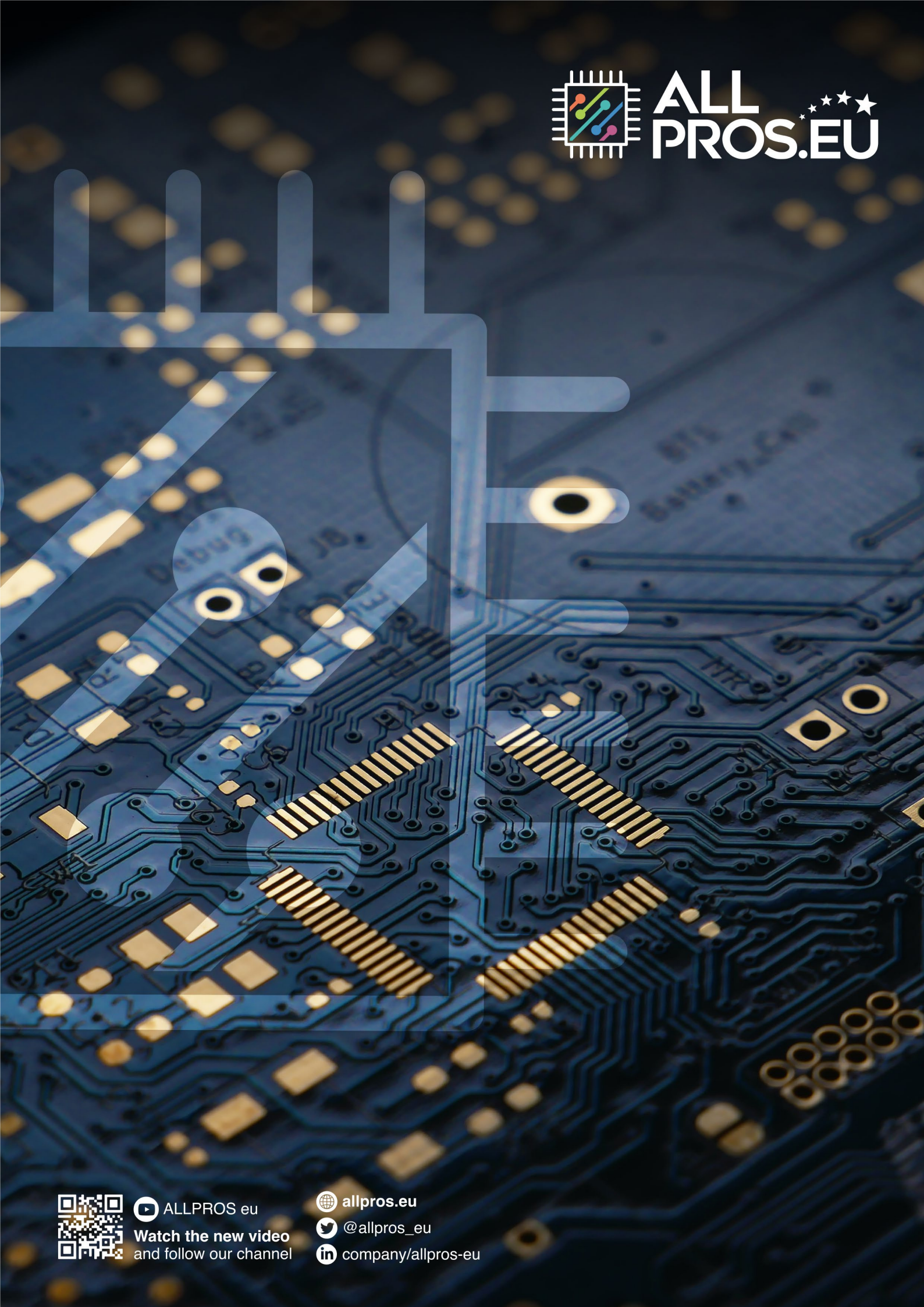
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