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# FPGA Based Efficient OFDM Based Design and Implementation for Data and Image Transmission for Healthcare

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***Abstract:*** ***Enormous growth in telecommunication industry demands for high speed data transmission with better quality of service (Qos). The telecommunication networks are offering the services which is from 1 Mbps to several Mbps of speed. However, most of the existing techniques address to assure the very high speed data for multimedia communication. The multimedia data may find a suitable application in healthcare system. The OFDM modulation technique promises to provide the multimedia services at rather high speed using the spectrum more efficient compared traditional scheme like TDMA, FDMA. The orthogonality of carriers eliminates the interference among the closely packed carriers and offers comparatively efficient bandwidth. The OFDM design requires choosing proper parameter selection. Important feature of OFDM is that the multipaths are effectively eliminated by choosing a higher cyclic prefix values which, gives significant results but causing more energy loss. This paper presents an efficient design for OFDM transceiver by using FPGA. The design is modeled and simulated using Matlab Simulink and finally the design is coded using Verilog RTL and simulated in modelsim and synthesizing and implementation is done using in Xilinx EDA tool. The image type of data is taken for transmission in the proposed OFDM transceiver system. The received image type data achieves PSNR value of 29.920dB and the binary input data achieves 36.06% improvement in power utilization and less area overhead. The paper also shows the improvement in area and power compared to existing authors.***

***Keywords: FPGA, High Speed, OFDM, Power Optimization, Healthcare.***

## I. INTRODUCTION

The growth in wireless industry justifies the necessity for multimedia transmission at much higher speed [1]. Existing services offered by wireless companies range from voice to data. The speed of the data services range from few kilobytes to Megabytes. The high speed data is useful for the transmission of image and data [2]. The demand for high speed communication requires many techniques, one of such technique is multicarrier modulation, which is commonly used for multimedia data transmission schemes and the physical layer implementation of data transmission for WiMAX network [3].

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The multicarrier modulation divides the data into smaller chunks of data and these small chunks can be modulated individually using a carrier signal [4]. The multicarrier modulation has many significant features such as delay spread avoidance and improved spectral efficiency. The research addressed that OFDM is a popular choice for broadband networks [5]. The implementation of FFT and IFFT implementations is the main challenge due to the complexity of the algorithm which has many additions and multiplications to be done in small time. DSP chip and FPGA hardware are considered as the design implementation platforms for various FFT/IFFT algorithms [6]. The data processing speed which is needed by the VLSI technology offered bye the use of FPGA which has features like the full environment for implementation of PSoC [7]. The FPGA composed of millions of configurable logic blocks and other etc blocks for the RTL implementation that makes promising answers for prototyping the ASIC using the dedicated architectures resources for specific DSP applications [8]. The challenge for the research community is to focus on optimizing the VLSI desings with respect to area/time. The existing mthods for improving the design speed includes pipelining, re-timing, parallel processing etc., The paper highlights on an FPGA based improved OFDM transceiver design, may be suitable for data/image transmission which finds application in healthcare. The performance of the system which is proposed in this paper is evaluated and compared with the research work published to come to a conclusion that the proposed systems effectiveness in area and power. The paper contains following different sections which includes background of the OFDM and Survey of existing research. The paper also discusses the problem statement, also the design and implementation of the system proposed and finally the results analysis.

## II. BACKGROUND

The current section evolves with discussion of OFDM concept which includes overview of OFDM, OFDM transmitter, OFDM receiver and issues associated with OFDM.

### A. Overview of Orthogonal Frequency Division Modulation (OFDM)

The OFDM is a multicarrier modulationr transmission scheme. The OFDM is a process of division of spectrum which results into many carriers and each of the carrier is modulated at lower frequency rate.

The spectrum representation of Frequency division multiplexing (FDM) is given in Figure.1. In FDM, the subcarriers are non-overlapping by which demands higher bandwidth [9].

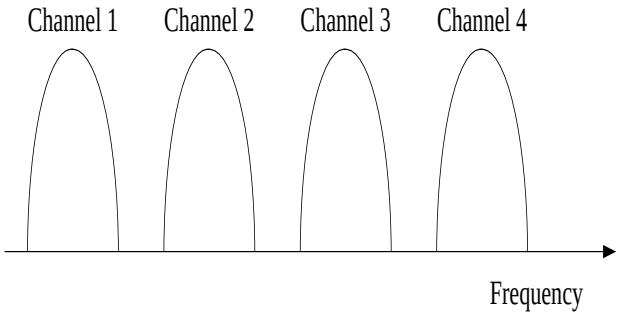


**Figure.1. Spectrum of FDM**

The OFDM spectrum is represented in Figure.2 with overlapping. The OFDM is very similar to FDM technique but the way its efficient interms of spectrally by placing the sub-channels carriers much closer. The position of sub carriers are done by selecting the frequencies which are in orthogonal to each other [10].

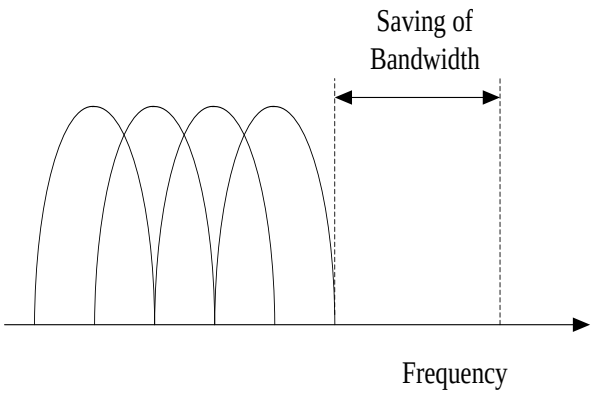


**Figure.2. Spectrum Overlaps in OFDM**

The orthogonality is meant for both the functions of real and complex values. The functions Nm(t) and Nn(t) are orthogonal over the interval p < t < q if they satisfy the condition:

$$\int_{p}^{q} N_m(t) N_m^*(t) dt = 0, \quad where \ \ n \neq m$$

The OFDM performs the splitting of the bandwidth as narrowband channels with its sub-carrier which are made orthogonal to each other. Thus, each subcarrier spectrum exhibits null in center frequency of every other sub-carriers in the system and is expressed in Figure 3 below.

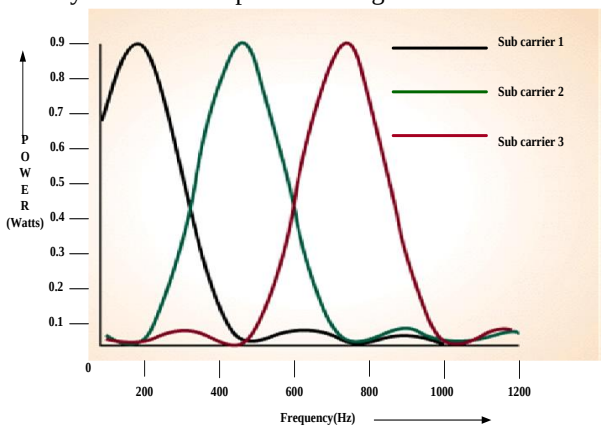


**Figure.3. Orthogonality of Sub-Carriers**

This leads no interference among the sub-carriers causing spacing theoretically possible. Due to this, there is no overhead associated with switching between users [11]. This helps to overcome overhead carrier spacing issues of FDMA.

### B. OFDM Transmitter and Reciever

The OFDM is a multi-carrier modulation mechanism that divides various spectrums into many carriers and each of the carrier will be separately modulated with low data rate signal. The OFDM exhibits similar features like FDMA where the access to many users can be attained by subdividing the available bandwidth to multiple channels This can be attained by keeping all the carriers orthogonal to one other, preventing interference [12]

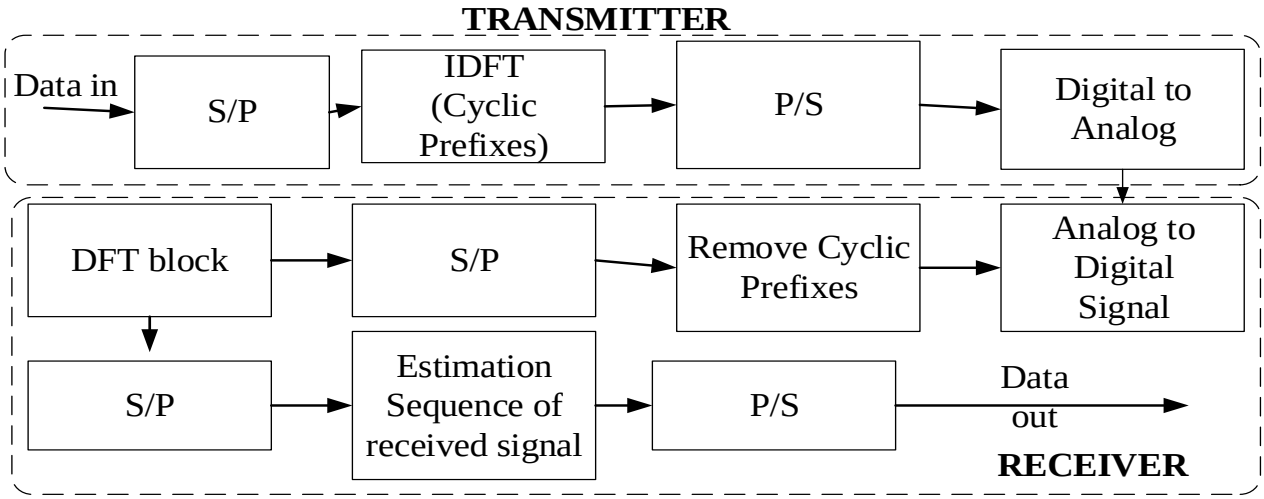


**Figure.4. General OFDM Transceiver System**

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OFDM Significance:
The OFDM has much important features [13, 14] than other modulation schemes and are highlighted below:

- The *bandwidth efficiency* is the main reason for high speed communication. In wireless communication the bandwidth can be shared by all the devices expected to share the crowded range of carrier channels. Due to orthogonality nature of OFDM, total bandwidth is reduced by 50%
- ISI causes problem in *high speed transmission*. The OFDM assists to transmit with at high data rate.
- The OFDM helps to spreads a various frequency selective fade over symbol period. The OFDM helps randomizes the *burst errors* caused by *deep fade*.

## III. RELATED WORK

The work of [15] focusses on the design of IFFT algorithm for OFDM system. The design was implemented using a Matlab. Above author implemented the design over a FPGA Spartan 3A and the results found to be effective. Similar work was done by [16] for OFDM design using the radix 2 point decimation FFT/IFFT. The design was implemented using Verilog code and simulated using altera modelsim. The exhaustive review on OFDM for data/image transmission for various applications and research gaps are addressed and the implementation of FFT algorithm for OFDM transceiver is presented in Vasanth kumar and k V Prasad [17].
The system design is improved for area and speed. The outcomes suggest that the system achieves higher speed and low area. The work introduced by Vasanth kumar [18] discussed the study on transmitter and receiver of OFDM system. The design is implemented over Spartan 3A kit and used VHDL language for coding. The results indicated the optimized and efficient results.

## IV. PROBLEM STATEMENT

The OFDM design needs a exhaustive and full knowledge on selecting the critical parameters. The most important feature of OFDM is that due to the nature of subcarrier level modulation with low frequency, the multipath fading is eliminated due to the increase of symbol duration, because of which more number of Cyclic Prefix (CP) bits are needed. This causing more energy losses. Therefore, there is a need of correct OFDM design concept [19, 20]. For the same concern many researchers explored various OFDM transceiver designs by implementing the various algorithms in conventional manner [21]. From the survey of existing research trend in OFDM it is observed that many of the mechanisms follows the software or c language based approach which may not be significant for real time application areas in wireless based systems, WIMAX. It is found that very less proven architecture are present on hardware. These hardware architecture are designed based on OFDM and are known to have many designs constraints such as area and power overhead. The existing architecture uses Local oscillator for frequency conversion which is analog based. To overcome all these issues digital approach which requires RF conversion which needs frequency synthesizer in digital approach.

## V. PROPOSED SYSTEM

To improve in the analog RF communication system, effificent OFDM design is achieved using Verilog coding language and implemented over a FPGA platform the performance evaluation. The different blocks of OFDM transmitter and receiver is shown in Figure 5. The figure has both transmitter and receiver blocks for the data transmission. Main components of the transmitter are the IFFT, QAM modulation and Digital up converter modules. The receiver block has FFT, QAM demodulation and Digital downconverter as the main modules. The input data travels through transmitter and receiver blocks. The proposed architecture implements Pipelined 8 point 16bit FFT. The study also implements the Upconverter and downconverter using the DFS(Digital frequency sysnthesis) approach.

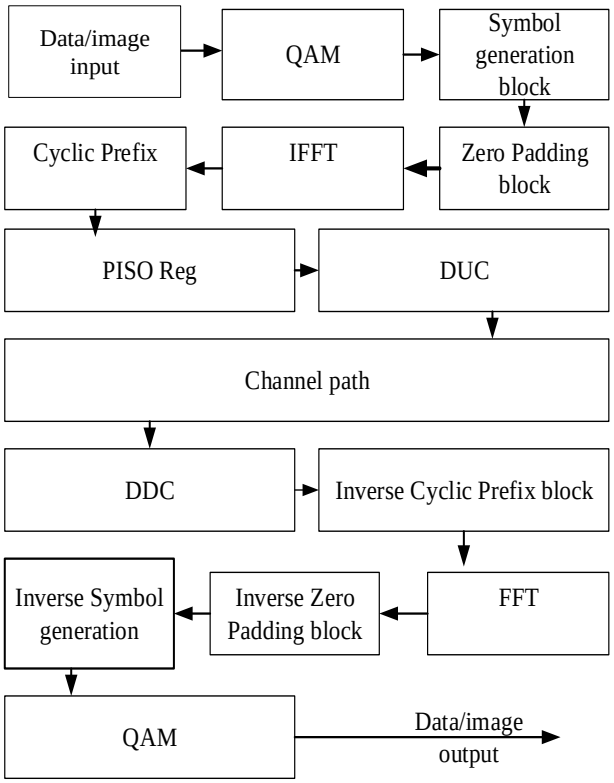


**Figure.5. Architecture of Proposed System**

*Transmitter:* This design needs a clock of 100Mhz.Different clock frequency are achieved by dividing the global clock which is needed by different blocks in transmitter and receiver. The 16 QAM modulation is used for the input data. The output would be of inphase and quadrature data. The next module in the transmitter takes the output of 16bit from the modulation and gives 64bit of symbol data. Zero padding is necessary to generate 12b bit of complex data. The IFFT module performs the inverse fourier operation on 16bit data and the results are stored in 8bit register. So there will be a 128 bits of real and imaginary data outputs from IFFT. A cyclic prefix of 8bits to 48bits are added to the output of IFFT. The output of added cyclic prefix data are sent over the air using PISO. The operation of Upconvereter is to convert basedband data to number of passband data.

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*Receiver:* Upconverter or the Downconverter block consit of Frequency synthesizer which performs the operation digitally which is efficient compared to analog synthesizer. This module generates sine and cosine singlas based on input angle data. The sine and cosine signals are multiplexed with multipliers to give upconverter and downconverter data. The upconverter block is shown in figure 6. The Digital frequency synthesizer architecture consists of multipliers, adders and multiplexers. Different inputs such as xi,yi and angle are fed to the synthesizer architecture. Outputs of sine and cosine signals are obtained along with the register data. Later sine and register data are multiplied to give upconverter data.

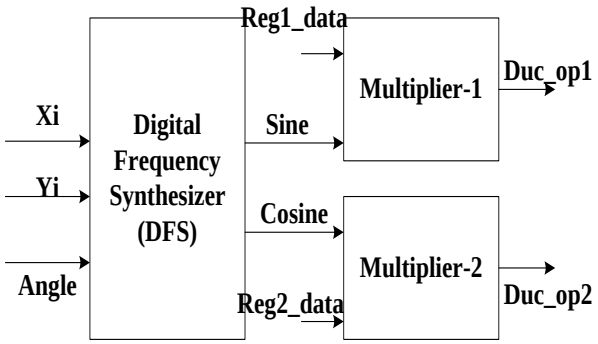


**Figure 6 Upconverter Module**

The specification table of the OFDM design is shown in Table.1.

**Table.1. OFDM Design Specification**

| Channel Bandwidth BW | 4 MHz |
|---|---|
| Image size | 256x256 |
| Modulation | 16-QAM |
| FFT size | 256bits |
| Cyclic Prefix size | 48bits |
| Bit rate Fb | 16Mhz |
| FFT size | 256 |
| Pilot carriers | 8 |
| Data carriers | 192 |
| Nulls | 56 |
| Maximum number of symbols | $1x10^6$ |
| Total number of errors | 500 |

## VI. RESULTS DISCUSSION

The OFDM T design consist of Transmitter and receiver, Upconverter and Downconverter Modules. The clock frequency taken for the design is at 100MHz..The design is synthesized in Xilinx ISE EDA tool using Verilog and simulated using Modelsim and implemented over Virtex 5 FPGA Board. The clock period is 10ns. The asynchronous reset is used and kept initial high to reset the process.. The valid input is always high in all the stages. The input data taken is data/image and output data/image is obtained after the data/image passing through all the receiver blocks. The following Figure.6, represents the input image at the transmitter block and the output image received with PSNR of 29.920dB after the image data is passed through all the OFDM blocks. The input and output images are compared to obtain a PSNR 29.920 DB and MSE = 66.091. The execution time to complete the process is 1.31ms. The quality of the image will be satisfactory based on the above PSNR value in standard OFDM Systems. Above results are achieved when passing a input data through a OFDM transceiver system developed using Matlab Simulink and the parameter chosen for simulating the design are given Table 1.

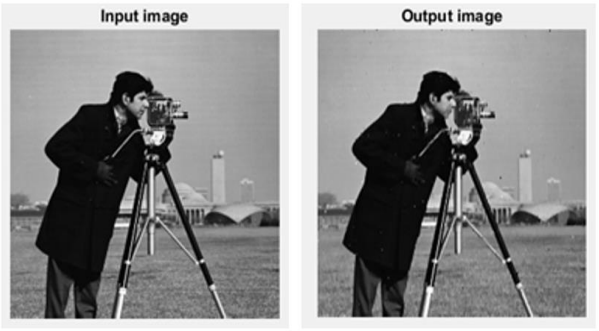


**Figure.7. Input and Output Image- with PSNR = 29.920 dB**

The proposed OFDM system is implemented using Verilog HDL code and simulated using modelsim. The Table 2 shows the utilization of the proposed OFDM system

**Table 2: OFDM System Transmitter Utilization**

| Logic Utilization | Used | Available | Utilization |
|---|---|---|---|
| Number of Slice registers | 995 | 126800 | 0% |
| Number of Slice LUT's | 5266 | 63400 | 8% |
| Number of fully used LUT-FF pairs | 575 | 5686 | 10% |
| Number of Bonded | 23 | 210 | 10% |
| Number of BUFG/BUFGCTRLS | 3 | 32 | 9% |
| Number of DSP48E1s | 16 | 240 | 6% |

The proposed system also exhibits a lower power of 1.201W compared to the work [22]. The results shows that the proposed system design is power optimized with a value of 36.08% improvement and the same is recorded in Table3.

**Table 3: Analysis of Power Consumption Comparison**

| Utilization of power | Existing [22] | Proposed | Improvements |
|---|---|---|---|
| Total Power | 1.8W | 1.201W | 36.08% |

The proposed system design OFDM receiver utilization is tabulated in table.4. From the Table.4, it is found that the less resources are used and the percentage of resource utilization is mentioned in the table.

**Table 4: OFDM System Receiver Utilization**

| Logic Utilization | Used | Available | Utilization |
|---|---|---|---|
| Number of Slice registers | 1121 | 126800 | 0% |
| Number o Slice LUT's | 3777 | 63400 | 5% |
| Number of fully used LUT-FF pairs | 271 | 4627 | 5% |
| Number of Bonded | 23 | 210 | 10% |
| Number of BUFG/BUFGCTRLS | 4 | 32 | 12% |
| Number of DSP48E1s | 16 | 240 | 6% |

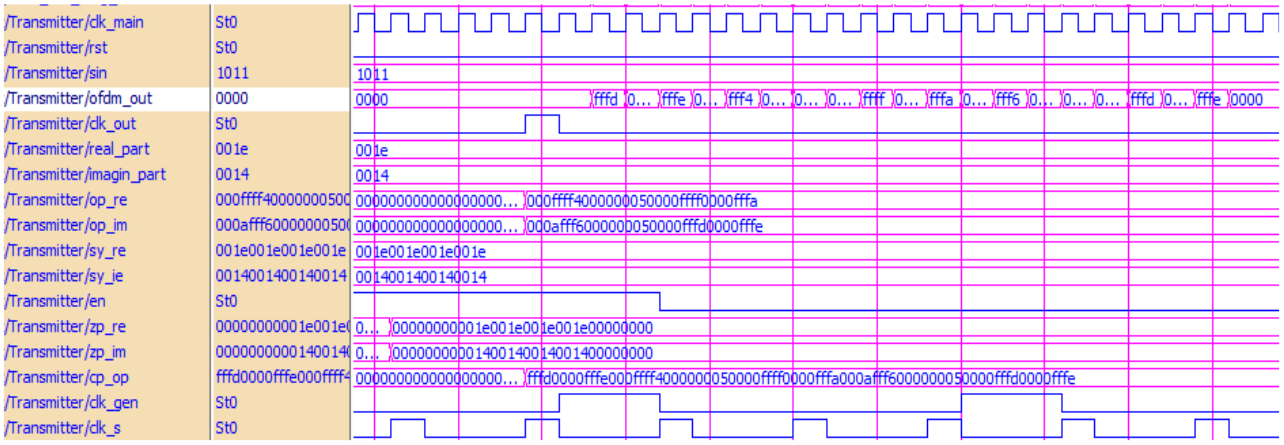


**Figure 8: Proposed OFDM Transmitter Simulation Output**

Figure 8 and Figure 9 shows the simulated output of OFDM transmitter and OFDM receiver respectively.

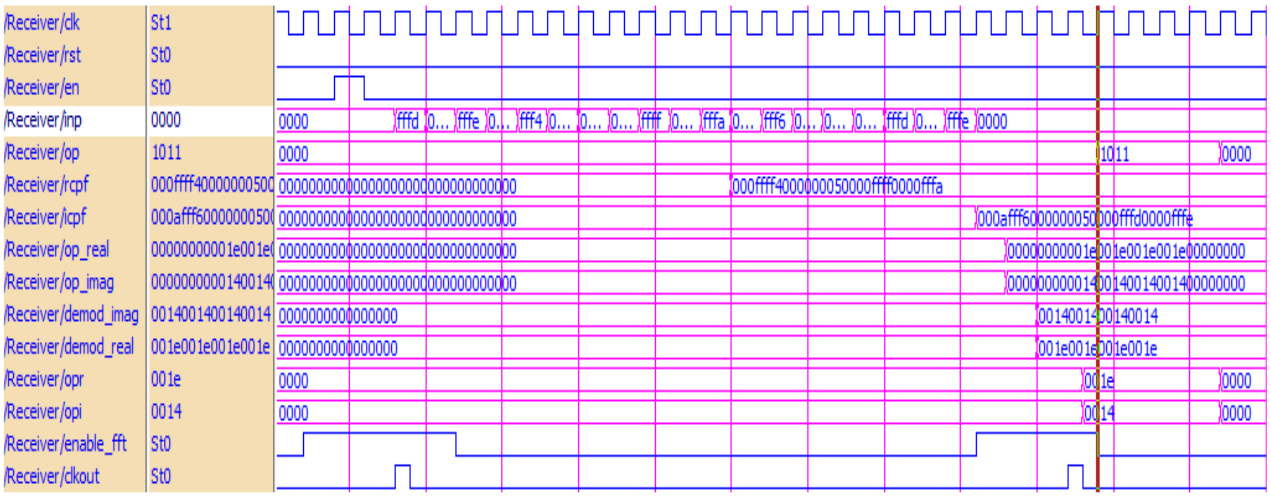


**Figure.9. Proposed OFDM Receiver Simulation Output**

## VII. CONCLUSION

The tremendous growth in communication industry allowed multimedia communication to demand the quality of service for data/image transmission at higher speed. The challenge to optimize VLSI circuit in terms of area and power are always a research oriented. The existing conventional techniques for improving the design speed on FPGA involve pipelining, re-timing, parallel processing etc., Therefore to provide high speed data/image communication for healthcare applications, this paper presents the OFDM Transceiver design which mainly consist of Transmitter, receiver, Upconverter and Downconverter Modules. The design is implemented over FPGA platform and synthesized in XILINX EDA tool using Verilog coding language and simulated using Modelsim6.3f and Implemented on Virtex 5 FPGA Board. The transmitted image achieves PSNR value of 29.920dB and MSE of 66.091 with execution time of 1.31ms. This quality of the image be satisfactory based on the above PSNR value in standard OFDM Systems. of the OFDM systems on FPGA hardware. The paper also presents a resource utilization summary of OFDM transceiver system. The results obtained from the proposed system achieved total power reduction and less hardware complexity.

## DECLARATION

| | |
|---|---|
| Funding/ Grants/ Financial Support | No, I did not receive. |
| Conflicts of Interest/ Competing Interests | No conflicts of interest to the best of our knowledge. |
| Ethical Approval and Consent to Participate | No, the article does not require ethical approval and consent to participate with evidence. |
| Availability of Data and Material/ Data Access Statement | Not relevant. |
| Authors Contributions | I am only the sole author of the article. |

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**Vasanth Kumar T. R**. completed his Bachelor of engineering (BE) from the University of VTU, India, and his Masters from the VTU University. Completed the Ph.D. in the field of VLSI/FPGA Research areas includes Wireless Communication FPGA, 4G/5G. He has over decades of experience working on wireless/networking technologies. He has worked with number of organizations in the past. Author is tied with number of organizations for collaboration work.