NEXCODE: Next Generation Uplink Coding Techniques

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***Abstract*—NEXCODE is a project promoted by the European Space Agency, aimed at research, design, development, and demonstration of a receiver chain for telecommand links in space missions, including the presence of new short low-density parity-check codes for error correction. These codes have excellent performance from the error rate viewpoint but also put new challenges as regards synchronization issues and implementation. In this paper, after a short review of the results obtained through numerical simulations, we present an overview of the breadboard designed for practical testing and the test-plan proposed for the verification of the breadboard and the validation of the new codes and novel synchronization techniques under relevant operation conditions.**

Keywords—Low-density parity-check codes, space missions, telecommand.

I. INTRODUCTION

The only error correcting code currently included in the Consultative Committee for Space Data Systems (CCSDS) recommendation [1] and in the European Cooperation for Space Standardization (ECSS) standard [2], for telecommand (TC) synchronization and channel coding, is a Bose-Chaudhuri-Hocquenghem (BCH) code with codeword length $n = 63$ bits and information vector length $k = 56$ bits. This code has very poor error rate performance, because of limited coding gain, but, as a counterpart, it offers good error detection capabilities. These features have been considered satisfactory for many years, since they are able to comply with the TC link requirements put by the currently flying and upcoming missions.

Nowadays, however, the need to increase further the coverage and/or the uplink data rate has aimed the Next Generation Uplink (NGU) initiative [3], promoted by the CCSDS with the goal to define improvements to the existing TC recommendations, this way complying with new mission requirements. In this view, identifying more powerful codes is a central element of the upgrading effort. After a long discussion, that has involved as possible candidates a number of different error correcting codes, there is now a general consensus towards the adoption of two short binary low-density parity-check (LDPC) codes, both characterized by rate $R = 1/2$: the first one has $k = 64$ information bits and the second one $k = 256$ information bits.

The Next Generation Uplink Coding Techniques (NEXCODE) project, funded under the Technology Research Program of the European Space Agency (ESA), is aimed at research, design, development, and demonstration of a TC receiver chain for scientific missions, including these new channel codes. Among the project objectives we can mention:

- Clarify the impact of the new codes in terms of:
  - needed protocol modifications;
  - on-board (O/B) receiver algorithms, that is, acquisition and tracking of uplink signals at lower signal-to-noise ratio (SNR), determined by higher coding gain;
  - O/B receiver architecture, to cope with extra complexity and/or new algorithms.
- Prototype the O/B receiver chain core elements, including the decoder for the advanced coding schemes and the novel synchronization algorithms, by means of commercial hardware (HW), e.g. field programmable gate array (FPGA), to help validating the approach and minimize the risk of adoption, bringing the technology readiness level (TRL) up to 3-4.
- Evaluate the most relevant metrics, e.g., the effective coding gains, and the performance/complexity trade-off.

The NEXCODE project has assumed two different application scenarios, representative of near Earth (NE) and deep space (DS) missions: for the former, the enhanced coding gain has been used to enable higher data rates; for the latter, conversely, the gain has been used to increase the maximum communication distance, with very low data rates. The DS scenario has revealed to be the most demanding one, in terms

of the impact on the overall receiver functionalities.

It must be said that, according to the project's targets, very stringent requirements have been set on the codeword error rate (CER) and the undetected codeword error rate (UCER), namely: CER $\leq 10^{-5}$ and UCER $\leq 10^{-9}$. Actually, as commands are sent in the payload of TC transfer frames, the error rate requirements could be specified in terms of frame error rate (FER) and undetected frame error rate (UFER), where a frame may be composed by more codewords. These quantities are obviously related to the previous ones; in this paper, however, CER and UCER have been adopted for clarity reasons.

In the first phase of the NEXCODE project, we have simulated the error rate performance of the new error correcting codes under different decoding algorithms and practical constraints (e.g., by considering the effect of quantization).

Then, the impact of the new coding techniques on affected spacecraft (S/C) sub-systems has been assessed, in order to identify the changes required to take advantage of the potential benefits, i.e. increased coding gain, resulting in a lower operating SNR. In particular, the receiver design, including acquisition and tracking loops for carrier/sub-carrier/symbols, has been addressed in order to cope with the lower SNR.

Potential changes to the O/B architecture have been also investigated, with the aim of an optimization of the overall receiver from power, complexity, flexibility and reliability point of view. Backwards compatibility has been addressed, assessing the feasibility of a (configurable) design compatible with both existing BCH standard and the newly proposed codes.

The project is now in its second, and more substantial, phase, which consists in the realization of a breadboard of the core elements of the O/B receiver, able to demodulate and decode uplink signals employing the new codes. The implementation and testing of such a hardware proof-of-concept is expected to help validating the approach and minimizing the risk of adoption of the new codes for future missions. The use of the breadboard should also be instrumental in the promotion of the new coding techniques within the standardization bodies.

The object of this paper is to describe the advancement in the HW/software (SW) implementation of the breadboard and the test-plan for its validation and verification.

The organization of the paper is as follows. In Section II, we report some basic results on the simulated performance, in terms of both the error rate and the synchronization error probability. In Section III, we present the breadboard design and we make some realization considerations, whose validation is based on the test-bench approach described in Section IV. Finally, Section V concludes the paper.

II. Error Rate and Synchronization Properties

The new LDPC codes can be decoded by a number of different decoding algorithms. Among them, the most classic ones are those based on iterative procedures, like the sum-product algorithm (SPA) [4], typically implemented using log-likelihood ratios (SPA-LLR), or its simplified versions, e.g., min-sum (MS) [5] and normalized min-sum (NMS) [6]. Through the project, however, we have had the opportunity to check applicability of a different, non-iterative approach, based on ordered statistic decoding (OSD) [7]. By using an instance of the OSD, commonly known as most reliable basis (MRB) algorithm, we have verified that significant additional coding gains can be achieved, with respect to the iterative algorithm, in the case of the LDPC(128, 64) code. On the contrary, effective application of the MRB algorithm to the LDPC(512, 256) code is too complex, while a simplified version does not allow to achieve significant gains. In order to limit complexity, for both the short and the long codes, that is the main drawback of the MRB algorithm, we have also proposed to use a hybrid approach which consists in assuming the iterative decoder as the main decoder, invoking the MRB decoder only when the iterative algorithm fails, that is, it is not able to find a valid codeword. However, also with the hybrid approach, an effective implementation of the MRB algorithm for the LDPC(512, 256) code remains unfeasible.

To confirm the statements above, Figure 1 shows the CER performance of the NMS algorithm and the hybrid algorithm for both codes, as a function of E_s/N_0, where $E_s = E_b/2$ is the energy per channel symbol (i.e., after encoding, E_b being the energy per bit) and N_0 is the one-sided power spectral density of the thermal noise.

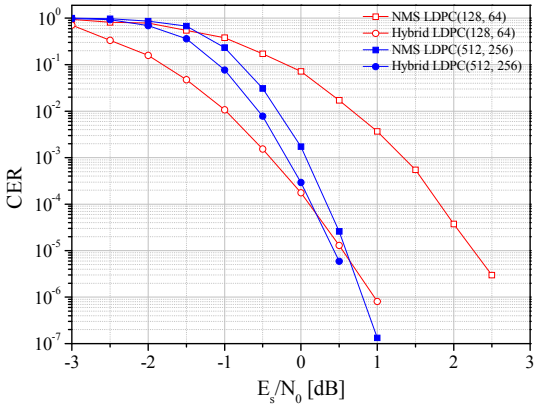

Fig. 1. CER performance of the considered LDPC codes under different decoding algorithms.

From the figure we see that a reduction of E_s/N_0 in the order of 1.7 dB can be achieved at CER = 10^{-5}, for the shorter code, when using the hybrid algorithm instead of the NMS algorithm. Implementation of the hybrid approach for decoding of the LDPC(128, 64) code is one of the challenges of the present project since, at our knowledge, no example of practical realization has been presented till now.

On the contrary, for the longer code, the extra gain offered by the hybrid approach, for the same CER, is almost negligible. The error rate performance of the LDPC(512, 256) code could be further improved by extending the hybrid algorithm, but at the cost of an unacceptable complexity. So, we can conclude that, for the longer code, it is convenient to use the NMS algorithm.

We remark here that the LDPC(512, 256) code remains preferable, in terms of FER, in the case of long frames, as it allows a reduced segmentation (i.e., a smaller number of codewords). Moreover, its UCER/UFER performance is particularly favorable.

In fact, as regards the UCER performance, preliminary evaluations confirm that the LDPC(512, 256) code, decoded by using the NMS algorithm, satisfies the target of 10^{-9} at the expected working point, that is, $E_s/N_0 \approx 0.6$ dB. For the LDPC(128, 64) code, it is possible to verify that the target can be reached by using the NMS algorithm at $E_s/N_0 \approx 2.2$ dB, that is the value needed to satisfy the requirement on the CER. On the contrary, for the MRB algorithm (and, by extension, also the hybrid algorithm) the target can be reached, without increasing the value of E_s/N_0 compliant with the CER, only by using a cyclic redundancy check (CRC) code. Actually, the CRC is already included in [1] (as an option) and in [2] (mandatory). By using it downstream the MRB decoder, we have estimated an UCER $< 10^{-9}$ at $E_s/N_0 = 0.5$ dB, that is close to the value needed for satisfying the requirement on the CER when using the hybrid algorithm. Details on the UCER estimation procedure can be found in [8].

Figure 1 shows that by exploiting the coding gain, very small values of E_s/N_0 are required. So, signal acquisition and tracking will potentially operate at SNRs much lower than those currently expected, and this, depending on the configuration, may prove extremely challenging. More precisely, this requires a revision of the current architecture and operation of the legacy TC receiver, and the identification of receiver processing bottlenecks for DS and NE scenarios. For example, in tracking mode, the main modules in the receiver are: a carrier tracking block, typically implemented by a phase lock loop (PLL); a subcarrier tracking block when necessary, typically implemented as a Costas loop; and a symbol timing tracking, implemented as a data transition tracking loop (DTTL). These three tracking loops initiate their operation after the signal has been detected and acquired, process referred to as *acquisition mode*. All these receiver functionalities require revision, evaluation, and eventual enhancements when the operating SNR is decreased thanks to the new coding gain. These modules have been designed under much more benign conditions. Enhancements include reduction of the loop bandwidth, in order to diminish the noise contribution to the tracking loops. This is in contrast to having a sufficiently large loop bandwidth to accommodate the dynamic of the signal, e.g. Doppler and Doppler rate. A suitable technique to accommodate the latter is to improve the signal acquisition via a fast Fourier transform (FFT) processing of the signal.

After having accomplished the time and frequency synchronization, the frame synchronizer has to determine the correct position of the start sequence which marks the start of the communication link transmission unit (CLTU). Since this operation is considerably more challenging at lower SNR, one of the objectives of the project has been to evaluate the frame synchronization error (FSE) probability and to eventually propose an improved solution.

In contrast to the case of a periodically inserted sync marker, in which the receiver searches for the most likely position within one frame, in the present case, synchronization has to be achieved before reception of the entire CLTU, whose length is variable and unknown a priori.

For this reason, it is necessary to resort to one-shot frame synchronization which compares, for each position of the observation window, the computed metric to a pre-defined threshold in order to decide if the current position corresponds or not to the start of the CLTU. In this scenario, two types of error may occur:

- False alarm: The metric exceeds the threshold, but the samples in the observation window do not correspond to the start sequence.
- Missed detection: The start sequence is in the observation window, but the metric is below the threshold.

Figure 2 shows the behavior of the FSE probability as a function of E_s/N_0 for different metrics and two lengths N of the start sequence. While the meaning of hard/soft correlation is well known, the simplified likelihood ratio test (S-LRT) uses a near-optimum metric [9], derived as outlined in [10], the latter providing the optimum approach. A start sequence length $N = 16$ bits corresponds to the current standard, and from the figure we see it provides quite unsatisfactory performance. On the contrary, by adopting $N = 64$ bits, at $E_s/N_0 = 0.5$ dB, we have FSE $< 10^{-3}$, which is a reasonable requirement, for any choice of the metric, the S-LRT being the best. This confirms the need, with the new codes, to lengthen the start sequence up to 64 bits, which is another issue currently under discussion, in view of the standard updating.

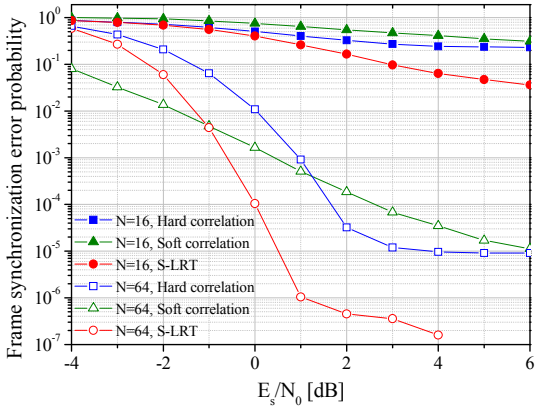

Fig. 2. FSE probability with hard and soft correlations and with the S-LRT for the original 16-bits and a 64-bits start sequence.

After detecting the CLTU start, blocks of n bits are decoded. The number of blocks is unknown, since the commands have variable length. Then, the receiver has to recognize the CLTU end. This is another issue that the new standard shall change, as the "uncorrectable pattern" approach, currently used, cannot be applied with the new codes. (This approach currently requires the BCH decoder to mark a block including the tail sequence as uncorrectable, because the error correction capability has been overdone. Since the new codes are very powerful, this approach becomes very difficult and infeasible.)

The approach we have chosen in NEXCODE is the application of a detector, which looks for the 64-bits tail sequence after each codeword. Like for the start sequence detection, we have applied different metrics, searching for a solution which permits us to have a probability of false alarm, P_{fa}, and a probability of missed detection, P_{md}, sufficiently small, e.g., both lower than 10^{-6}.

Figure 3 shows the behavior of P_{md}, as a function of E_s/N_0, for $P_{fa} = 10^{-6}$. Also in this case we see that the target can be reached at $E_s/N_0 = 0.5$ dB. In particular, the simplified Massey detector [11] provides a performance very close to the optimal LRT one, but with limited complexity. In addition, the Massey metric and S-LRT metric used for the start sequence detection are equivalent and they can share architectural implementation in the breadboard.

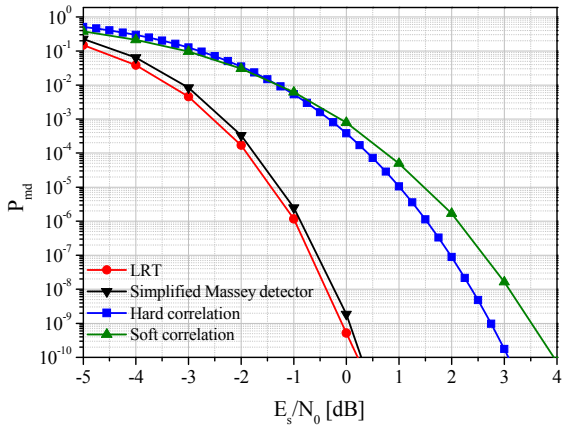

Fig. 3. P_{md} vs. E_s/N_0 for $P_{fa} = 10^{-6}$.

III. Breadboard Realization Considerations

The study activity includes a HW proof-of-concept of the new advanced uplink coding techniques. For this purpose, a breadboard able to demodulate and decode uplink signals is under development. For the breadboard design, the current telemetry, tracking and command (TT&C) architecture and the optimizations required to incorporate the novel techniques must be considered; at the same time, the demonstrator goals, algorithm validation and performance evaluation are the main driver for the overall design.

The breadboard architecture is based on a System-on-Chip (SoC) approach fully contained in an FPGA device, where a microprocessor is embedded, performing digital signal processing (DSP) functions for TT&C transponder processing. The microprocessor interfaces all DSP blocks and all other peripherals through an on-chip bus, which allows it to control and configure every TC receiver processing unit. This approach offers the advantage of a configurable, modular and synchronous architecture, allowing portability, modification or addition of DSP cores, including compatibility with typical transponder platforms.

The breadboard architecture is presented in Figure 4, where the HW/SW partition of the different TC processing units is also shown.

This flexible platform permits to deal with different TT&C modulation standards and mission profiles, including both NE and DS scenarios requirements. The modular architecture allows incorporating the novel synchronization and decoding algorithms presented in Section II.

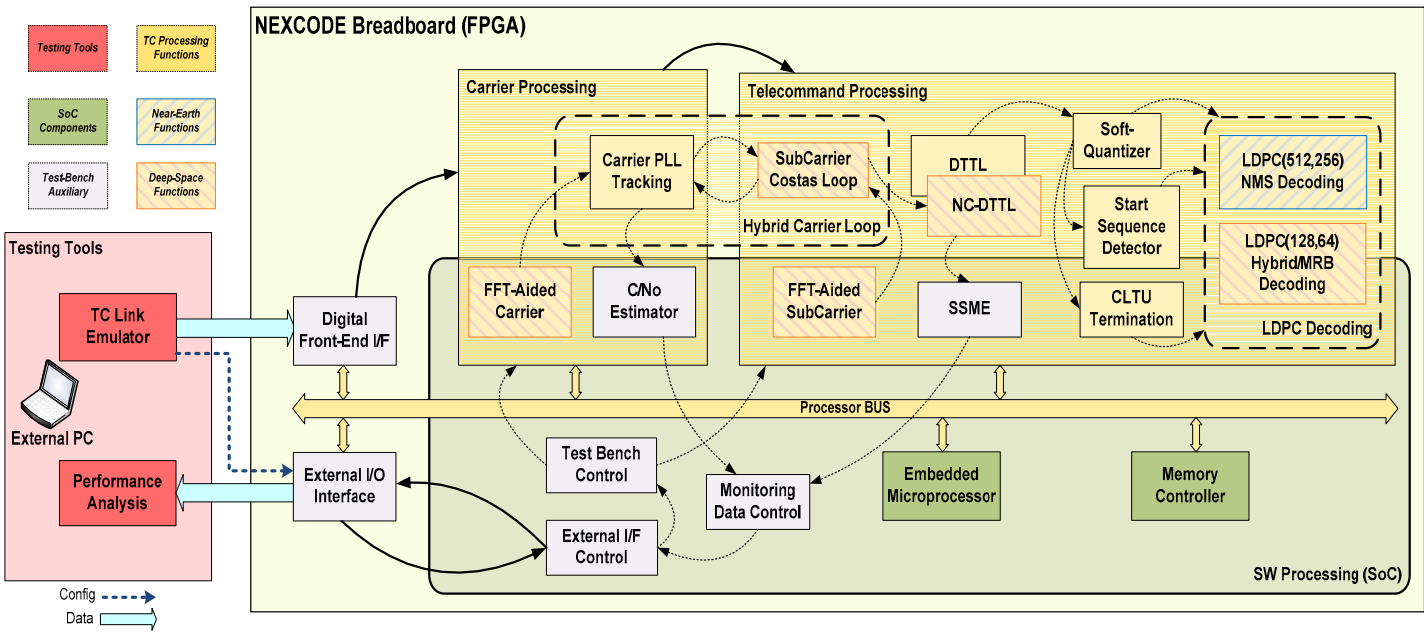

Fig. 4. High-level view of the breadboard architecture.

Starting from the signal acquisition and tracking, the identified enhancements include an FFT technique for aiding the carrier tracking. This FFT algorithm can be supported by SW processing that operates on the typical HW carrier processing unit outputs; therefore, the legacy TT&C HW architecture is reused.

The HW/SW combined processing is even more relevant for the DS missions typically characterized by low data rates down to tens of bps, providing the most demanding scenario for acquisition and tracking, i.e. the lowest SNR. A functionality to overcome signal synchronization bottlenecks in this scenario is the hybrid carrier loop algorithm or sideband-aided carrier recovery [12]. It uses the composite signal sidebands power to enhance the effective SNR in the carrier tracking loop bandwidth. The algorithm architecture is a combination of the carrier and subcarrier tracking loops scheme as shown in Figure 5.

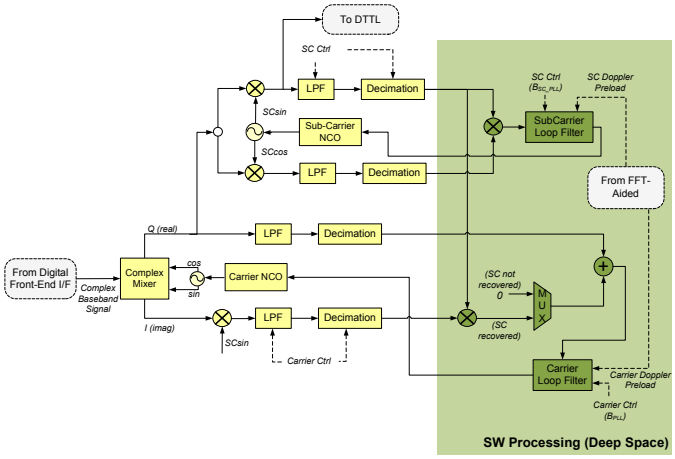

Fig. 5. Hybrid loop architecture for DS scenario.

After signal decimation, the signal can be managed by SW processing, that is in charge of the discriminator and loop filter whose output estimates are fedback to close the tracking loop.

Another proposed novel receiver configuration is the non-coherent (NC)-DTTL, which provides tolerance to phase loss in the subcarrier tracking stage [13]. It is based on the combination of two typical DTTLs, one block on each branch of the subcarrier quadrature components, as shown in the architectural diagram in Figure 6.

These are illustrative examples of novel synchronization functionalities that will rely on the flexible HW DSP processing available on standard TT&C platforms, while the enhancements are incorporated by adding new SW routines; thus, the developments validated in the prototyping breadboard could be easily adopted by standard TT&C platforms.

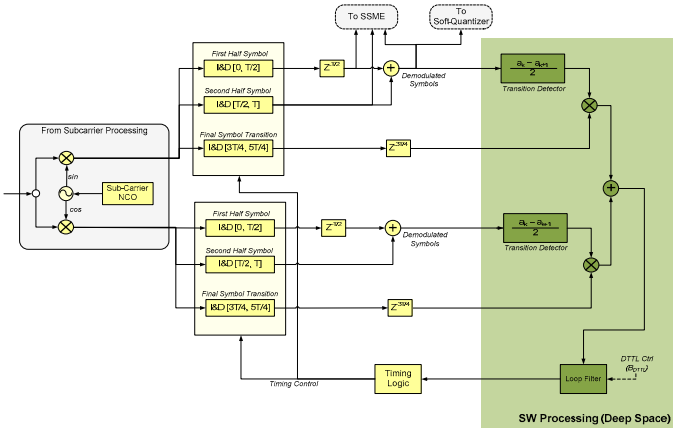

Fig. 6. NC-DTTL architecture for DS scenario.

Nevertheless, some of the new synchronization techniques and the new decoding algorithms require additional HW processing. The accommodation of these novel techniques in the TT&C platforms could be based on a dedicated FPGA as auxiliary board that will act as any other DSP core connected to the processor bus following the SoC approach. In this auxiliary FPGA, the DSP processing requiring HW resources will be implemented, and therefore these novel functionalities could be attached in any generic platform in future missions.

The proposed technique for CLTU start and end sequence detection will be accomplished with a shared HW processing unit, which will be in charge of a 64-bits pattern recognition based on S-LRT metric. This HW processor can be configured to detect CLTU start or end sequence depending on the TC reception stage.

As regards the decoding procedures, the NMS algorithm is necessary for both codes, while the MRB algorithm is part of the hybrid configuration proposed for the shorter code in DS scenario. The decoders logic works on the quantized soft values coming from the communication channel. The breadboard will serve to evaluate the impact of the quantization of these channel messages, considering a 3-bits quantization (for backward compatibility to the typical TT&C) and a 6-bits quantization that offers an additional gain of 0.3 dB. These channel messages are the input data for the HW decoder implemented in the FPGA, so the bit quantization analysis is critical to define the interface between the novel decoders and the standard TT&C platforms.

The NMS decoder architecture follows a partially parallel architecture, which is based on the parity-check matrix of the LDPC code and it takes advantage of the quasi-cyclic nature of these codes. A flexible HW architecture for NMS will allow the decoding of both LDPC(128, 64) and LDPC(512, 256) codes.

The MRB algorithm is necessary as part of the hybrid approach for decoding of the LDPC(128, 64) code. Due to the high complexity of the algorithm and the low symbol rate in DS scenario, a fully SW approach was foreseen initially. However, the algorithm profiling on the breadboard's microprocessor proves that a fully SW approach is not possible due to the large latency. In contrast, a mixed HW/SW

implementation is proposed for the breadboard. The SW part of the MRB algorithm can be in charge of matrix operations and vector reordering done at initialization once per codeword, while the HW parallelization can be exploited for processing the large number of binary operations needed for the most reliable candidate evaluation.

IV. Test-Bench and Validation Approach

The breadboard will be validated against the software simulator used for the novel synchronization and decoding algorithms evaluation during the first phase of the NEXCODE project. The CLTU generator and the channel emulator from the SW simulator will be used for synthetic signal generation as test inputs for the HW proof-of-concept. The realistic SW channel emulator can replicate front-end electronic impairments, S/C dynamic and channel propagation effects. These impairments can be controlled and configured according to the requirements of the test scenarios. Therefore, the test-bench can be reduced to a digital signal processing domain entirely contained in a single FPGA as described in Section III. A full digital implementation approach allows a completely controllable and faithful environment that is ideally suited for validation purposes.

The testing signals must be generated for a wide range of validation purposes. Functional validation, system integration tests, evaluation of specific TC processing components or end-to-end performance are some of the test cases that are planned. The different types of tests impact on the characteristics of the test signals to be generated, and it makes sense to assume the following categories for performance evaluation:

- *Synchronization algorithms evaluation tests*: focused on the carrier and subcarrier acquisition and tracking algorithms and symbol timing synchronization algorithms. Novel algorithms were proposed to overcome system bottlenecks, especially in DS scenario, and these novel algorithms must be validated on the breadboard. Few seconds of signals are enough for evaluation of phase synchronization techniques; while a small number of codewords are enough to validate the symbol timing recovery, since the symbol error rates (SER) at operating SNR levels is around 10^{-3}. This test set will evaluate specially the synchronization algorithms near to the target $E_s/N_0 \approx 2$ dB, and also, the TC receiver sensitivity, i.e., the minimum operating SNR.
- *Channel decoding evaluation tests:* focused on evaluating and validating the channel decoding algorithms in the breadboard. The CER $\approx 10^{-5}$ is being evaluated; so, the number of codewords to test is huge in order to obtain accurate statistics.
- *End-to-end (E2E) performance evaluation tests*: where the test-bench is validated as a whole. The compliance of most of the system requirements will be assessed with these tests.

The different purposes of the tests impact on the test signal length. The symbol error statistics required for channel decoding evaluation implies a huge number of generated codewords. Hence, to reach CER $\approx 10^{-5}$ at the minimum symbol rate of 7.8125 sps in DS scenario with enough reliable statistics, the test would last 31 months. This is not feasible for a test campaign and these CER values cannot be evaluated with real time signals. The alternative is a recurrent approach consisting in the acceleration of the test signal injection in the breadboard under test. A desirable acceleration for DS would be a symbol rate of 2 ksps which is the maximum throughput achieved by MRB decoder algorithm according the detailed design. It implies an 256 times acceleration; so, the test duration is reduced down to 89 hours, which is still a very long test, but plausible for the final performance tests.

Nevertheless, this test acceleration is hard to achieve in the complete TC processing chain included in the breadboard, especially since there are critical SW processing elements in the synchronization schemes. Therefore, we decided to adopt a two test-bench set-ups approach with two different signal injections modes, illustrated in Figure 7 and described next:

1. *CLTU modulated waveforms*: The breadboard receives the signals behaving exactly as if the data stream were received from an analog-to-digital converter (ADC) in the TT&C transponder. The modulated waveform are represented in the equivalent complex baseband signal, in-phase (I) and quadrature (Q) components and the sampling rate must be greater than twice the signal bandwidth including dynamics. This signal injection is the most general case and it will be used for evaluation of carrier acquisition, synchronization algorithms and E2E performance.

2. *CLTU soft-symbols: The s*ource test signals are CLTU soft-symbols with the addition of Gaussian white noise by the SW channel emulator. This data stream is directly connected to the channel decoding algorithms in the breadboard, as if the channel symbols were received from the matched filter of the TT&C transponder. This is the best test-bench set-up for channel decoding algorithm evaluation, since it allows the acceleration of the symbol processing without impacting on the synchronization schemes. Furthermore, the soft-symbol representation is less demanding in terms of interface bandwidth and test signal size, since only one sample per symbol is required, i.e., sampling rate is just the symbol data rate.

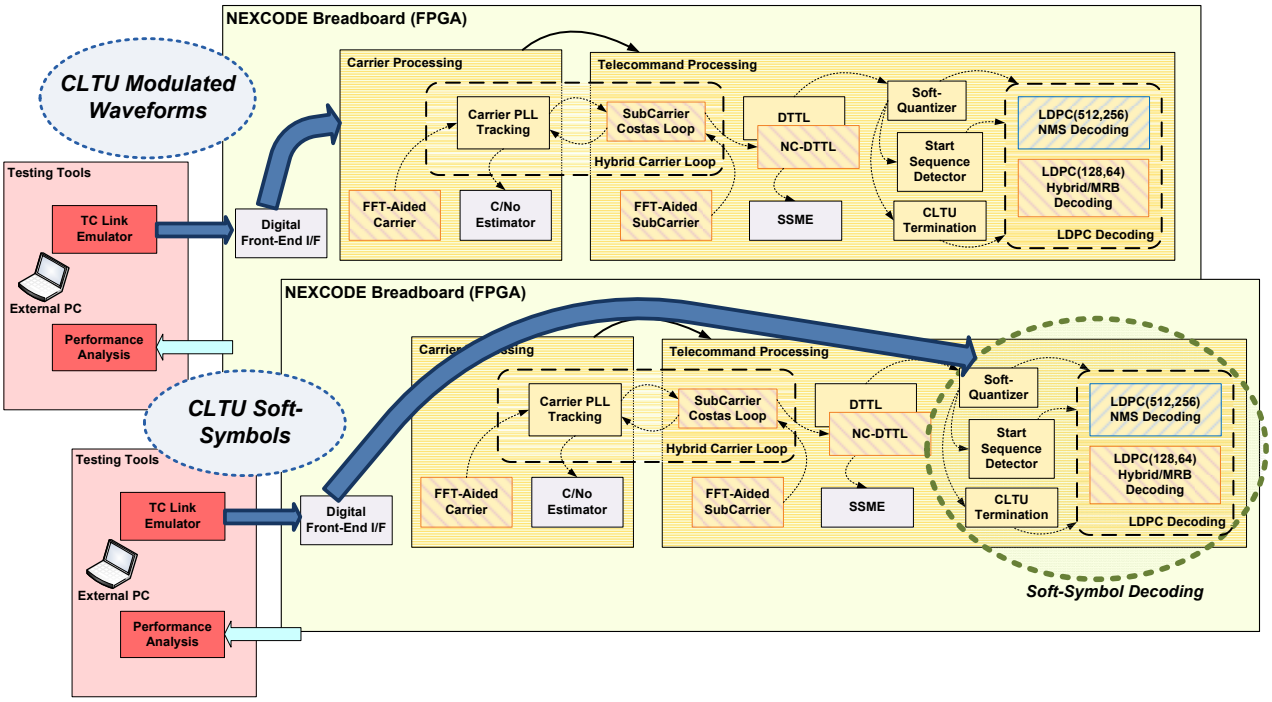

Fig. 7. Test-bench set-ups for system performance evaluation.

As state-of-the-art performance of the TT&C transponder, some previous test results demonstrate implementation losses around 2.5 dB at 7.8125 bps. This value includes the losses of the TC receiver chain (radio frequency (RF) section and digital part) up to the symbol timing synchronization stage, i.e., based on SER results. The SER figures obtained by SW simulation were less than 0.5 dB worse than the theoretical limit. Given that the test-bench is based on a fully digital domain implementation, basically, the quantization error is the additional contribution apart from the synchronization errors; hence, the overall losses should not be large and the target implementation losses are set around 1 dB for SER figures.

As regards the channel decoding evaluation, CER performance of the selected decoding algorithms has been obtained by simulation for the unquantized case and also for different channel symbols quantizations. When using 3 bits for the channel messages and 6 bits for the decoder messages (internal to the algorithm), the loss against the unquantized case is very limited, in the order of 0.15 dB for the short code and 0.2 dB for the long code. In the breadboard implementations very small additional losses are expected with respect to the SW simulator. These losses are produced by the limited accuracy of the fixed point operations in the FPGA, and then the target implementation losses are set around 0.5 dB for CER figures compared to the unquantized simulation case.

V. Conclusion

In this paper we have presented the NEXCODE project results, an ongoing activity for ESA to study and demonstrate new error correcting codes aiming at provision of better data rates and coverage in space missions. Theoretical performance results have been shown, demonstrating that the new coding techniques can operate at $E_s/N_0 \approx 0.5$ dB for the requirements of CER $\leq 10^{-5}$ and UCER $\leq 10^{-9}$. This low SNR operation is challenging for the overall receiver algorithms, including signal acquisition and tracking. Novel synchronization algorithms have been presented to overcome the standard TC processing bottlenecks at signal acquisition and tracking and at frame synchronization. A breadboard of the core elements, which is currently under development, will help to validate the potential changes to the O/B receiver architecture and to minimize the risk of adoption of these new techniques for future missions. The breadboard architecture presented provides a flexible platform supported by a SoC approach. The breadboard high-level design shows how the novel synchronization and decoding algorithms can be incorporated to the legacy TT&C platforms, by exploiting combined HW/SW processing and by attaching a dedicated FPGA for the algorithms with highest processing demands. Finally, the test-bench and the validation approach have been presented whose purpose is the effective performance and complexity evaluation of the novel algorithms as well as bringing the prototype TRL up to 3-4.

Acknowledgment

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