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GaN-based flip-chip LEDs with highly reflective ITO/DBR p-type and via hole-based n-type contacts for enhanced current spreading and light extraction

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ABSTRACT

We demonstrate GaN-based double-layer electrode flip-chip light-emitting diodes (DLE-FCLED) with highly reflective indium-tin oxide (ITO)/distributed bragg reflector (DBR) p-type contact and via hole-based n-type contacts. Transparent thin ITO in combination with TiO_2/SiO_2 DBR is used for reflective p-type ohmic contact, resulting in a significant reduction in absorption of light by opaque metal electrodes. The finely distributed via hole-based n-type contacts are formed on the n-GaN layer by etching via holes through p-GaN and multiple quantum well (MQW) active layer, leading to reduced lateral current spreading length, and hence alleviated current crowding effect. The forward voltage of the DLE-FCLED is 0.31 V lower than that of the top-emitting LED at 90 mA. The light output power of DLE-FCLED is 15.7% and 80.8% higher than that of top-emitting LED at 90 mA and 300 mA, respectively. Compared to top- emitting LED, the external quantum efficiency (EQE) of DLE-FCLED is enhanced by 15.4% and 132% at 90 mA and 300 mA, respectively. The maximum light output power of the DLE-FCLED obtained at 195.6 A/cm^2 is 1.33 times larger than that of the top-emitting LED obtained at 93 A/cm^2.

1. Introduction

GaN-based light-emitting diodes (LEDs) have received considerable attention for applications in full-color displays, visible light communication, automotive lighting, and solid-state lighting due to their advantages of high luminous efficiency, long operation lifetime, and low energy consumption [1–3]. GaN-based LEDs are typically grown on sapphire substrate that is electrically insulating so both p-type and n-type contacts are located on the same side of top-emitting LEDs, resulting in current crowding effect around electrode pads. Most scientific efforts have therefore focused on one approach to alleviate the current crowding effect: using insulating SiO_2 as current blocking layer [4,5]. In this scheme, an insulating SiO_2 layer inserted beneath the indium-tin oxide (ITO) was used to uniformly redirect the current path and thus improve current spreading. However, the reduced total area of the p-type contact between the ITO and the p-GaN due to the presence of the insulating SiO_2 layer will increase the forward voltage of top-emitting LEDs. Moreover, to make n-type contact on the n-GaN layer, a cutout area must be formed to expose n-GaN layer by etching a portion of p-GaN and active region, which decreases the active region area and consequently reduces the ability of LEDs to emit light [6]. Accordingly, optimized n-type contact pattern has been investigated to improve current spreading and to increase the utilization ratio of active region area [7–10].

In addition, there are severe heat conducting problem in laterally conducting top-emitting LEDs due to the poor thermal conductivity of sapphire substrate. Consequently, high junction temperature induced by heat accumulation decreases the external quantum efficiency (EQE) and light output power of LEDs. Furthermore, GaN-based LEDs exhibit a reduction in EQE at high current densities, which is in part attributed to non-uniform carrier distribution. These well-known current-induced and temperature-induced efficiency droop have hindered further enhancement in LEDs performance [11,12]. Flip-chip technology was brought up as practical approach to satisfy heat dissipating [13–15]. In the flip-chip approach, the top-emitting LED chip is physically flipped upside down and makes contact with the submount by arrays of solder bumps, thus providing a thermal path for the generated device heat to efficiently dissipate from contacting solders to the underlying heat sink [16,17]. The light extraction efficiency of flip-chip LEDs (FCLEDs) is limited due to the total internal reflection and absorption of light by

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opaque metal electrodes [18–21]. The p-type contact with high reflectance was required to minimize the absorption of light by opaque metal electrodes and thus improve light extraction efficiency of LEDs.

In this paper, we demonstrate a novel double-layer electrode flip-chip LED (DLE-FCLED) with ITO/DBR p-type contact and via hole-based n-type contacts, which simultaneously improves light extraction efficiency, current spreading and heat dissipating. In the DLE-FCLED structure, reflective ohmic contact to p-GaN was made by means of ITO/DBR, and contact to ITO was achieved by drilling holes through DBR which also acted as a dielectric mirror. Contact to n-GaN layer was made by etching via holes through p-GaN and InGaN/GaN multiple quantum well (MQW) active layer, resulting in a reduction in the loss of active region area. The utilization of double-layer electrode allows p-type contact hole to circle around the finely distributed via hole-based n-type contacts, which can reduce the lateral current spreading distance between p-type contact and n-type contact, and therefore improve uniformity of current spreading over the active region. In addition, the presence of the continuous metallic electrode layer in DLE-FCLED increases the contact area for flip-chip technology with Au-Sn eutectic bonding, thus providing superior heat dissipating.

2. Experiments

GaN-based LEDs were grown on the c-plane patterned sapphire substrate by using metal-organic chemical vapor deposition (MOCVD) technique. Trimethylgallium (TMGa), triethylgallium (TEGa), Trimethylaluminum (TMAl), and trimethylindium (TMIn) were used as Group III sources; TEGa was used to grow InGaN/GaN MQW, and TMGa was used to grow n-type and p-type GaN layers. Ammonia (NH_3), silane (SiH_4), and bis(cyclopentadienyl)magnesium (Cp_2Mg) were used as the Group V sources, n-type dopant and p-type dopant, respectively. The LEDs structure consists of a 20-nm-thick GaN nucleation layer, a 2.5-μm-thick undoped GaN buffer layer, a 2.0-μm-thick Si-doped n-GaN layer, a 180-nm-thick InGaN/GaN MQW, a 40-nm-thick Mg doped p-AlGaN electron blocking layer, a 27-nm-thick p-AlGaN/GaN superlattices, and a 110-nm-thick Mg-doped p-GaN layer. The InGaN/GaN MQW comprises twelve pairs of 3-nm-thick $In_{0.16}Ga_{0.84}N$ well and 12-nm-thick GaN barrier layers. The GaN quantum barrier was grown at 870 °C, and the reactor temperature was then decreased to 780 °C to grow the InGaN quantum well. After GaN epitaxial growth process was completed, the LED wafer was subsequently annealed at 750 °C at N_2 atmosphere to activate Mg in the p-GaN layer. The peak emission wavelength of LEDs is 456 nm.

Fig. 1 shows the fabrication process of the DLE-FCLED chip. The detailed processing steps are illustrated in the following: (a) inductively coupled plasma (ICP) etching based on BCl_3/Cl_2 mixture gas was employed to define via holes (40 μm) by etching through the p-GaN layer and MQW layer to expose the *n*-GaN layer; (b) an ITO layer with thickness of 60 nm was deposited on top of p-GaN layer followed by thermal annealing in N_2 ambient at 540 °C for 20 min to improve ohmic contact between ITO and p-GaN; (c) an insulating DBR comprising five pairs of alternating TiO_2/SiO_2 (45.8 nm/78.5 nm) dielectric layers was deposited on the top of ITO and filled the via holes. The TiO_2/SiO_2 DBR was then selectively etched to form n-contact hole (26 μm) and p-contact hole (13 μm) by combining photolithography and $CHF_3/Ar/O_2$ mixture gas; (d) Cr/Pt/Au (20 nm/50 nm/1.5 μm) metal was deposited on the top of TiO_2/SiO_2 DBR to form the first n-electrode and the first p-electrode. The first p-electrode was kept separate from the first n-electrode by an isolation trench. By filling the n-contact hole and p-contact hole with Cr/Pt/Au metal, current injection can be achieved; (e) a 500-nm-thick SiO_2 insulating layer was deposited on the top of first electrode layer. The SiO_2 insulating layer was then opened to form interconnect hole by buffer oxide etchant (BOE) wet etching; (f) Cr/Pt/Au (20 nm/50 nm/1.5 μm) was deposited on the top of SiO_2 insulating layer to form the second n-electrode and the second p-electrode. The first p-electrode and second p-electrode were connected through p-interconnect holes (40 μm). The first n-electrode and the second n-electrode were connected through n-interconnect holes (45 μm). Finally, LED wafer was thinned down to be about 158 μm and diced into chips with size of 381×762 μm^2. The epitaxial structures of top-emitting LED and DLE-FCLED are identical. For comparison, the same size of top-emitting LED chip was also fabricated through conventional procedures [22]. The design of top-emitting LED chip includes 190-nm-thick SiO_2 current blocking layer, 60-nm-thick ITO transparent conductive layer and Cr/Pt/Au (20 nm/50 nm/1.5 μm) n- and p-electrodes. The strip-

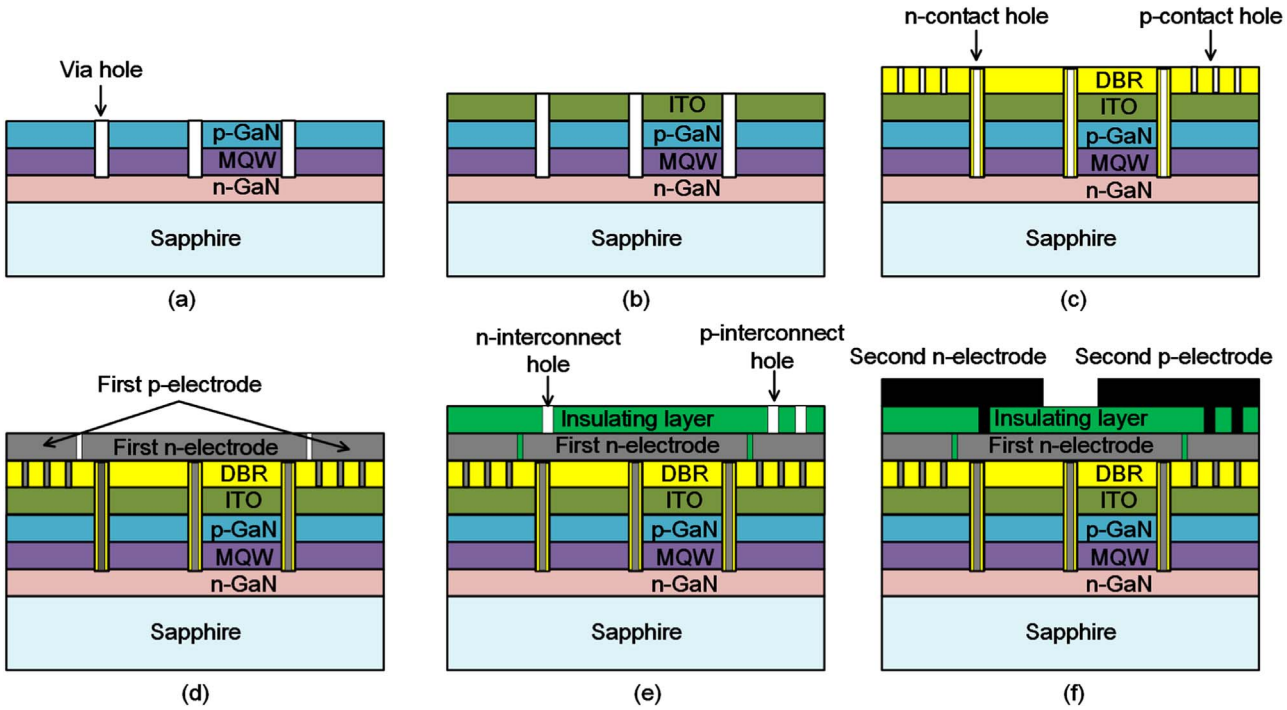

Fig. 1. Schematic illustration of DLE-FCLED fabrication process.

shaped SiO_2 current blocking layer and Cr/Pt/Au electrodes are employed in the top-emitting LED to obtain better current distribution property. The light output power–current–voltage (L-I–V) characteristics of LEDs were measured using a semiconductor parameter analyzer (Keysight B2901A) and an integrating sphere.

3. Results and discussion

Formation of reflective p-type ohmic contact electrode with low specific contact resistance and high reflectance is especially important for high performance FCLEDs. Metallic mirrors including aluminum (Al) and silver (Ag) can be used as highly reflective contact for FCLEDs owing to their high reflectance in the visible wavelength range. However, pure Al or Ag caused high specific contact resistance when it is directly deposited onto p-GaN layer due to their low work function. The combination of thin transparent p-type ohmic contact and reflective metallic mirror was therefore used as reflective p-type ohmic contact electrode in FCLEDs. In this scheme, an intermediate layer of thin nickel (Ni) or ITO was sandwiched between the metallic mirror and the p-GaN layer to decrease specific contact resistance, which in turn led to a reduction in reflectivity of the p-type contact [23,24]. In order to increase the reflectance of p-type contact, DBR having high reflectance can be employed as reflective layer instead of metallic mirrors [25,26]. For reflectance comparison, Ni (1.5 nm)/Ag (200 nm), ITO (60 nm)/Al (200 nm), and ITO (60 nm)/DBR (621 nm) films were deposited on the double side polished sapphire wafer, respectively. The measured reflectance of the deposited films as a function of light wavelength is shown in Fig. 2. At emission light wavelength of 456 nm, the measured reflectance of Ni/Ag, ITO/Al, and ITO/DBR is 76.1%, 62.4%, and 87%, respectively. It is indicated that there is a significant increase in the reflectance when metallic reflector such as Al and Ag is replaced by DBR. Accordingly, transparent thin ITO combined with five-pair TiO_2/SiO_2 DBR having high reflectance in the blue light wavelength range is used for reflective p-type ohmic contact in the DLE-FCLED chip, resulting in a reduction in absorption of light by opaque metal electrodes.

Fig. 3a shows the top-view scanning electron microscopy (SEM) image of the fabricated DLE-FCLED chip. In Fig. 3a, the p-contact holes are circled around n-contact holes to enhance current spreading, and the interconnect holes are used to connect the first electrode layer and the second electrode layer. In order to increase bonding area for flip-chip configuration, the second n-electrode pad and the second p-electrode pad are respectively located on the left and right of the DLE-FCLED chip as shown in Fig. 3a, thereby maximizing heat conduction from chip to submount. Fig. 3b and c illustrates the cross-sectional SEM images obtained by using focused ion beam (FIB) along A–A and

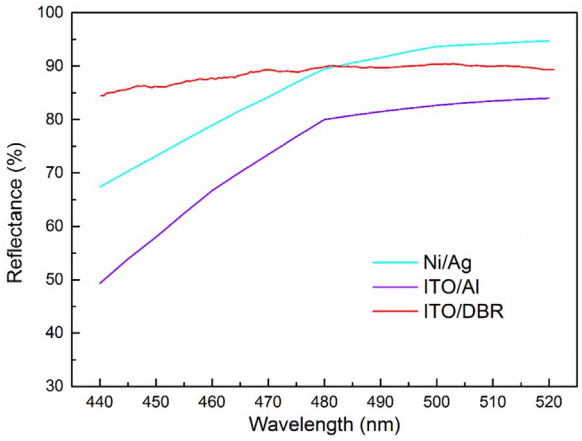

Fig. 2. Measured reflectance of Ni/Ag, ITO/Al, and ITO/DBR films at normal incidence. (For interpretation of the references to color in this figure, the reader is referred to the web version of this article.)

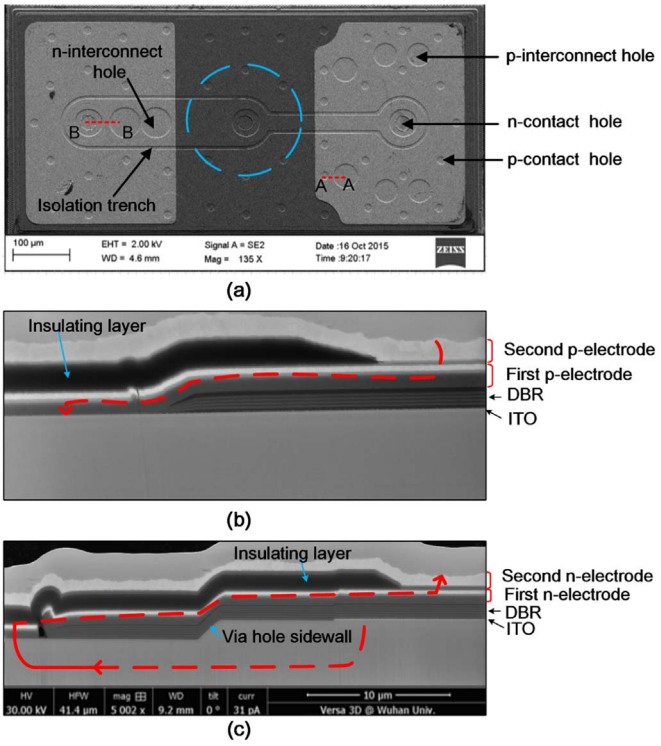

Fig. 3. (a) Top-view SEM image of the fabricated DLE-FCLED chip. (b) Cross-sectional SEM image of the DLE-FCLED chip along A-A direction milled by FIB. The current path from second p-electrode to ITO is marked by red dash line. (c) Cross-sectional SEM image of the DLE-FCLED chip along B-B direction milled by FIB. The current path from ITO to second n-electrode is marked by red dash line.

B–B directions as marked in Fig. 3a. In Fig. 3b, the first p-electrode and the second p-electrode is connected by p-interconnect hole with filled Cr/Pt/Au metallic column. Outside the p-interconnect hole, a SiO_2 insulating layer was inserted between the first p-electrode and the second p-electrode. In Fig. 3c, the sidewall of via holes is covered by insulating TiO_2/SiO_2 DBR to prevent short-circuiting in the p-n junction. Similar to Fig. 3b, the first n-electrode and the second n-electrode is connected by n-interconnect hole with filled Cr/Pt/Au metallic column as shown in Fig. 3c. Outside the n-interconnect hole, a SiO_2 insulating layer is inserted between the first n-electrode and the second n-electrode. Furthermore, current paths from second p-electrode to ITO and from ITO to the second n-electrode are marked by red dash line in Fig. 3b and Fig. 3c, respectively.

One of the primary advantages of via hole-based double-layer electrode is the improved current spreading performance. An efficient current spreading can lead to uniform light emission intensity. Simulations performed with commercial SimuLED package further demonstrated the performance on current spreading for DLE-FCLED and Top-emitting LED, as shown in Fig. 4. It was found that a smaller root-mean-square value of current density is achieved for DLE-FCLED, indicating a more favorable uniformity of current spreading. Effective light-emitting area and current density distribution of DLE-FCLED and top-emitting LED at 10, 90 and 200 mA were given in Table 1.

Due to an improved p-contact resistance and p-type doping, DLE-FCLED and top-emitting LED had a negligible vertical series resistance (Rv), the voltage drop across the Rv is smaller than kT/e (26 mV, when T=300 K). The current distribution of DLE-FCLED and top-emitting LED can be expressed as [27,28]:

$$J(x) = J_0 \exp(-x/L_s) \tag{1}$$

$$L_s = \sqrt{\frac{2n_{ideal}KT/q}{J_0\left(\frac{\rho_{ITO}}{t_{ITO}} + \frac{\rho_{n-GaN}}{t_{n-GaN}}\right)}} \tag{2}$$

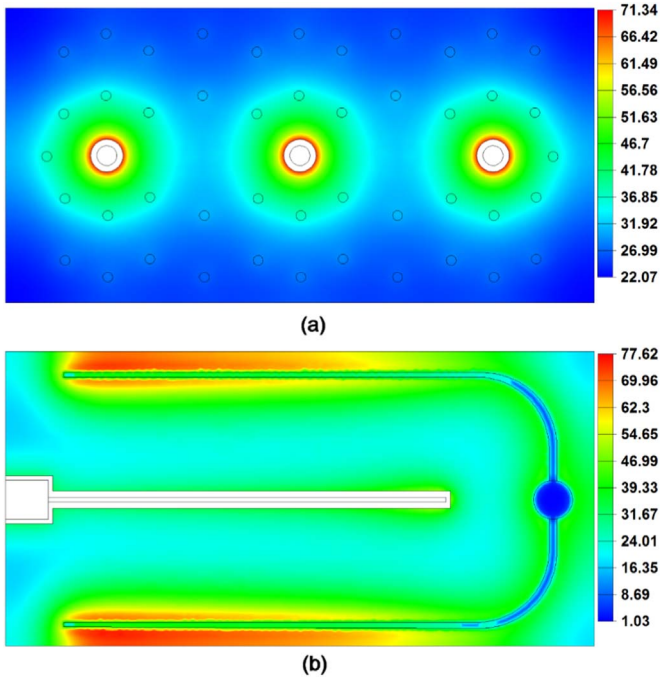

Fig. 4. SpeCLED simulation of the current density distribution at 90 mA in the active region of (a) DLE-FCLED (b) top-emitting LED.

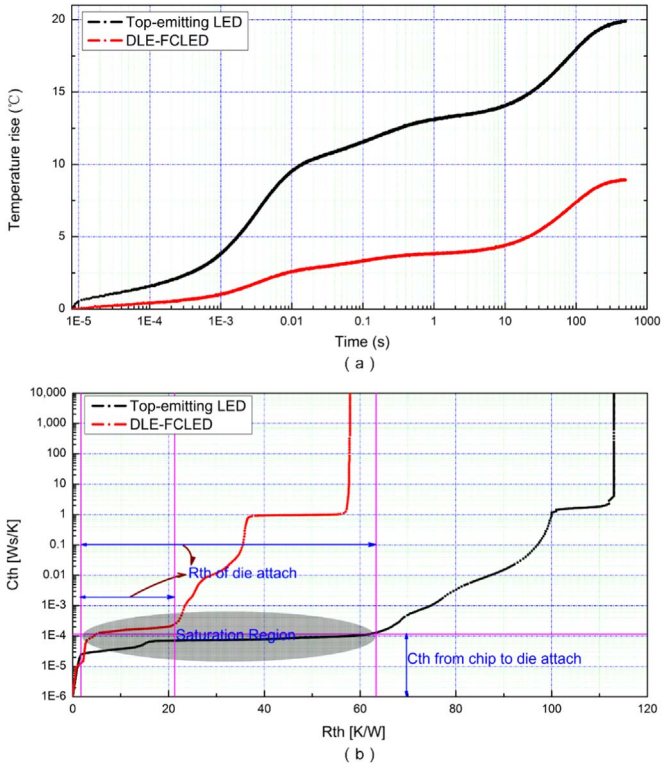

Fig. 5. Transient thermal characteristics of top-emitting LED and DLE-FCLED. (a) Transient junction temperature rise of the LED packages at an injection current of 90 mA. (b) Integral structure functions of top-emitting LED and DLE-FCLED packages under 90 mA current injections.

where J_0 is the current density at the edge of electrode with current crowding, x is distance from electrode with current crowding, L_s is current spreading length, ρ_{ITO}, t_{ITO}, ρ_{n-GaN}, t_{n-GaN} are the resistivity and thickness of ITO layer and n-GaN layer, respectively. K, q, T are the Boltzmann constant, element charge, and temperature, respectively. n_{ideal} is the ideality factor. The utilization of double-layer electrode allowed finely distributed p-type contact hole to circle around the via hole-based n-type contacts while keeping the active region area as large as possible, leading to reduced distance between p-electrode and n-electrode and thus improved uniformity of current spreading over the active region according to Eq. (1).

The junction temperature (Tj) and thermal resistance are two critical parameters that are related to the EQE, reliability, and lifetime of LEDs [29]. Therefore, we measured the above two parameters by transient thermal analysis in order to explore the extent of heat dissipation that the DLE-FCLED can provide. The thermal transient measurements were carried out in a thermal transient tester (T3ster, MicRed). For this measurement, LED packages (SMD type) consisting of chips of dimension 381×762 μm^2 were used. Silver paste was used for mounting the top-emitting LED chip onto Ag-coated aluminum submount. The DLE-FCLED chip was bonded onto Ag-coated aluminum submount with pre-deposited Au/Sn layer via flip-chip technology with Au-Sn eutectic bonding. Fig. 5a shows the transient junction temperature rise of LED packages obtained at 90 mA under the continuous-wave (CW) current operation mode. Here each curve represents time dependence of Tj rise of a chip with the constant injection current of 90 mA under ambient temperature of 25 °C. The measured Tj of the DLE-FCLED is up to 34.4 °C, whereas the measured Tj of the top-emitting LED is up to 45.1 °C. It is indicated that the junction temperature of DLE-FCLED is lower by 23.7% than that of top-emitting LED. The integral structure functions derived by direct mathematical transformations from the experimental cooling curves are demonstrated in Fig. 5b. The first curve inflection denotes chip thermal resistance, and both of value are roughly same, which is about 2.6 K/W. The following saturation region means heat flow from chip to die-attach which is correlated with heat-spreading performance of LEDs. Under an injection current of 90 mA, the value of the Cth from chip to die attach is calculated according to material attributes, and it is used to discriminate Rth of chip and die attach. As shown in Fig. 5b, the values of Rth for the FCLED and top-emitting LED are measured to be 22.6 K/W and 63.5 K/W, respectively. It is revealed that the Rth of the FCLED chip is lower by about 40.9 K/W than that of top-emitting LED. A reduction in thermal resistance between the chip and the submount is expected to extend the CW operation range to higher power levels.

The dependence of forward voltage and dynamic resistance on injection current for top-emitting LED and DLE-FCLED is shown in Fig. 6a. The forward voltages measured for DLE-FCLED and top-

Table 1
Current density distribution of DLE-FCLED and top-emitting LED at 10, 90 and 200 mA.

Driving current	10 mA		90 mA		200 mA	
LED type	DLE-FCLED	Top-emittingLED	DLE-FCLED	Top-emitting LED	DLE-FCLED	Top-emitting LED
Effective light-emitting area (mm^2)	0.97	0.95	0.97	0.95	0.97	0.95
Maximum current density (A/cm^2)	5.84	6.85	71.34	77.62	164.75	177.88
Minimum current density (A/cm^2)	2.84	0.65	22.07	1.03	47.88	1.12
Root-mean-square value (A/cm^2)	3.52	3.78	32.29	35.94	71.98	80.72

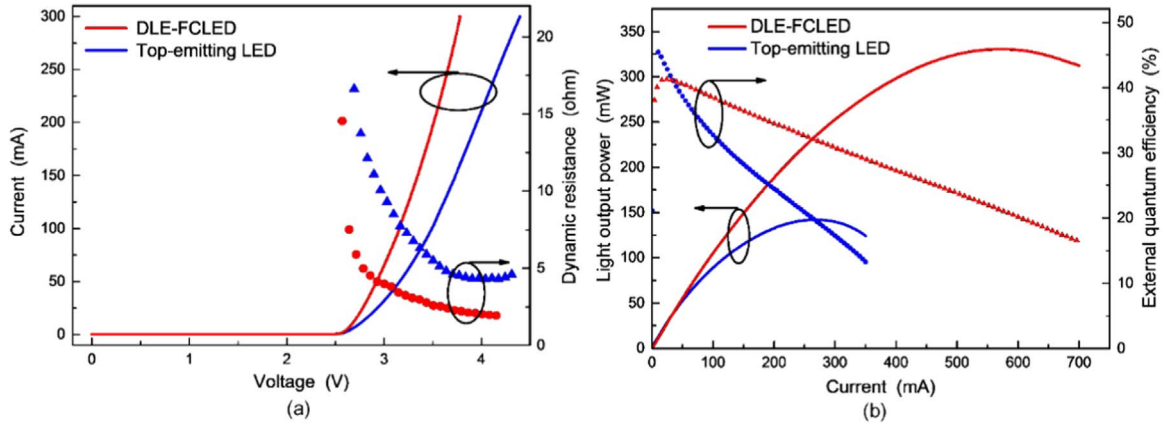

Fig. 6. (a) Forward voltage and dynamic resistance versus injection current for top-emitting LED and DLE-FCLED. (b) Light output power and EQE versus injection current for top-emitting LED and DLE-FCLED. The chip dimension is 381×762 μm^2.

emitting LED are respectively 3.12 V and 3.43 V at 90 mA. The DLE-FCLED with series resistance of 1.94 Ω, 57.7% lower than the case of top-emitting LED with series resistance of 4.59 Ω that is deduced from dynamic resistance. The dynamic resistance of LEDs is expressed as [30]

$$r = \frac{dV}{dI} = \frac{1}{Iq/nkT + 1/R_{sh}} + R_s \tag{3}$$

where R_s is the series resistance, and R_{sh} is a shunt resistance parallel to the p-n junction. Clearly, the first item in Eq. (3) is negligible when current I becomes large, and the dynamic resistance remains constant, equal to the series resistance of LED, which is well consistent with the calculated dynamic resistance curve as shown in Fig. 6a.

Fig. 6b shows the light output power and EQE as a function of injection current for encapsulated top-emitting LED and DLE-FCLED under the CW current operation mode. Although the DLE-FCLED suffers relatively lower EQE under low forward biases, the peak efficiency current shifts from 1.45 A/cm^2 for the top-emitting LED to 8.19 A/cm^2 for the DLE-FCLED. It is worth noting that the light output saturation current density increases from 93 A/cm^2 for the top-emitting LED to 195.6 A/cm^2 for the DLE-FCLED. The light output power of DLE-FCLED is 15.7% and 80.8% higher than that of top-emitting LED at 90 mA and 300 mA, respectively. The EQE of the top-emitting LED and DLE-FCLED at 90 mA and 300 mA are 33.8% and 39.0%, and 13.3% and 30.8%, respectively. Direct comparison is performed at the same injection current, and the results indicates that the EQE of DLE-FCLED improves by 15.4% and 132% at 90 mA and 300 mA, respectively. The efficiency droop is reduced from 38.2% for the top-emitting LED to 5.6% for DLE-FCLED at 90 mA. These improvements are attributed to the introduction of highly reflective ITO/DBR p-type contact and via hole-based n-type contacts, leading to higher light extraction efficiency, better current spreading and reduced loss of active region area, and also to the flip-chip configuration with Au-Sn eutectic bonding that provides superior heat dissipating.

Fig. 7 shows far-field angular light emission pattern of top-emitting LED chip the DLE-FCLED chip, respectively. During these measurements, we injected a current of 90 mA into these two different kinds of LEDs. It can be seen clearly that the light emission intensity of DLE-FCLED with a thick sapphire substrate of 150 μm in the near vertical directions is the same as that in the near horizontal directions due to contribution of sidewall light emission from the chip edge along the 150-μm-thick sapphire substrate. However, the light emission intensity of top-emitting LED in the near vertical directions is markedly higher than that of top-emitting LED in the near horizontal directions because the grown GaN epitaxial layer is very thin (about 7 μm), thereby resulting in weak sidewall light emission along the thin GaN epitaxial layer. As shown in Fig. 8, the angular variation of the emission pattern

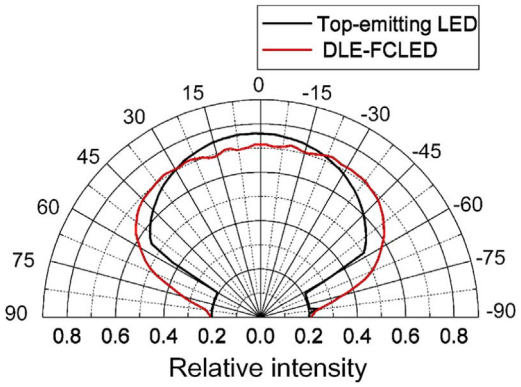

Fig. 7. Far-field angular light emission pattern of top-emitting LED chip and DLE-FCLED chip.

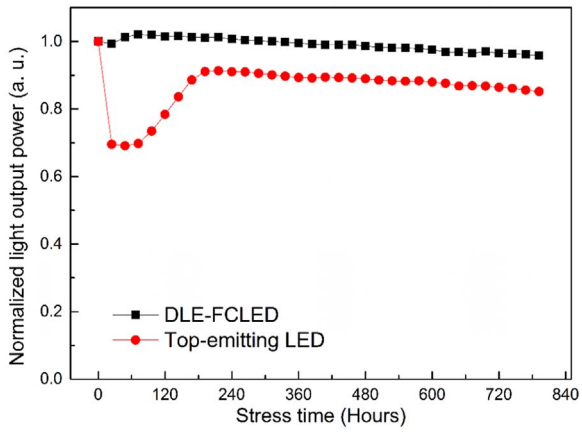

Fig. 8. Optical degradation of the top-emitting LED chip and DLE-FCLED chip during high temperature operation life test.

for the DLE-FCLED is nearly negligible between −45° and 45°, and the angular variation of the emission pattern for the top-emitting LED is significant between −45° and 45°. Accordingly, we can obtain brighter light emission at the in-plane directions with DLE-FCLED.

Moreover, the optical degradation of top-emitting LED chip and DLE-FCLED chip, as shown in Fig. 8, is also investigated at the condition of 85 °C using an injection current of 90 mA. After high temperature operation life test (792 h), the light output power of DLE-FCLED decreases by 4.21%, while the light output power of top-emitting LED decreases by 14.83%. Clearly, the DLE-FCLED exhibits markedly smaller optical degradation and thus higher device reliability as compared to the top-emitting LED. The optical degradation of LEDs

during the high temperature operation life test is generally believed to be the result of generation/propagation of extended defects which increases non-radiative recombination paths [31,32]. It was previously reported that the efficiency droop can be categorized into two classifications: current-density droop and temperature droop [33]. The GaN-based LEDs suffer from a strong decrease in light output power with increasing temperature, which is well known as temperature droop. The top-emitting LEDs are much inferior to DLE-FCLEDs in terms of heat dissipating performance, thus top-emitting LEDs are more easily to yield to high temperature operation life test and generate defects. It is this inferiority in heat dissipating that causes the large initial drop in the normalized light output power of top-emitting LEDs.

4. Conclusions

In summary, we demonstrate a highly reflective ITO/DBR p-type contact and via hole-based n-type contacts for FCLEDs. The ITO/DBR p-type contact has high reflectance in the blue light wavelength region, thereby leading to a reduction in absorption of light by metal electrodes and thus an increase in light extraction efficiency. The finely distributed via hole-based n-type contacts reduce lateral current spreading length, and hence improves uniformity of current spreading over the active region. The forward voltage of DLE-FCLED is 3.12 V at 90 mA compared to 3.43 V for top-emitting LED. The light output power of DLE-FCLED is 15.7% and 80.8% higher than that of top-emitting LED at 90 mA and 300 mA, respectively. The light output saturation current density increases from 93 A/cm^2 for top-emitting LED to 195.6 A/cm^2 for DLE-FCLED. The DLE-FCLED outperforms conventional top-emitting LEDs by generating bright-light emission with relatively lower junction temperature and thermal resistance, owing to its high light extraction efficiency, superior current spreading and heat dissipation.

Acknowledgements

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