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Implementation of a modified carrier-based PWM technique for a cascaded MLI using DSP microcontroller

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ABSTRACT

A multi-level converter is a power electronic device desired to generate a desired AC voltage level using several introduced DC voltages, the output voltage of the converter is characterized by a low harmonic content (THD) compared to conventional inverters. The adopted innovative design permits the independent control of PV modules, enabling, in this way, to operate independently and won't be very affected by intermittence. Additionally in this paper, a new control strategy based on sinusoidal pulse width modulation (SPWM) technique is analyzed for cascaded H-Bridge inverter. In this new technique, separate modified carriers are used for each H-Bridge (HB). Multiple-carrier SPWM is used with the new control SPWM technique. Those carriers are being implemented with diverse sinusoidal dispositions phase disposition (PD), phase opposition and disposition (POD), alternative opposition and disposition (APOD), and with altered frequencies. Experimental results are obtained while using different operating conditions.

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1. INTRODUCTION

Inverters are used in all areas of power electronics [1]. Due to the rapid evolution of semiconductor components made in terms of power, robustness, and speed. Although their many advantages, conventional inverters exhibit certain inconveniences such as limitation of its application to low and medium power voltages and the rapid deterioration of its components due to the voltage constraints on the power switches [2]. To overcome these problems, a new type of inverter has been introduced: the multi-level inverter. A converter is said to be multi-level when it generates an output voltage composed of at least three levels. This type of converter has two particular advantages. On the one hand, the structure of the multi-level inverter that makes it possible to reduce the voltage restrictions on the power switches. On the other hand, the output voltage delivered by multi-level converters has interesting spectral qualities. It can generate voltages close to the sinusoidal, with spectral performance superior to that of two-level inverters [3].

Numerous multi-level inverter topologies are stated in the literature. The most known ones are diode clamped inverters (NPC), cascaded h-bridge inverters (CHB) and flying capacitor inverters (FC) [4]. Among the diverse multilevel inverter topologies, the cascaded h-bridge multilevel inverter's topology is an advantaged choice to the new built design for its modularity and the robust degrees that make it possible to operate even

under defective conditions, increasing the reliability of the system [5]. In spite of all these features, the cascaded multilevel topology has also some weaknesses; for instance, the strings of photo-voltaic (PV) panels are not grounded; so additional procedures have to be engaged in order to remove the returning currents.

The production of the modulation control signals for Cascaded H Bridge multi–level inverters is generally done in real time. To determine the closing and opening moments of the switches, analog control, digital or both simultaneously, there are several pulse width (PWM)modulation techniques, mainly sinusoidal modulation and vector modulation space vector modulation [6]. The space vector pulse width modulation (SV-PWM) space vector modulation has been widely applied because of its simple structures. However, despite the easy implementation for converters with low levels "below 5", the implementation can become complex for those above 5 levels with an excessive computing time [7].

Sinusoidal PWM (S-PWM) also recognized as multi-carrier PWM is widespread because of its simplicity, and its ability to produce good quality in the output [8]. This technique is classified into phase disposition (PD-PWM), phase opposite disposition (POD) and alternative phase opposite disposition (APOD-PWM) [9]. SPWM technique is generally used in Cascaded H Bridge multilevel inverters, as it offers many advantages. In this paper an S-PWM with modified carriers' techniques, on CHB multilevel inverter is analyzed. It is found that for similar device and switching frequency, the overall performance of the modified carriers SPWM technique in terms of line voltage THDs is superior compared to those with conventional techniques. In addition, the switch utilization is uniform among the PV modules.

2. NUMBER OF NECESSARY COMPONENTS

With the help of the following Table 1, indicate the number of indispensable components "main switches, capacitors and clamped diodes" to build the different types of multilevel inverters. Implicitly from the Table 1, the cascaded inverter requires a minimum number of components. So those types of inverters offer the most profitable multi-level solution, especially when the number of levels becomes important. Cascaded inverters have the flexibility of their circuit design because each level has the same structure, and there are no additional diodes or balancing capacitors. The number of output voltage levels can be easily adjusted by adding or removing a full bridge, when the inverter does not need to produce the power to the system [10].

Table 1. Number of components required for the three-level multi-levels inverters topologies

Topology	N	E	K	Dp	Dc	C
Diode clamped (NPC)	3	2	4	4	2	0
Flying capacitor (FC)	3	2	4	4	0	1
Cascaded h-bridge	3	1	4	4	0	0

With, N: number of voltage levels, Dp: number of the main diodes, E: number of DC sources, Dc: number of clamped diodes, K: number of necessary switches, and C: number of balancing capacitors

3. CASCADED H-BRIDGE TOPOLOGY

The N-level Cascaded H-Bridge, multilevel inverter contains (N-1)/2 single phase H-bridges [11], this type of converter with a "modular" structure is based on the placement in series of H-bridge converters of Figure 1. Each module has its own voltage source and power components. The H-bridge alone makes it possible to obtain 3 voltage levels (Vdc, -Vdc, 0).

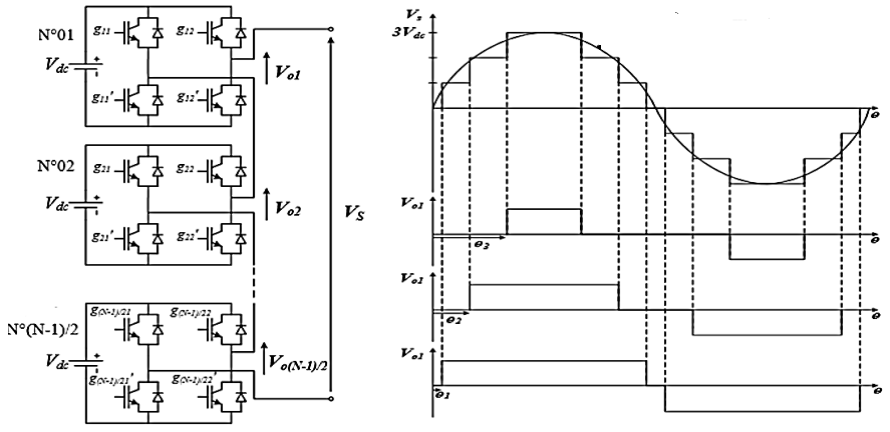


Figure 1. Waveforms for an N-level cascaded inverter

The use of this serial conversion structure allows increasing the number of voltage and power level. But the major restriction of this topology is the large number of isolated DC voltages required for each H-bridge. Its modular assembly of identical H-bridges is a positive feature due to possibility to adjusting levels by adding or removing H-bridges [12].

Thanks to its benefits, the cascaded inverter bridge has been widely used to applications with high power production due to its aptitude to produce waveforms with better harmonic spectrum and low switching frequency. Many benefits can be count for using cascaded multi-levels inverter: i) The number of possible output voltage levels is higher than the number of dc sources introduced to the inverter; and ii) The series of H-bridges will allow the built-up process to be done fast and cheaply

4. CARRIER-BASED PWM PULSE WIDTH MODULATION

Carrier-based pulse width modulation (PWM) is a popular technique used for power electronic applications, especially for voltage source inverters [13]. This technique is used to control the power delivered to an electronic load by adjusting the width of pulses in a high-frequency carrier signal. In carrier-based PWM, the amplitude of the carrier signal is kept constant while the width of the pulses is varied in proportion to the desired power level. The modulation index is the ratio of the pulse width to the period of the carrier signal, and it determines the amount of power delivered to the load [14].

One of the main advantages of carrier-based PWM is its ability to produce a smooth output voltage with low distortion. It is also an efficient technique, as it minimizes the power dissipation in switching devices such as transistors or metal oxide semiconductor field effect transistor (MOSFETs). However, it can be more complex to implement than other PWM techniques, as it requires a high-frequency carrier signal and precise timing control. There are several different carrier-based PWM techniques, each with its own advantages and disadvantages. Here are some of the key differences between some of the most common carrier-based PWM techniques:

Sinusoidal PWM (SPWM), SPWM is a widely used PWM technique for generating a sinusoidal output waveform. The technique involves comparing a sinusoidal reference signal with a triangular carrier wave to generate a pulse width modulated signal. SPWM produces low harmonic distortion, but the control circuit is complex and can be sensitive to changes in the load [15].

Dual reference phase shifted PWM technique: This technique is used to produce a higher number of output voltage levels. The technique involves two reference signals and two carrier signals that are phase shifted from each other. This technique produces a better output waveform than standard carrier-based PWMs, but it is more complex to implement [16]. Triple reference this technique involves three reference signals and three carrier signals, which are phase shifted from each other. This technique produces a higher number of output voltage levels than standard carrier-based PWMs [17]. Compared to the other techniques the S-PWM present many positive aspects: Carrier-based SPWMs are effective in reducing harmonic distortion in voltage source inverters. This is because the PWM technique produces a sinusoidal output waveform that closely matches the input waveform, resulting in low harmonic distortion [18].

Simplified control, SPWMs have a simple control scheme, which makes them easy to implement and maintain. The control strategy is based on the comparison of a reference signal and a carrier signal, which generates the PWM signals [19]. It can operate at high switching frequencies, which leads to improved system efficiency and reduced filter size. This is because the high-frequency switching reduces the size of the output filter needed to remove unwanted harmonics [20]. Overall, the choice of PWM technique depends on the specific requirements of the application, including the desired output waveform, the number of switching operations, and the complexity of the control circuit [21]. Each technique has its own advantages and disadvantages, and the optimal technique may vary depending on the specific application.

5. DESIGN METHODOLOGY

This project consists in realizing a multi-level inverter with the possibility of adjusting the levels by adding or removing an H-bridge card. This realization will have H-bridge boards adapted to be inserted on another main board with peripheral component interconnect (PCI) connectors" to increase the number of levels. In this way, it will allow to control each solar panel of the system and make it independent, if the system meets a problem the defaulted panels will be replaced by batteries when needed. As a result, the system will not be mainly affected by any kind of defaulted elements or intermittence. The experimental tests were performed in three stages. The first were performed on the testing setup to ensure the proper operation of the different H-bridges.

Then, the inverter is tested with the triangular carrier-based control technique. After that, comes the modification of the carrier to improve the control technique for this type of inverters. Thus, the realization of the prototype will pass mainly by two phases: first a realization of the H bridges in the form of mini-bars

Figure 2. Secondly, these bars can be inserted in another card that can detect the emplacement and then set the control scheme according to their location.

5.1. H-bridge cards

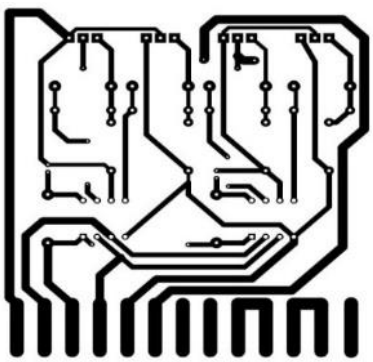
A pulse voltage from a digital signal processor (DSP) is regularly sufficient to switch a metal oxide semiconductor field effect transistor "MOSFET" working in small signals applications. However, 5 V drive signal is not appropriate when working in high voltages. It is required to apply 12 V to switch completely the components of the H Bridge [22]. A MOSFET driver translates the logical signals generated by those DSP in order to switch completely and quickly the gate of the MOSFET even in high voltages. In addition, the driver MOSFETS, generates from a single input signal, two signals with a dead time which minimizes the number of output pins used by the controllers.

Since the converted voltages are high the drivers MOSFETS are needed their task is injecting currents so the MOSFET spend the minimal time on the transition state. The design of the H-card for each H-bridge will require the following equipment's as shown in Table 2.

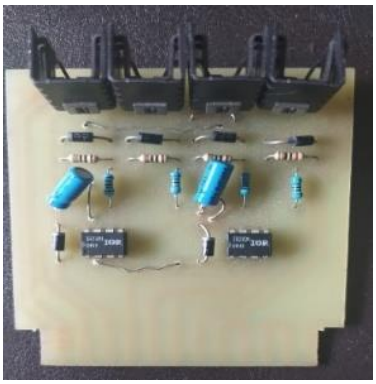
Table 2. Components required for the H-bridge card

Quantities	Equipment	Purpose
4	Resistances 10R	Protective resistance
4	Resistances 1k	MOSFET protection resistor
2	Capacity 33 uF/16 V	Maintains the stability of the driver's power supply
2	Drivers IR2304	Driver de grille à transistor
4	MOSFET IRF Z44N	Bridge switches h
6	Diodes 1N4007	Freewheeling diodes/reverse current protection

MOSFET IRF Z44N offers great features that are essential for this application with high current handling capability, fast switching speed and high efficiency for a wide variety of applications [23]. Resistances and Diodes are used to remove currents that might be introduced by the on/off times of the MOSFETs. Based on the H-bridge components discussed in the previous Table 2, a design of the mini card Figure 2 can be as shown Figure 2(a) shows the PCB design of the H-bridge cards and Figure 2(b) shows the card after the realization.



(a)



(b)

Figure 2. Mini-card design (a) PCB design and (b) H-bridge mini-card

6. SERIAL CONNECTION OF THE H-BRIDGES

6.1. Dimensions and forms

To ensure a seamless integration between the H-bridge and the PCI connectors, it is important to accurately measure and match the dimensions of the connectors before making the necessary adaptations to the schematics. In this part, the necessary adaptation for the functioning H-bridge is created with the PCI connectors. PCI connectors Figure 3, is adapted to the schematics in a suitable way that the connection between the H bars with the PCI are made without errors, so first thing is determinate the different dimensions of the PCI connectors.

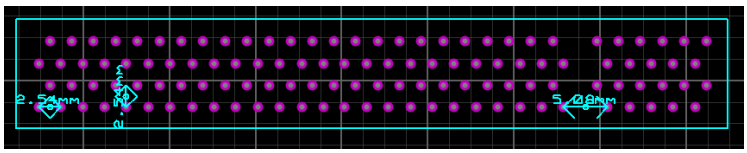


Figure 3. PCI connector diagram on areas

6.2. PCI connector features

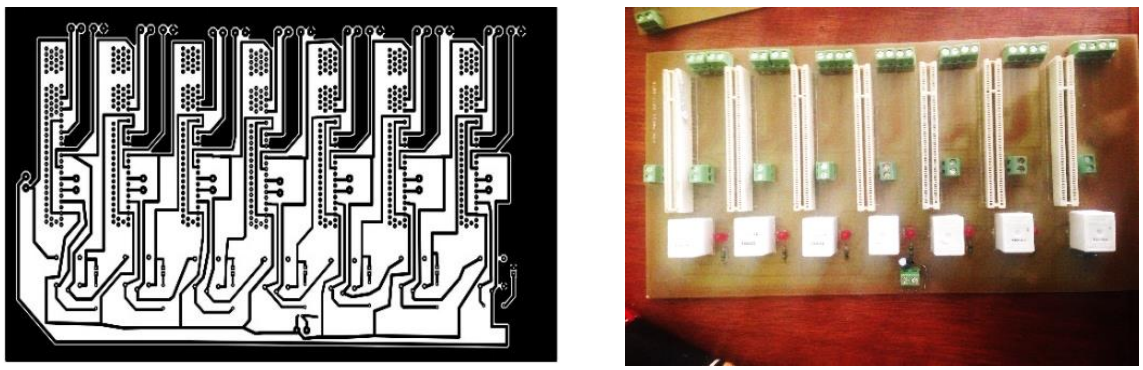
By incorporating the printed PCI connectors, the H-bridge mini cards can be easily connected to the control card through a serial connection, thereby enabling the efficient functioning of the system. The design of the printed PCI connectors as shown in Figure 3 will allow the connection between the H-bridges mini cards inserted and the card designed to control of the serial connection of those cards Figure 4 represent the PCI connector with the top view Figure 4(a) and the bottom view Figure 4(b):

- Total length: 84.84 mm
- Length used: 63 mm
- Spacing between two pins: input: 1.27 mm
- Number of pins per line: 49
- Pin spacing: output: 2.5 mm
- Number of pins used: 25

(a) (b)

Figure 4. PCI Connector for cards connection (a) top view and (b) bottom view

The H-bridge mini cards will be inserted in the card shown in Figure 5(a) and Figure 5(b) designed so it detects the emplacement and then set the control scheme according to their location. The use of a normally closed relay, will allow the H-bridge stage to be cancelled if the mini card is not present, the DSP generates a signal to detect the placement of the H-Bridge cards inserted. A code of 7-digit will indicate those cards emplacements. For example, the code 0010010 means that two cards are inserted, and their location are in the second and fifth slot. After the test, the SPWM sub program will generate the switching pulses according to the code "from 3 to 15 level" and will run until the inverter stop Figure 6 shows the diagram to generate the switching scheme [24]. Several ways have been developed with the objective of generating a sinusoidal voltage with as little harmonics as possible at the output of the inverter [25]. A comparative study between the 7 and 15 level inverters with different controls was done in the following analysis.



(a) (b)

Figure 5. Circuit design printed on are (a) PCB design and (b) H-bridge main card

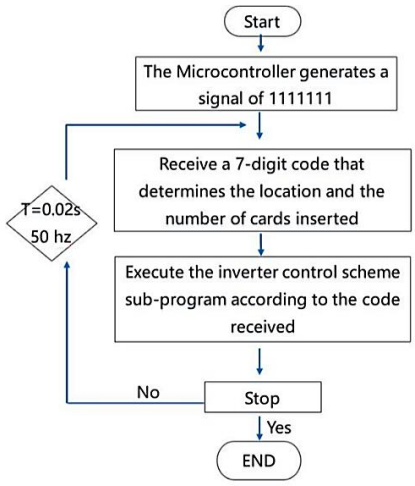


Figure 6. Diagram to generate the switching scheme

7. SWITCHING PROGRAM

To generate the control pulses based on sine modulation of an N level Inverter, N-1 triangular carriers are required. This sinusoidal pulse width modulation technique is the most widely used for controlling two-level or multi-level inverters [26]. It consists in comparing a reference signal, generally sinusoidal (the signal to be synthesized) with a generally triangular carrier signal, the output signal changes state at each cross between the modulated signal and the carrier. Those carriers are continuously compared to the same reference voltage, focusing each carrier to a voltage level [27]. If the reference is superior to a carrier signal, then the corresponding devices to that carrier is switched on and if the reference lesser than a carrier signal, then the devices corresponding to that carrier is switched off this method is known as level-shifted pulse width modulation (LS-PWM). Carriers further classified as multilevel PD-MLI phase, APOD or POD-MLI phase opposition [28]. Depending on the arrangements of the carriers, these possibilities are illustrated by the following Figures 7 to 9.

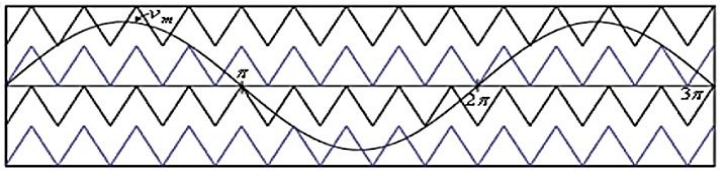


Figure 7. Phase disposition

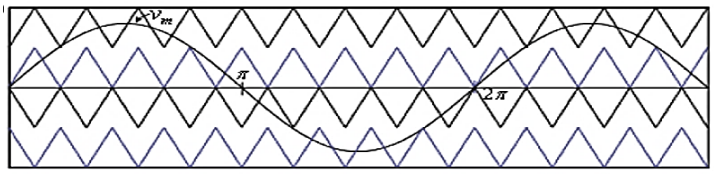


Figure 8. Phase opposition disposition

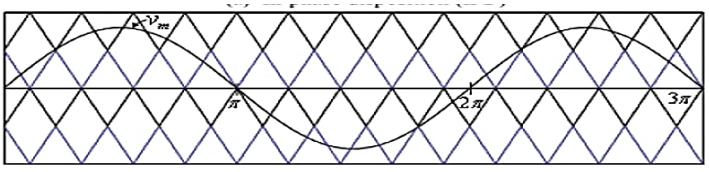


Figure 9. Alternate phase opposition disposition

7.1. Phase disposition

In phase disposition technique (PD) all the carriers have the same amplitude and frequency. Furthermore, all the N-1 carriers are in phase. This technique is based on a comparison of a sinusoidal reference signal with vertically shifted carrier signals, as shown in Figure 7, This method uses N – 1 carrier signals to generate the N level output voltage. All the carrier signals require the same amplitude and frequency [29].

7.2. Phase opposition disposition

The phase opposition disposition of the carrier signal is a common modulation technique used in power electronics to reduce the harmonic distortion in the output waveform and improve the overall efficiency of the system. In phase opposition disposition (POD) Figure 8, the carrier signal above the zero have same frequency, same amplitude and in phase of each other's. But the below the zero are phase shifted 180 degree compares to the above zero [30].

7.3. Alternate phase opposition disposition

Alternate phase opposition disposition PWM (APOD), all carriers are changing phase 180 degree with its adjacent as shown in Figure 9, Odd carriers are in phase going from 0 to 1, but even carrier waveforms are phase shifted from 0 to -1 with 180 degree [31]. This technique is particularly useful in applications where high switching frequencies are required, such as in motor control and power supplies, as it helps to minimize the switching losses and improve the overall efficiency of the system.

8. THD ANALYSIS

A cascaded H-bridge N-Level inverter uses a multi-carriers modulation system requiring (N -1) triangular carriers, all having the same frequency and amplitude. The triangular carriers are arranged vertically [32]. For a converter of N levels, the modulation index m is defined as $m = \frac{fc}{fr}$, with fc is the carrier frequency and fr is the reference frequency [33]. The voltage adjustment coefficient $r = \frac{Ac}{Ar}$, with Ar: Amplitude of the reference, and Ac: Amplitude of the carrier. At first, triangular multi-carriers with high frequency are made Figure 10, to generate the pulses for the MOSFETS:

- Configuration I: m =20, r = 1/7, f_r = 50 Hz and $f_C = f_r \times m$ = 1000 Hz.
- Configuration II: m = 20, r = 1/7, f_r = 50 Hz and $f_C = f_r \times m$ = 1000 Hz

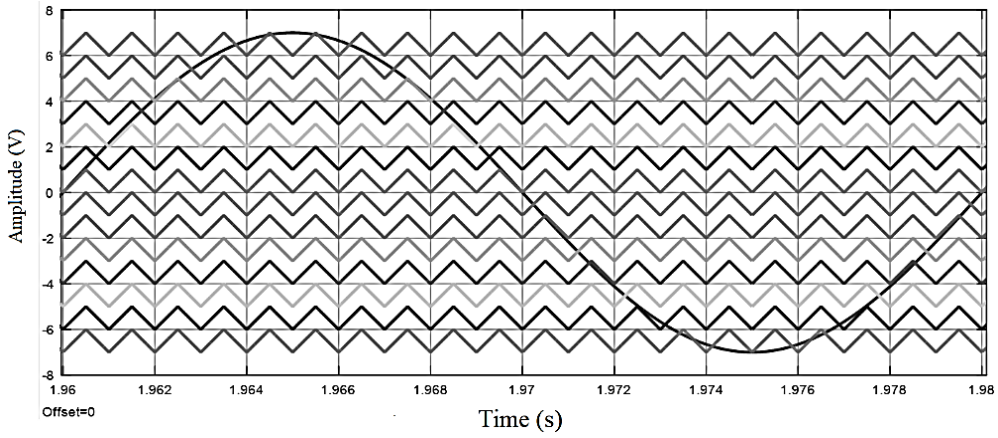


Figure 10. PD control scheme for a 15-level inverter

To achieve better performance in the output signal, a modification is made to the multi-carrier technique, as shown in Figure 11. This modification involves using a modified carrier with the same parameters aiming to enhance overall efficiency and effectively suppress the undesirable harmonic content, leading to a more refined and optimal signal representation. Moreover, the modified technique is implemented with diverse sinusoidal dispositions to evaluate their effectiveness, thereby determining the most optimal disposition. Through meticulous exploration of each technique's merits.

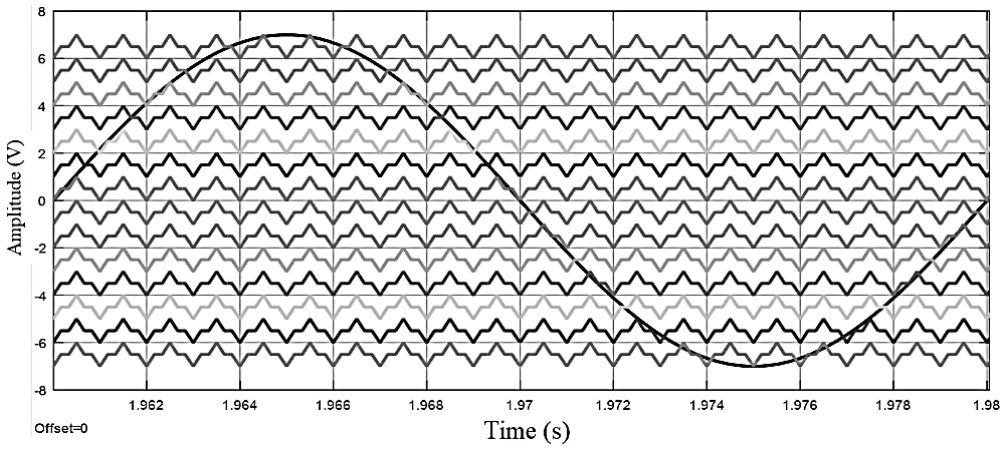


Figure 11. PD control scheme for a 15-level inverter with modified carriers

9. RESULTS

The output voltage waveforms and the harmonic distortions are obtained for different multi-carrier The results are obtained using triangular and the modified carrier techniques. These techniques are implemented with different sinusoidal dispositions PD PWM, POD PWM and APOD PWM to determinate the best technique for 15 LVL cascaded inverter. Figure 12 shows the output waveform and the harmonic spectrum for the 15 LVL inverter using phase opposite dispositions PD PWM. The total harmonic distortions are acquired for all the different configurations the conventional and the modified SPWM multi-carriers and represented on Table 3. A comparative study between 7 and 15 levels was shown in the following table to determinate the better technique for the H bridge inverter.

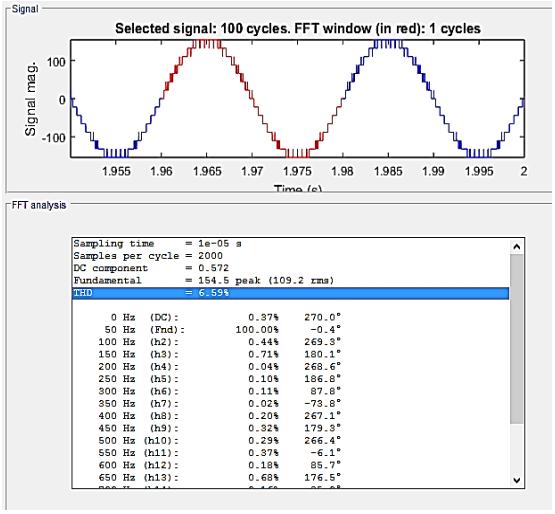


Figure 12. Harmonic spectrum analysis for a 15-level converter with phase opposite dispositions "POD"

Table 3. THD results acquired by the various control techniques

Triangular carriers	Cascade H-bridge with $f_c = 1\ k_{Hz}$, $f_r = 50$ Hz		
7-level	PD	POD	APOD
THD%	18.00	18.15	18.32
15-level	PD	POD	APOD
THD%	7.20	7.95	8.28
Modified carriers	Cascade H-bridge with $f_c = 1\ k_{Hz}$, $f_r = 50$ Hz		
7-level	PD	POD	APOD
THD%	14.77	16.01	15.36
15-level	PD	POD	APOD
THD%	6.59	6.71	7.20

– Results analysis

The total harmonic distortions acquired for both multi-carriers and analyzed in Figure 13 to determinate the best technique suited for cascaded multi-level inverter, Figure 13(a) is for the 7 LVL inverter and the Figure 13(b) is dedicated to the 15 LVL inverter.

i) Increasing the number of "N" levels significantly escalate the quality of the output signal.
ii) Modifying the triangular carriers gives better results in all types of multi –level inverters.

This modification is better suitable for cascaded H-bridge multilevel inverters with an improved voltage signal quality.

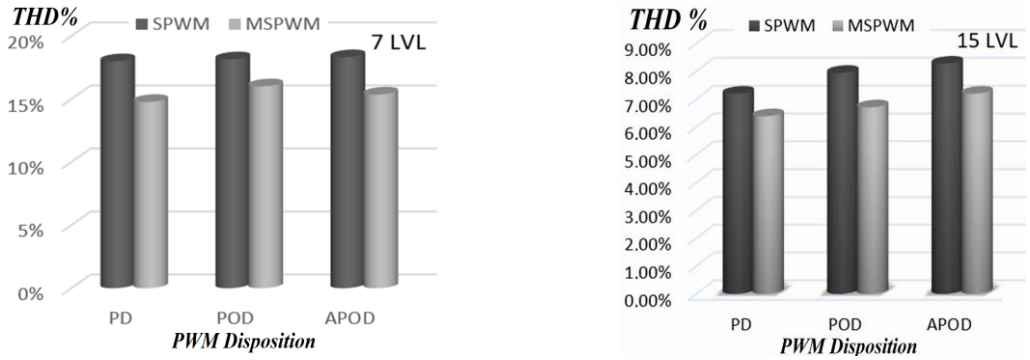


Figure 13. THD analysis (a) THD comparative for 7 LVL inverter and (b) THD comparative for 15 LVL inverter

10. CONCLUSION

Nowadays, the improvement of power quality and the interconnection between different networks require more and higher power electronic interface and power switching devices; multilevel converters are typically adjusted to these applications. In all existing multilevel converter topologies, the higher the number of levels, the more complicated the converter structure becomes. This increases its cost and the complexity of its control schemes. Three major structures of multilevel converters have been stated in the literature: cascaded h-bridges (CHB) with separate DC voltage sources, neutral point clamped (NPC) diodes, and flying capacitors (FC), among the multilevel topologies presented, the modular aspect of the H-bridge inverter caught our attention and then the focus was made on these types of H-bridge converters.

The development of the new multi-level will allow each string of PV panels to operate independently; as a result, it won't be extremely affected by shades or intermittence and can be easily replaced by batteries if facing some defaults. This paper also proposes the development of a better control strategy to generate a voltage closer to the sinusoidal form. For this purpose, different strategies of pulse width modulation have been established. The applied control techniques are made, and their performances are compared in terms of output voltage quality in order to reduce harmonics, the control used in this work is the sinusoidal modulation SPWM. Two strategies were tested on the 15-and 7-level. Results proved that the Modification carrier-based control shows better results.

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