Elliptical Alignment Holes Enabling Accurate Direct Assembly of Microchips to Standard Waveguide Flanges at sub-THz Frequencies

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***Abstract*— Current waveguide flange standards do not allow for the accurate fitting of microchips, due to the large mechanical tolerances of the flange alignment pins and the brittle nature of Silicon, requiring greatly oversized alignment holes on the chip to fit worst-case fabrication tolerances, resulting in unacceptably large misalignment error for sub-THz frequencies. This paper presents, for the first time, a new method for directly aligning micromachined Silicon chips to standard, i.e. unmodified, waveguide flanges with alignment accuracy significantly better than the waveguide-flange fabrication tolerances, through the combination of a tightly-fitting circular and an elliptical alignment hole on the chip. A Monte Carlo analysis predicts the reduction of the mechanical assembly margin by a factor of 5.5 compared to conventional circular holes, reducing the potential chip misalignment from 46 µm to 8.5 µm for a probability of fitting of 99.5%. For experimental verification, micromachined waveguide chips using either conventional (oversized) circular or the proposed elliptical alignment holes were fabricated and measured. A reduction in the standard deviation of the reflection coefficient by a factor of up to 20 was experimentally observed from a total of 200 measurements with random chip placement, exceeding the expectations from the Monte Carlo analysis. To our knowledge, this paper presents the first solution for highly accurate assembly of micromachined waveguide chips to standard waveguide flanges, requiring no custom flanges or other tailor-made split blocks.**

***Index Terms*—alignment, micromachining, waveguide flange, submillimeter-wave, calibration. (*IMS Abstract*)**

I. Introduction

Waveguide flange alignment is a known source of measurement error, degrading return loss and increasing insertion loss. Previous works have shown that this is the main source of error during THz waveguide measurements [1]. At higher frequencies, where potential misalignment of the waveguides approaches the size of the waveguide itself, this error can be significant enough to prevent accurate measurement of the device under test [2]. Alignment between waveguide flanges is facilitated by alignment pins fitting to alignment holes of the opposite flange. Misalignment is caused by multiple fabrication tolerances of these alignment features. To make matters worse, specified and delivered fabrication tolerances vary greatly between manufacturers of precision waveguide flanges. When merging metal to metal flanges, these tolerances are accounted for by a slightly larger alignment hole diameter and by slight compliance of the alignment features due to small plastic deformation.

At submillimetre-wave and THz frequencies, micromachined waveguide devices and systems become increasingly attractive since they allow for high-precision features, high product uniformity, and even re-configurability via integrated MEMS actuators [3], [4]. For integration in complete systems and measurement/verification, micromachined waveguide components must be connected to waveguide flanges.

Unfortunately, all microchip materials, including Silicon, III-V semiconductors and glass materials, are very brittle and any mechanical stress generated by the alignment pins of the flange would instantly break a chip made in such materials. Thus, the alignment holes on the chip must be greatly oversized such that even the worst-case combination of the multiple flange alignment-features fabrication tolerances does not result in the alignment pin touching the microchip. Such oversized alignment holes ensure high fitting probability but result in a large range of chip motion and thus greater measurement error. For this reason, direct assembly of microchips onto standard high-precision waveguide flanges is deemed to be practically infeasible [5]. Several highly-complicated and challenging work-arounds have been developed to alleviate the difficulty of assembling and aligning micromachined waveguide systems, including split-block designs housing the microchips with high-precision alignment features between the splitblocks and the microchips [3], [6], or high-accuracy alignment features machined into the waveguide flanges [7].

Here, we present, for the first time, a new technique allowing accurate direct assembly of microchips to standard waveguide flanges, which requires no custom flanges or tailor-made split block assemblies.

II. New Alignment Concept Combining a Tightly-fitting Circular and an Elliptical Alignment Hole

Fig. 1a shows the outline of a microchip to be aligned with a standard waveguide flange. As detailed above, for conventional fitting methods, the alignment holes on the chip must be significantly oversized in order to avoid breakage of the chip. The worst-case combination of the following flange alignment-features tolerances must be accounted for: (1) pin position accuracy in x: ±25 µm; (2) pin position accuracy in y: ±25 µm; (3) pin diameter accuracy: 1,562 +0 –13 µm (all IEEE 1785.2a standard); and an additional fitting margin of 0-10 µm to guarantee insertion of the pin in the hole. The additive nature of these tolerances is shown graphically in Fig. 1b, showing the overall tolerance space and thus required oversized alignment-hole diameter d on the microchip, with large

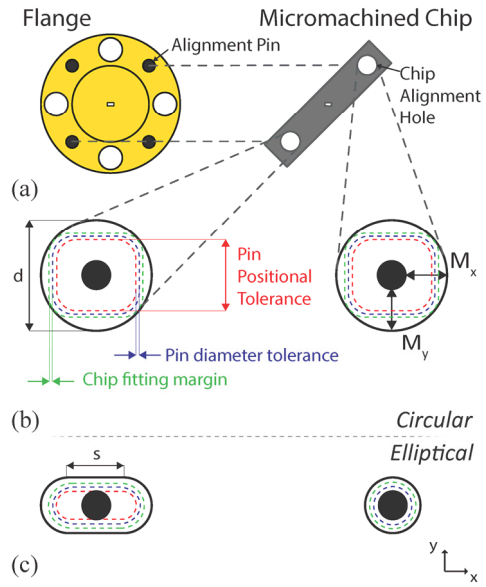


Fig. 1: (a) Fitting of microchip on standard flange; (b) conventional concept: oversized alignment holes required to fit all worst-case fabrication tolerance combinations of the flanges, to avoid breakage of the brittle chips; (c) proposed new concept: tightly fitting circular hole (right), vastly limiting chip movement, and "elliptical" alignment hole (left), accommodating flange alignment-pin positioning tolerances.

assembly margins M_x and M_y in the x and y directions, respectively.

In contrast, Fig. 1c shows the novel concept of combining a very tightly fitting circular alignment hole (right) and an "elliptical" hole, where the geometry of the hole has the form of a rounded slot of length s. Here, the tightly fitting hole reduces the overall movement of the chip to just the fitting margin and the relatively small pin-diameter tolerances, while the elliptical hole accommodates for the fabrication tolerances of the alignment-pin positions. Any y-axis alignment pin offset is compensated for by a small rotation of the chip. This rotation is negligible since it is a factor of 1,000 times smaller than the distance between the alignment holes, resulting in a maximum chip rotation of a few milli-rad.

III. Monte-Carlo Simulation Model and Results

A Monte Carlo simulation model was implemented in MATLAB to determine the probability of random variations of all combined fabrication tolerances of the flange alignment pins fitting a given geometry of alignment holes on a microchip. The randomly distributed pins are said to fit the chip if they lie completely inside the chip holes, i.e. do not come into contact with the chip-hole perimeters. The Monte Carlo simulation model is run 100,000 times for each alignment-hole geometry, from which the overall probability of fitting and the maximum (worst case) margin of movement of the chip is calculated. This margin determines how much the chip can move around the pins. For the data shown in this paper, a 3

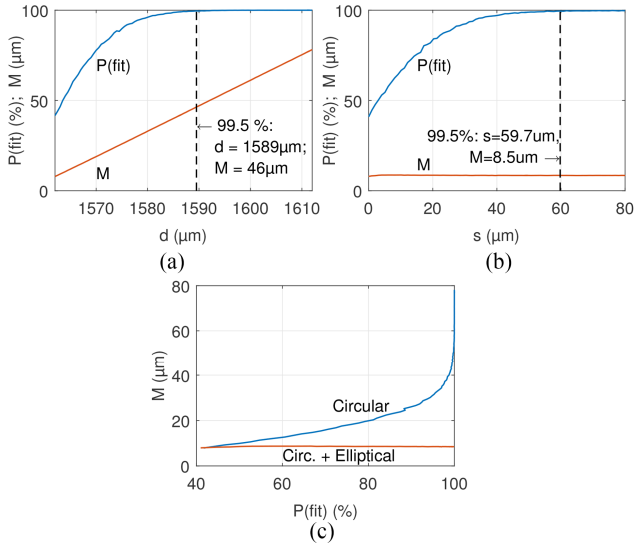


Figure 2: Monte Carlo Simulation Results for the IEEE 1785.2a standard: probability of fitting and total assembly margin M for (a) conventional oversize circular holes and (b) the proposed circular + elliptical configuration. (c) A comparison of M for given probability of fitting for both concepts.

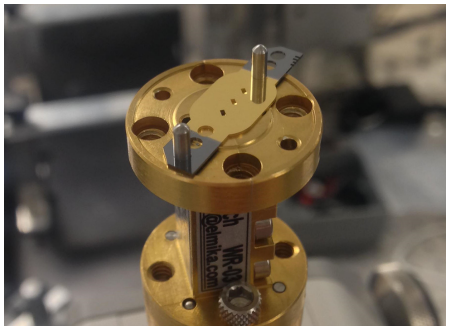
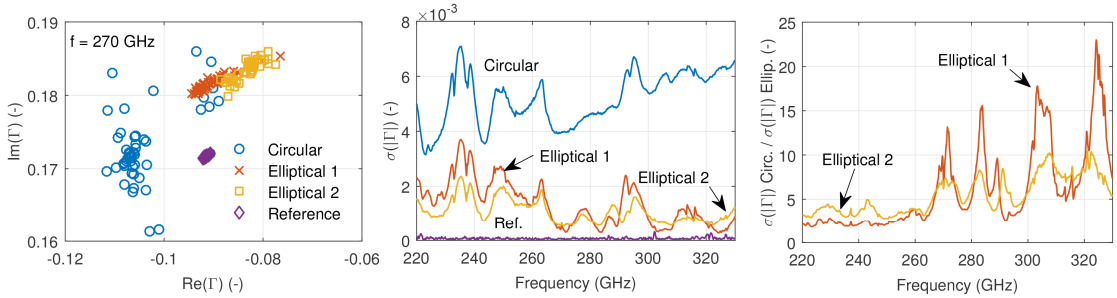


Figure 3: A fabricated micromachined waveguide shim placed on a WR-3.4 flange, which is vertically oriented.

sigma Gaussian distribution is assumed for all mechanical tolerance values, based on information supplied by the flange manufacturer.

The results of the Monte Carlo simulation for conventional over-sized circular alignment holes are presented in Fig. 2a, where the probability of fitting $P(fit)$ and maximum (vector length) assembly margin M are plotted versus d. Due to the flange fabrication tolerances, a fitting probability of 99.5%, deemed to be the minimum requirement for a high-confidence assembly, is reached only if the alignment holes on the microchip have a diameter of 1,589 µm. This large, but necessary, oversizing results in a maximum assembly margin of 46 µm, which is inacceptable for submillimetre-wave frequencies [5].

In contrast, Fig. 2b shows the Monte-Carlo simulation results for the proposed circular + "elliptical" hole combination. Here, the length of the rounded slot (s) is the optimization parameter which determines the probability of fitting. This superior alignment hole geometry results in 99.5% fitting probability for a slot length of 59.7 um. The resulting maxi-



(a) (b) (c)

Figure 4: Experimental results: (a) distribution of the measured reflection coefficient, for conventional oversized circular holes (circle), and 0um (cross) or 5um (square) margin of the proposed circular+elliptical hole concept, 50 measurements each; (b) standard deviation of $|\Gamma|$ for the three implementations over frequency; (c) ratio of standard deviations between new concept (0, 5um margin) and conventional concept.

mum margin of chip movement is only 8.5 um, i.e. a factor of 5.5 times smaller than that of the conventional holes. The fitting probability vs average assembly margin of the two concepts is plotted in Fig. 2c, clearly showing the improvement of the new concept.

IV. Experimental Verification

300 µm thick Silicon micromachined waveguide shims were fabricated as test chips to evaluate the proposed alignment-hole concept in the 220-330 GHz frequency band. Measurements of the reflection coefficient of a single shim were performed using a one-port radiating open configuration. The radiating open has previously been presented as an ideal standard for the measurement of shim offsets [2] as its electrical parameters are well known and it allows for the influence of the shim alone (without a connecting flange or other termination) to be examined. Following previous works [2], [8], the VNA frequency extender (Rohde & Schwarz ZC-330) was positioned vertically, thereby negating the effect of gravity on the alignment of the shim. This also serves to ensure that the contact between the shim and the flange is highly repeatable between sequential measurements. An example of one of the fabricated shims is shown in Figure 3.

To assess the repeatability of each alignment method, 50 repeated measurements of the reflection coefficient of the radiating open plus shim combination were made. The shim was fully replaced on the flange pins between each measurement. The VNA was calibrated using a standard Short-Open-Load algorithm and an IF bandwidth of 50 Hz, no averaging, was used throughout calibration and measurement. All data was acquired within 1 hour following calibration, to reduce any influence of thermal drift on the results. The thermal environment of the laboratory was fairly constant throughout, at T ≈ 25 ◦ C, RH ≈ 13%.

Fig. 4a shows the distribution of the measured reflection coefficient in the complex plane, with 50 measurements for every chip, at the center frequency of 270 GHz. For chips with conventional alignment holes the distribution is significantly larger than those designed for the same probability of fitting (99.5 %) with the proposed circular + elliptical concept, which was tested for chips with 0 and 5 um fitting margin. As reference, the spread of 50 measurements with no chip replacement shows the actual measurement setup repeatability. The standard deviation of the magnitude of the reflection coefficient over the complete frequency band is shown in Figure 4b. These measurements show a huge improvement of the chip-to-flange alignment repeatability over the conventional strategy: for the lower part of the WR-3.4 frequency band, the standard deviation is reduced by a factor of about 2-5, whereas for the upper frequency band, the standard deviation is reduced by a factor of 5-20, as shown in Figure 4c.

V. Conclusion

This paper presented, for the first time, a new concept to accurately fit microchips onto standard (IEEE 1785.2a) waveguide flanges, enabling direct-chip-to-flange assembly for submillimeter-wave frequencies, which so far was practically infeasible with the conventional oversized-hole strategy. The alignment accuracy of the new concept was compared to the conventional one by Monte-Carlo simulations, showing an alignment accuracy improvement by a factor of 5.5. In the experimental part of this paper, the reduction in measured standard deviation of $|\Gamma|$ in the upper part of the WR-3.4 band was found to be 5-20, as determined via statistical analysis of the measured reflection coefficient of a total of 200 random measurements.

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