Low-cost Si substrates from Si scraps and Si kerf: EU project Cabriss

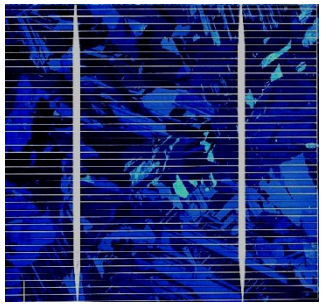
Alexander Ulyashin

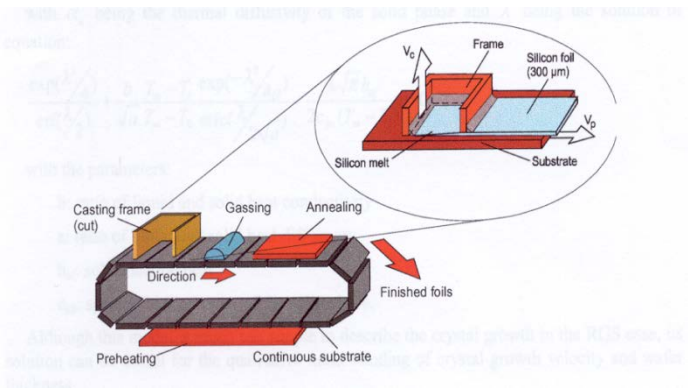
SINTEF, Oslo, Norway
and
CABRISS consortium

Si solar cell roadmap: low cost Si wafers/reduction of Si-content

Mono-Si → Multi-Si → Si-ribbons → Fast ribbon growth

Si-content





Self-supporting Si substrates/Si wafer based solar cells

Si substrates: Thin Si substrates < 100 µm;

exfoliated Si foils;

Si solar cells: HIT /MWT/EWT/IBC/BiFi solar cells

First generation PV: advanced concepts, lower Si content, kerf-less approaches, utilization of Si kerf, low-cost processing technologies, …., are still required

Si solar cell roadmap: Thin-film Si solar cells/reduction of Si-content

Si-content

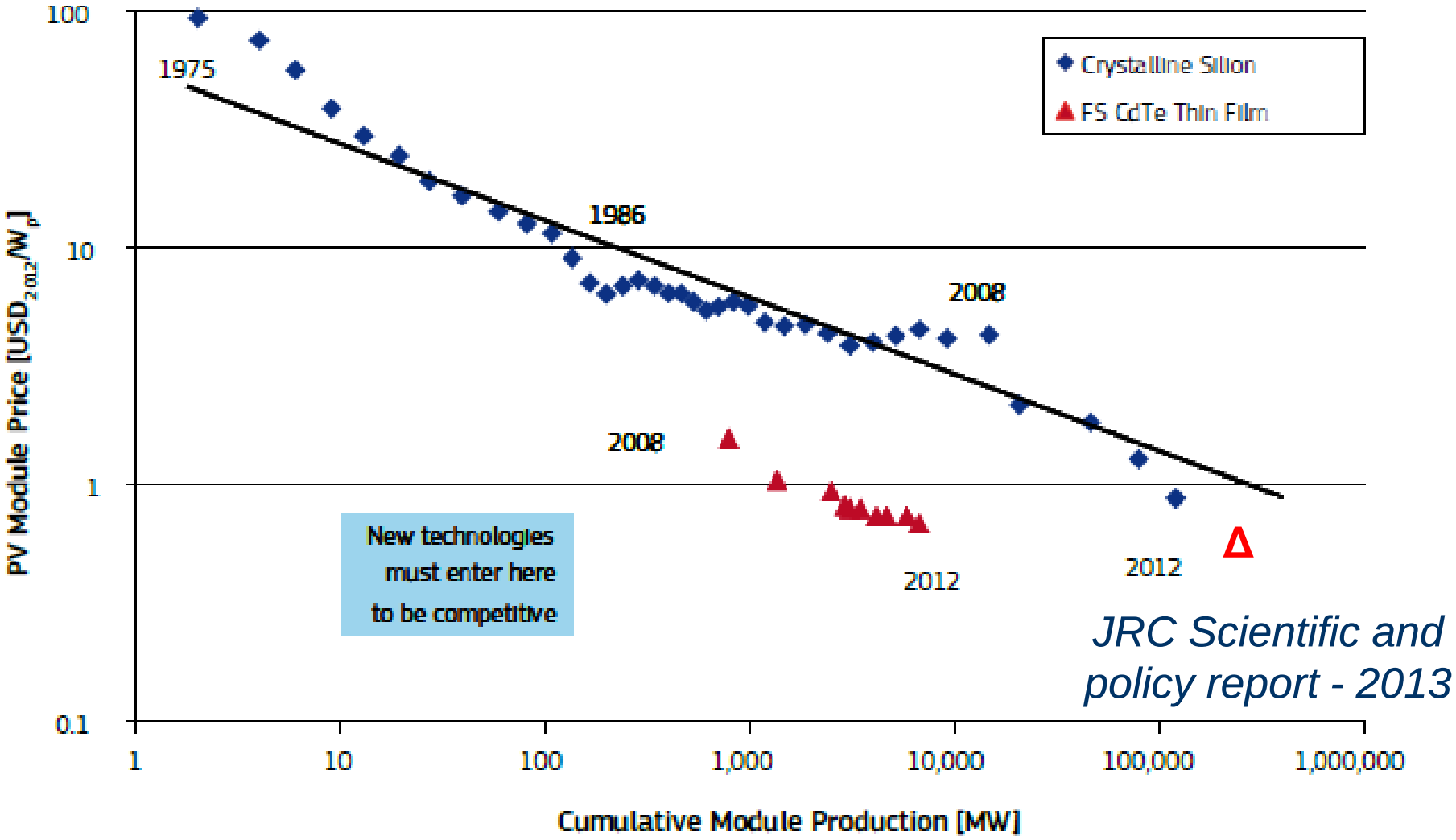
Epitaxial cells on low-cost substrates: 20–30 μm

Polycrystalline Si cells grown at high temperatures or obtained by SPC, 3–10 μm

a-Si:H → microcrystalline Si / grown at temperatures < 300°C, 1 – 2 μm

Second generation PV, advanced concepts are still required, low-cost processing, ….

Unexpected decrease of solar cell module prices



JRC Scientific and policy report - 2013

Recycling in combination with general trends in Si PV

IMPLEMENTATION OF A CIRCULAR ECONOMY BASED ON RECYCLED, REUSED AND RECOVERED INDIUM, SILICON AND SILVER MATERIALS FOR PHOTOVOLTAIC AND OTHER APPLICATIONS

CABRISS

Recycling of Si /Si losses

Si kerf ~ 50% loss of Si feedstock

Si scrap: broken wafers, broken solar cells ~1-2% loss of Si

Extraction of Si from the end-of-life panels

Cost reduction for first and second generations of Si PV

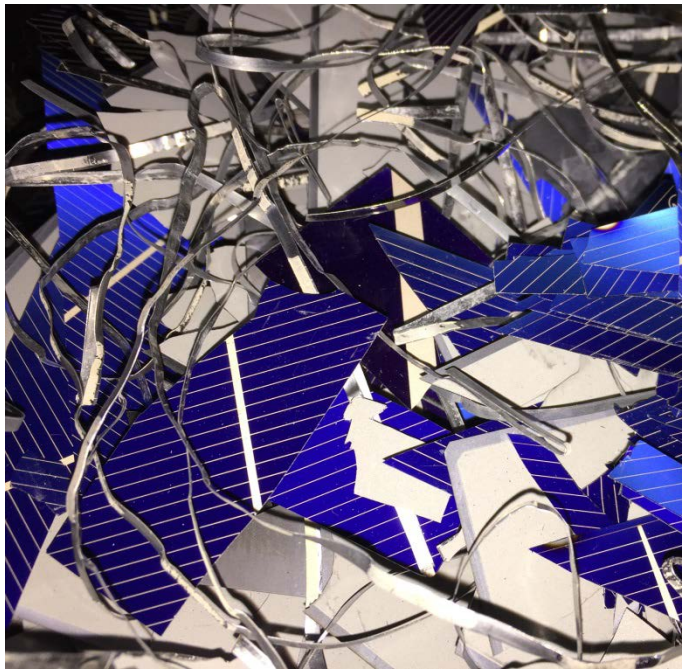
Recycling of Si

Si scrap: broken wafers, broken solar cells ~1-2% loss of Si

- PV collection, selection and dismantling …
  - Loser Chemie & PV Cycle

Materials extraction from Si PV waste Loser Chemie

Example Si waste/Si scrap



delivered de-metallized Silicon ✓

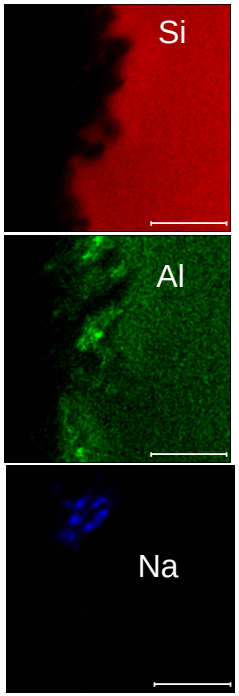
SINTEF

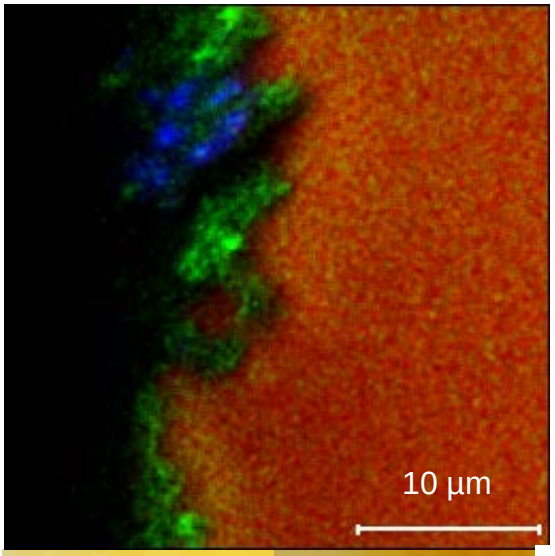
cea

Silicio FerroSolar
Grupo FerroAtlántica

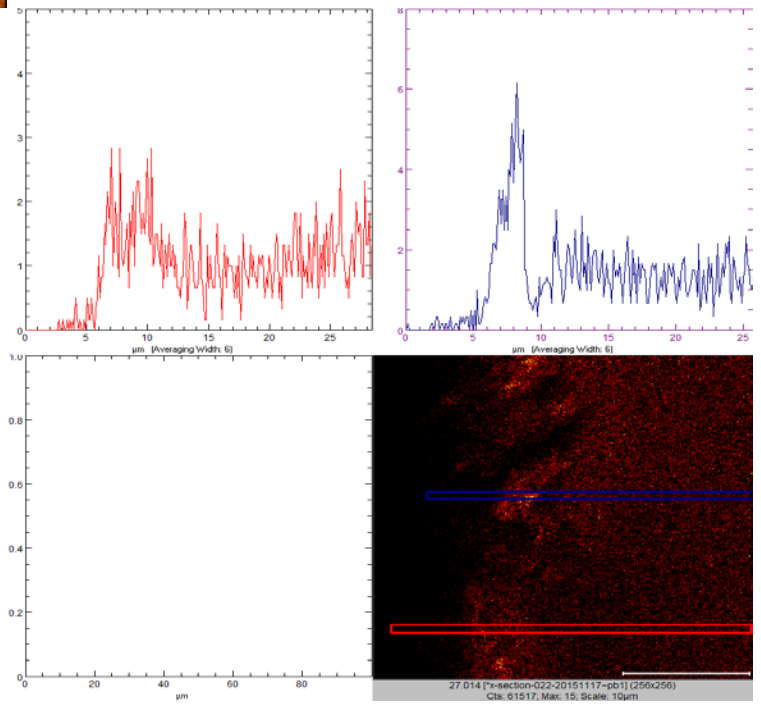
?

Recycling of Si scrap



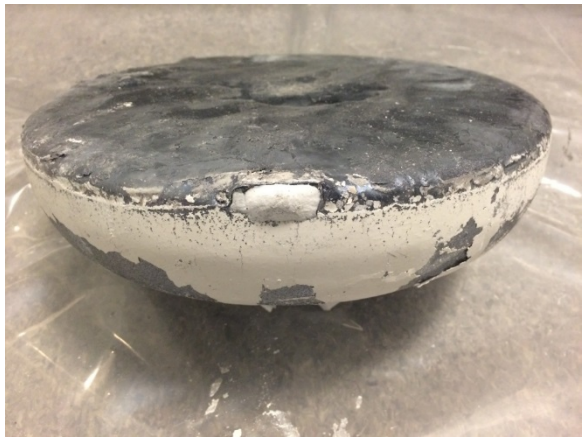


Aluminum/Tof-SIMS



Recycling of Si /solar cells

G1 Multi-Si from Si scrap (Loser/SINT) shiped to THM for wafering



Solar cell processing at the Solitek industrial line

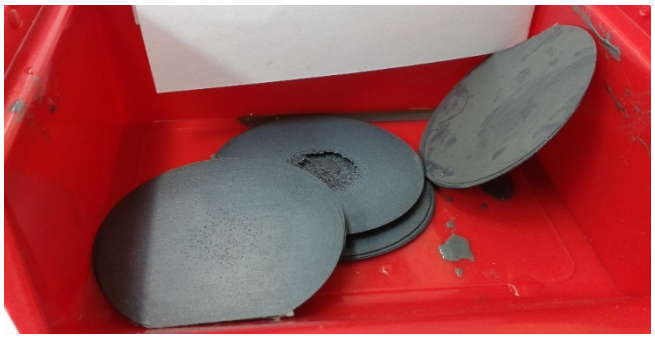
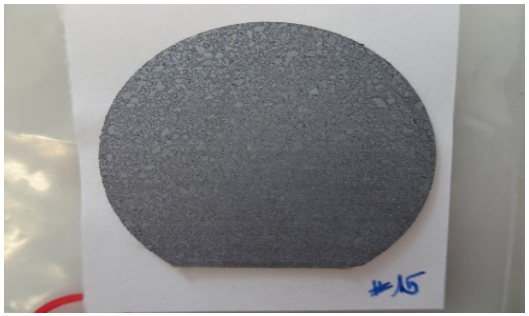
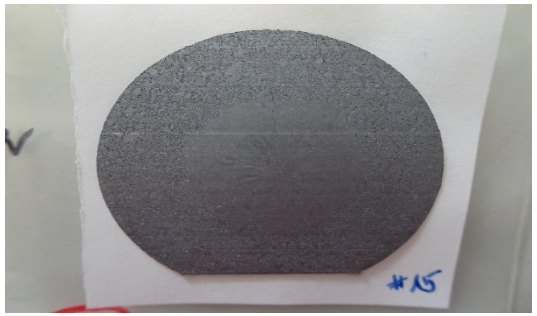
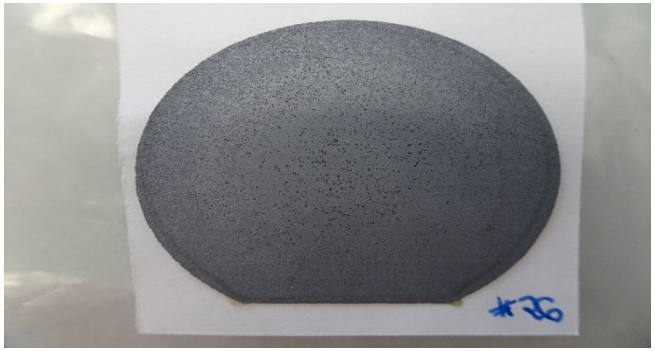
Title	Wafer count	Eta (%)	Voc (mV)	Jsc (mA/cm2)	FF(%)
Cabriss 4 (reference ingot from SINTEF)	78	17.24	627	34.7	79.19
Cabriss 6 (Si scrap)	37	17.26	625.3	35.3	78.18
Reference process at Solitek	1000	17.67	628	35.7	78.53

Recycling of Si /Si powder based concept

Hot pressing/Spark plasma Si powder based wafers, 40 mm diameter (SINTEF) + wafering (THM)

Wafering of Si powder based sintered ingots is possible:



1200 ◦C

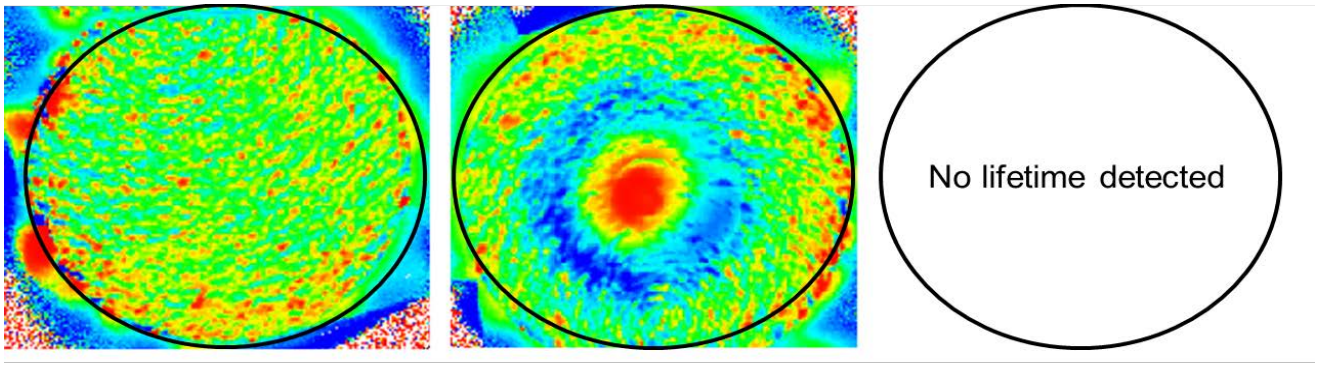
1250 ◦C

1200 ◦C

Recycling of Si /Si powder based concept

Minority carrier lifetime measurements at THM

Undoped solar grade Si powder **p+ (Boron) Si powder**

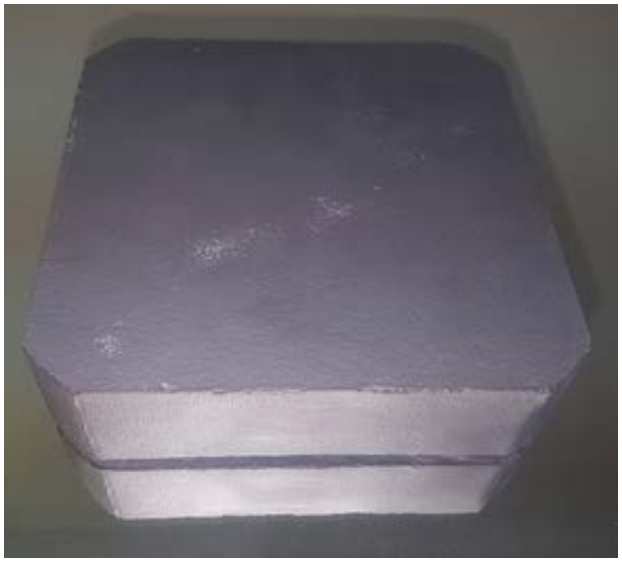


Sample	LT Minimum [µs]	LT Maximum [µs]	LT Median[µs]	Resistivity [Ohm cm] (Median of 5 measurements)
1	0.3	57.8	22.6	287.1
2	0.4	42.6	20.4	11.4
3	-	-	-	3.2×10^{-4}

Recycling of Si /Si powder based concept

Ingot with 156mm x 156mm x 100 mm manufactured by direct hot pressing by RHP.

Wafering at THM (to be done)



Silicon and Boron doped Si-ingots

Recycling of Si /Si kerf

Si kerf- Resitec / Si ingots-SINTEF

Cabriss 1 (100% of Si kerf)

Cabriss 2 (100% of Si kerf)

Cabriss 10 (5% of refined Si kerf)

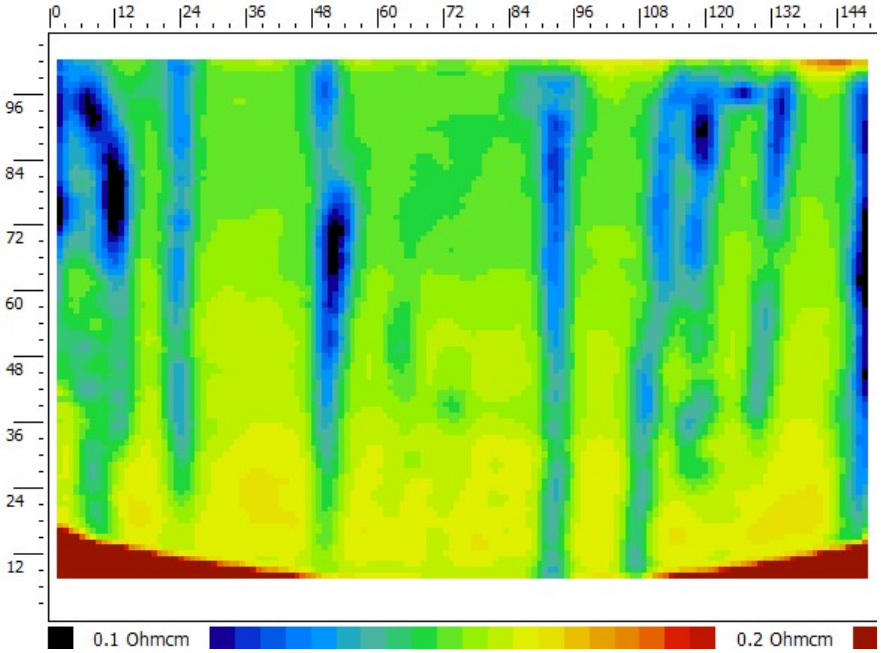
SINTEF purification of Si kerf via melting

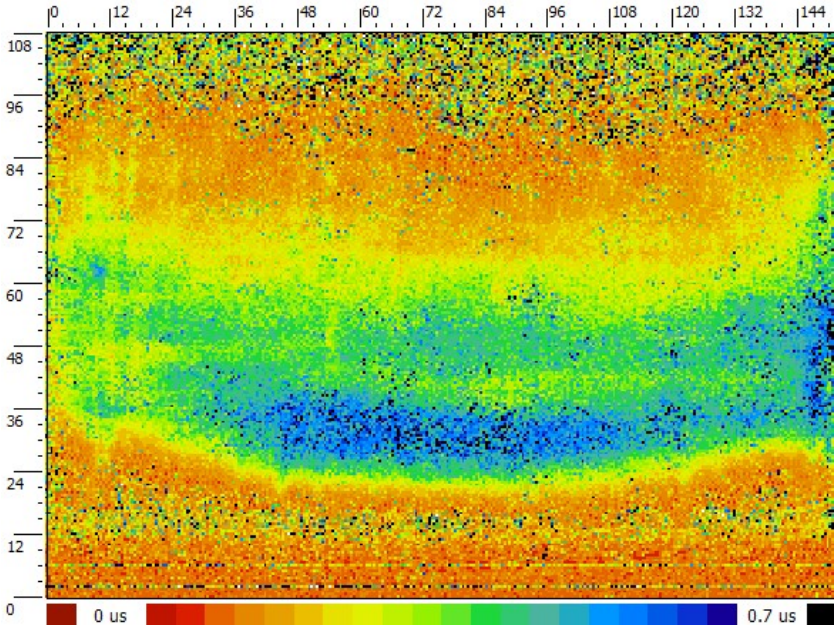
Cabriss 11 (100% of refined Si)

Recycling of Si /Si kerf

THM: Multicrystalline bricks CABRISS 10 : 5% of refined Si kerf

- CABRISS 10: resistivity 0.1 – 0.2 Ωcm
- Carrier lifetime < 1 µs

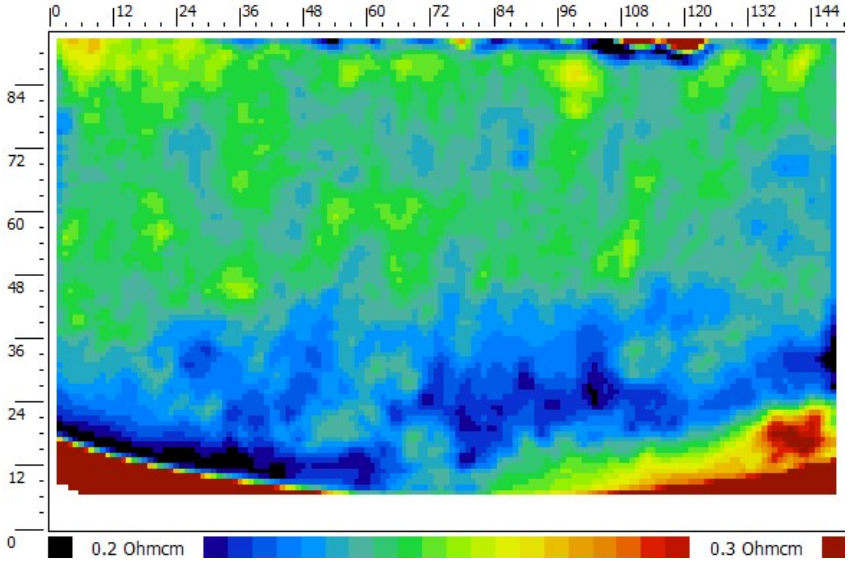




Recycling of Si /Si kerf

THM: Multicrystalline bricks CABRISS 11 (100% of refined Si kerf)

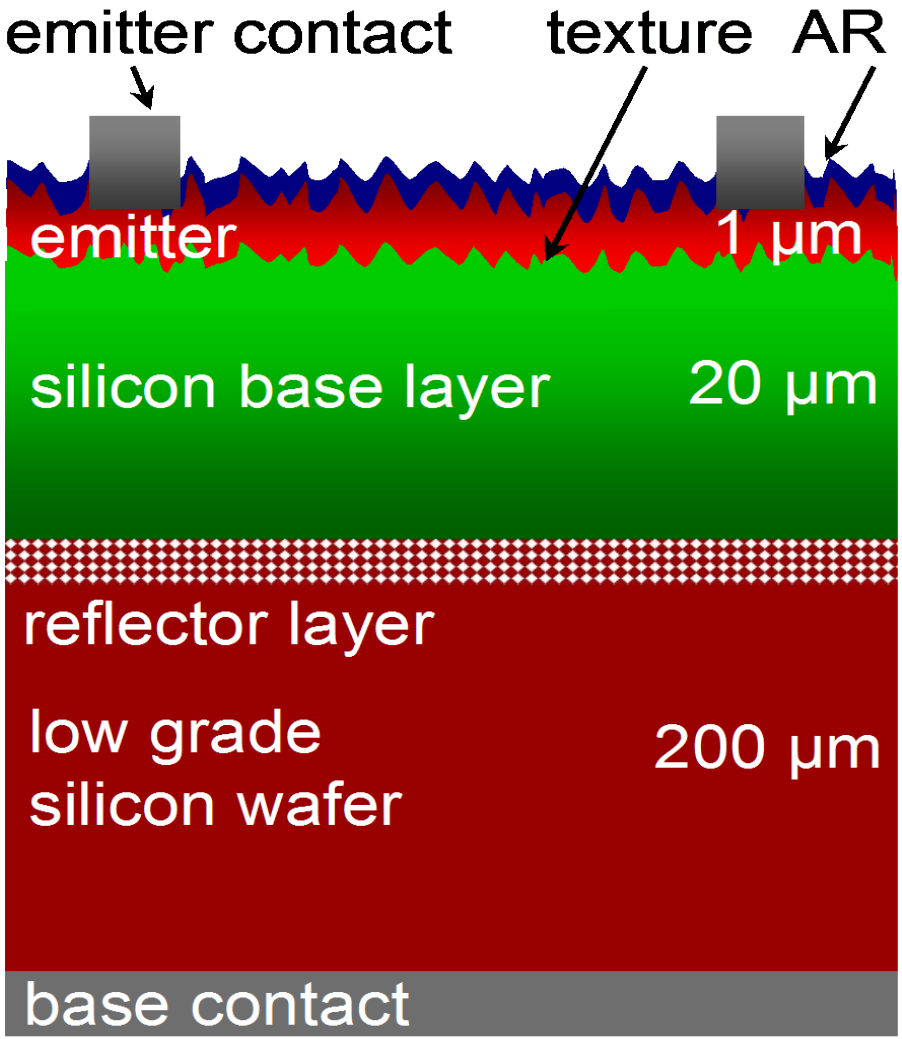
- CABRISS 11: reistivity 0.2 – 0.3 Ωcm
- No carrier lifetime detectable → resistivity is not the only reason for low lifetime, impurities must be present in high concentration



No carrier lifetime detectable

Wafering of Si kerf based ingots ??? THM

Si wafer equivalents /Si kerf/Si powder wafers/thermal spray of Si powders



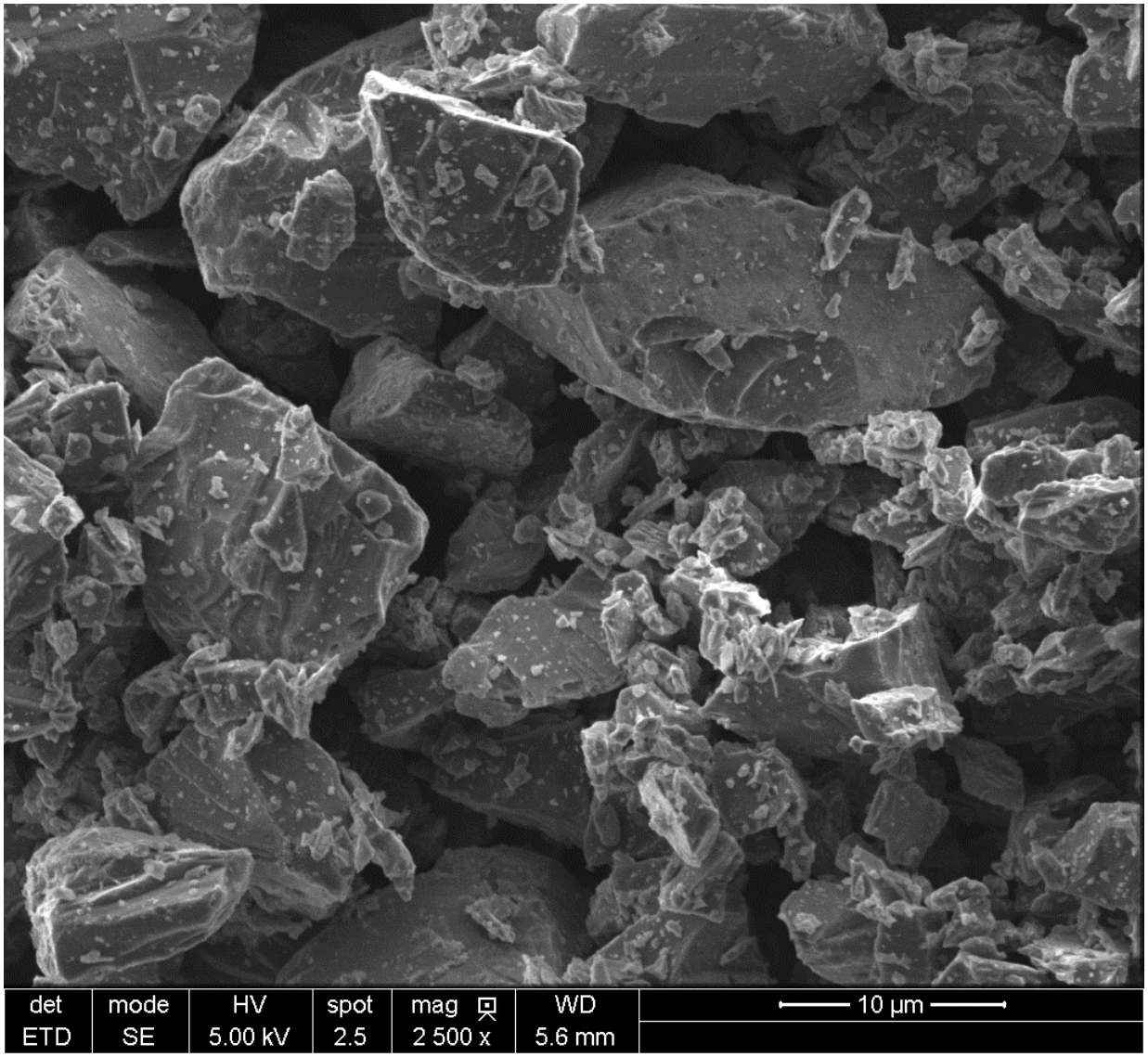
Solar grade Si

Bonded Si foils (IMEC)
Thermal spray of Si layers (Pyrogenesis)
E-beam deposition (SINTEF)
CVD ???

Low-cost/low grade Si

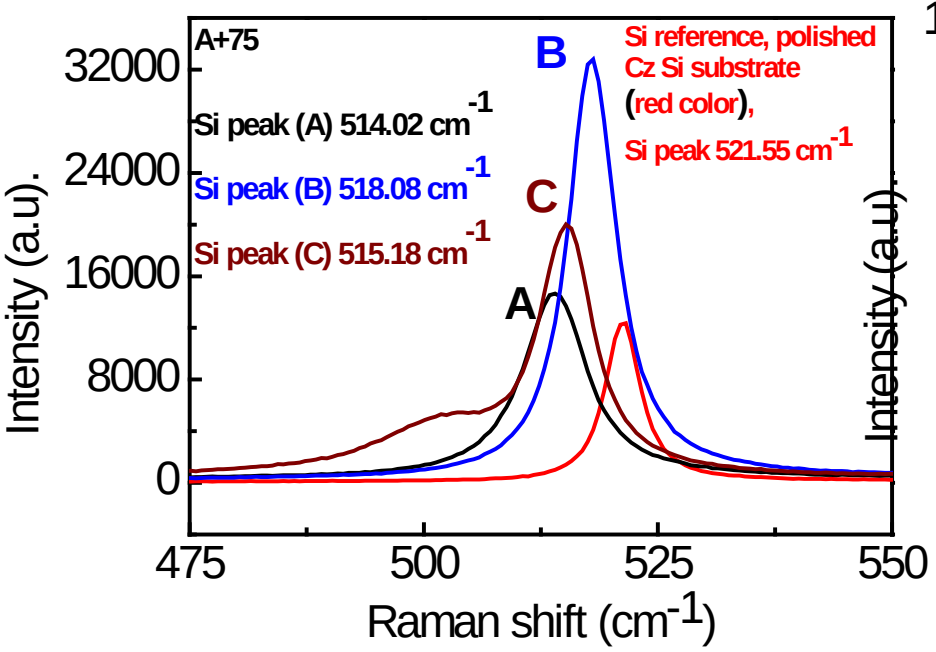
Si powder based substrates
Si kerf based substrates
Thermal spray based substrates

Si powder-to-substrate/layer approach/thermal spray

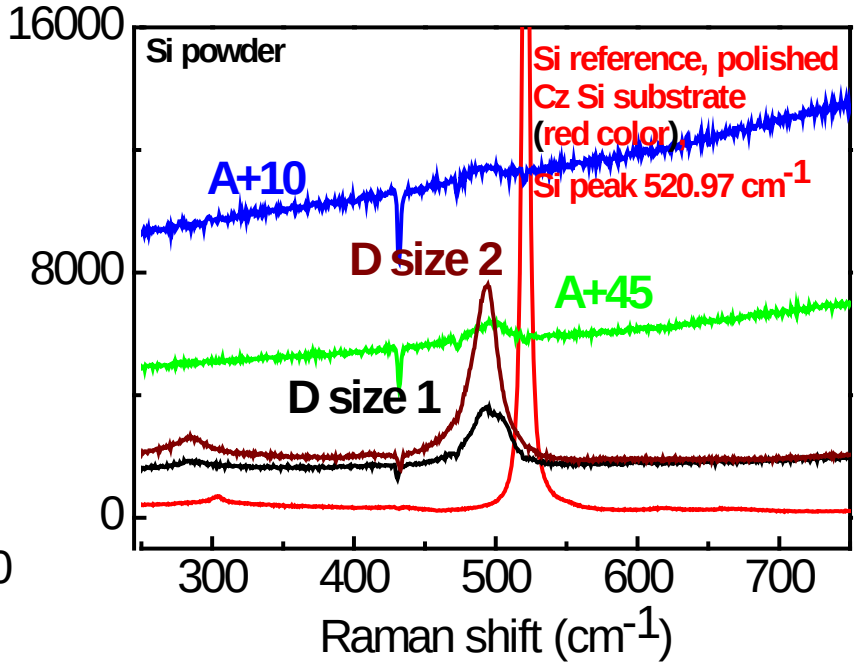


Requirements for Si powder/Raman

Mapping of individual Si particle

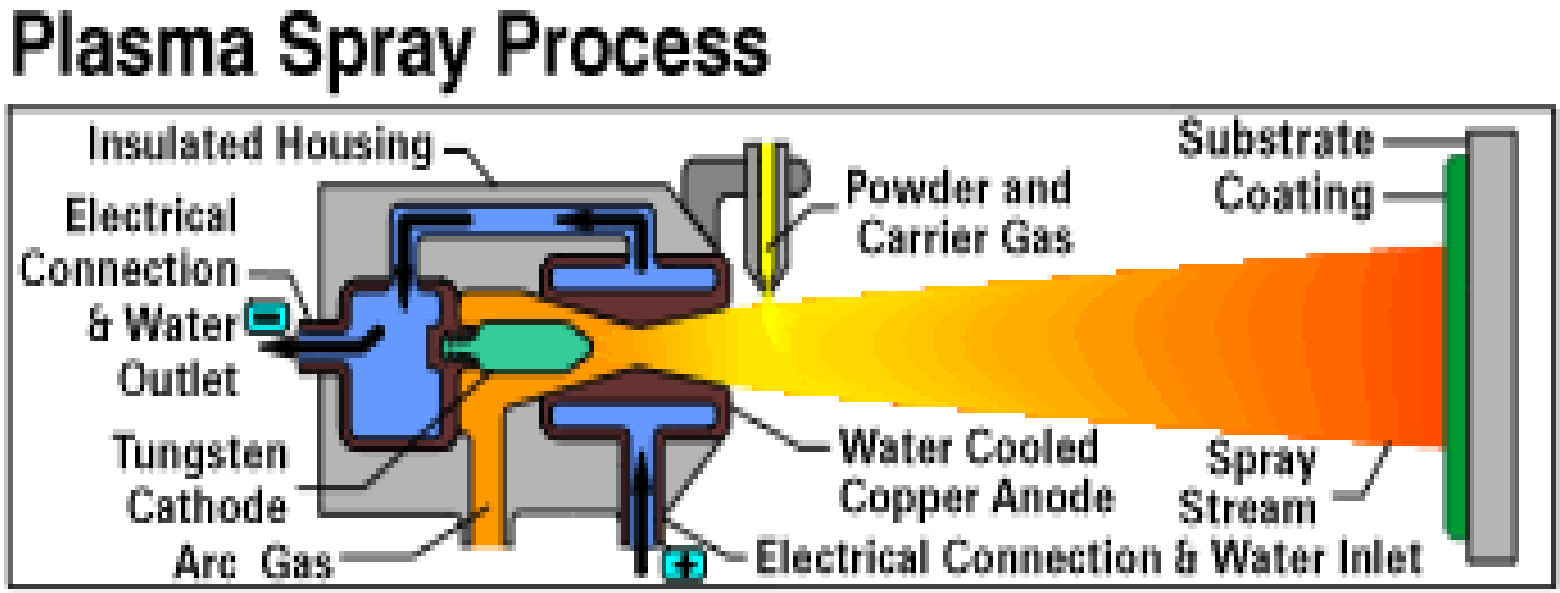


Different types of Si powder



Conclusion: Si powder sub-surface regions are not fully crystalline

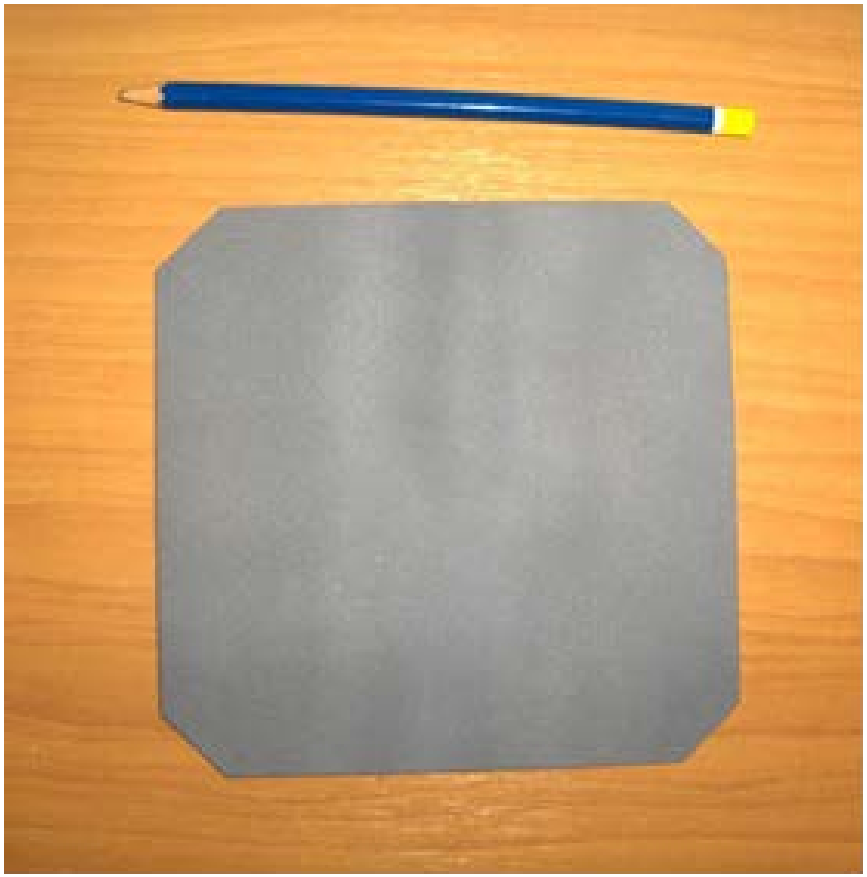
Atmospheric Plasma Spray (APS) gun



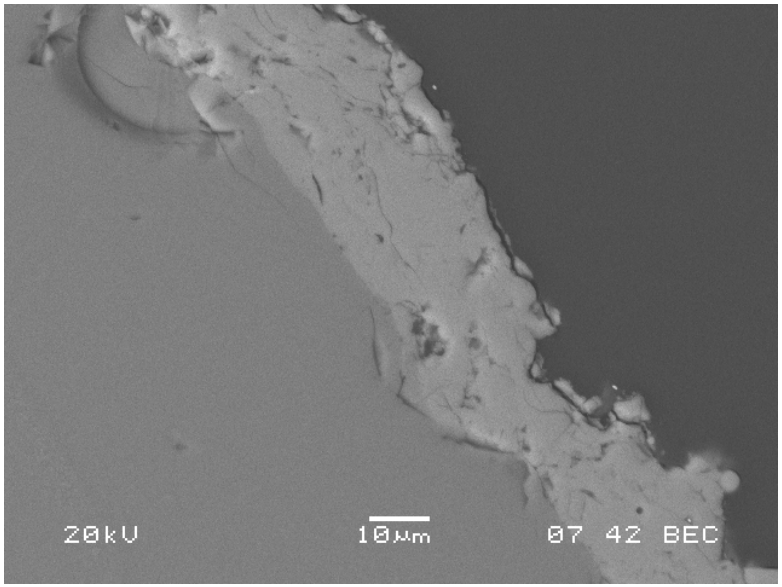
Low cost Si substrate made by TS with dimension 50x65 mm2

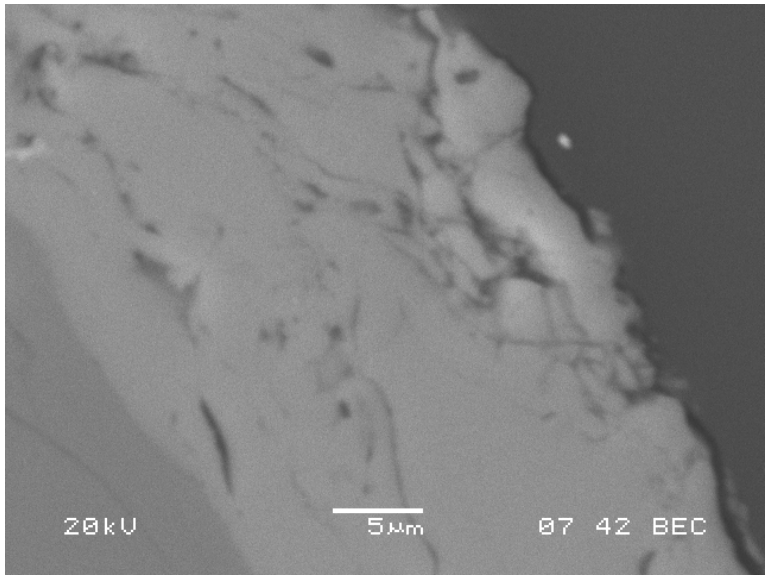
Si powder-to-substrate/layer approach/Pyrogenesis

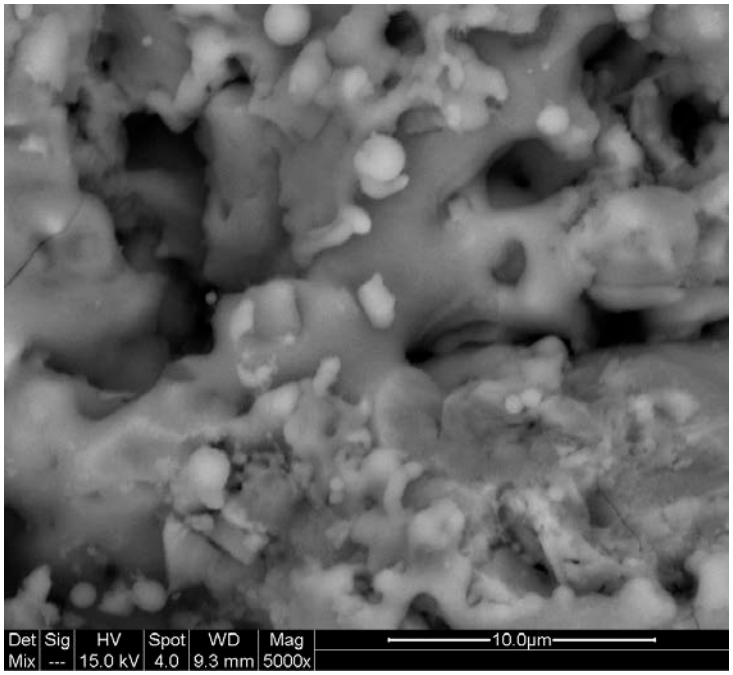
Low cost Si substrate made by TS with dimension 156x156 mm2



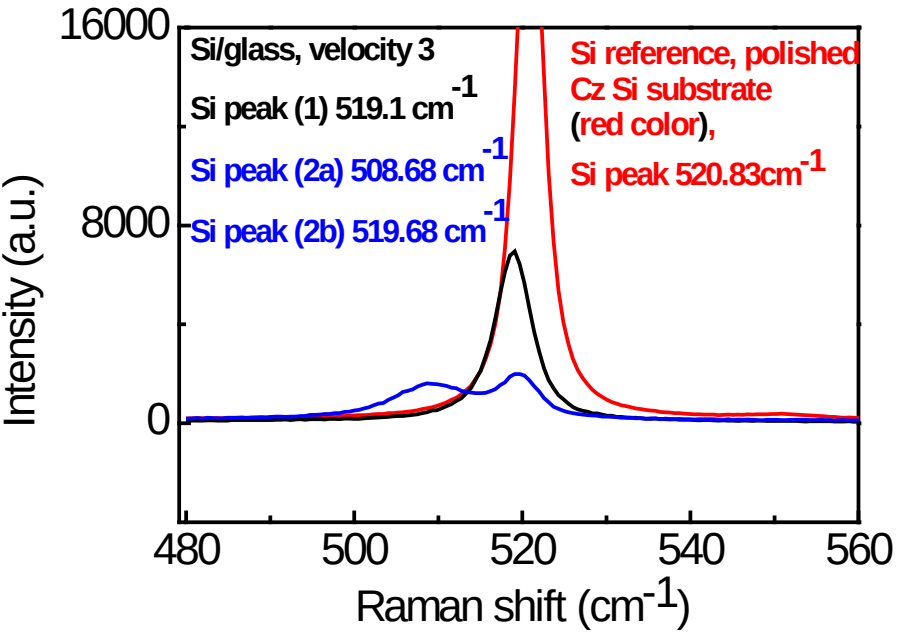
Si low cost layers on glass/ thermal spray/SEM



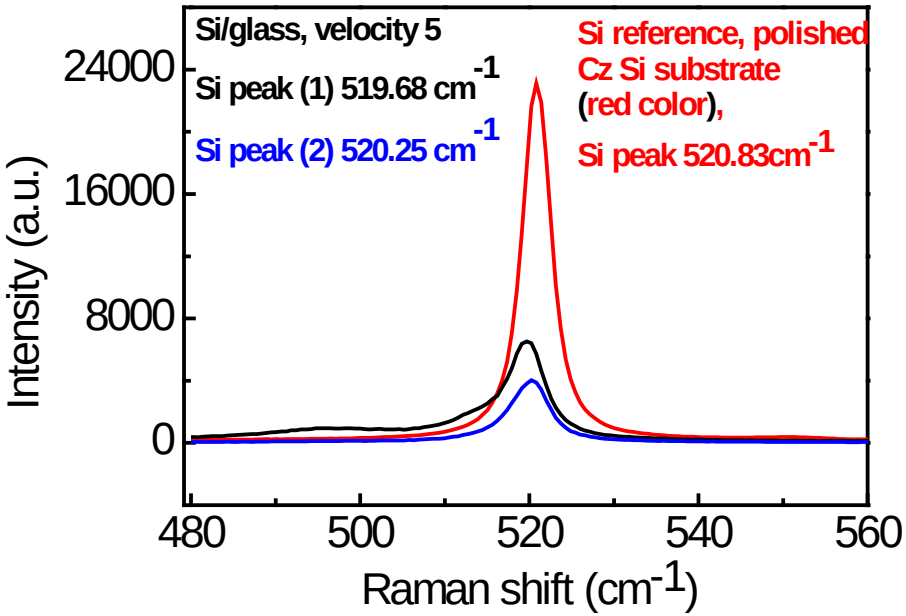




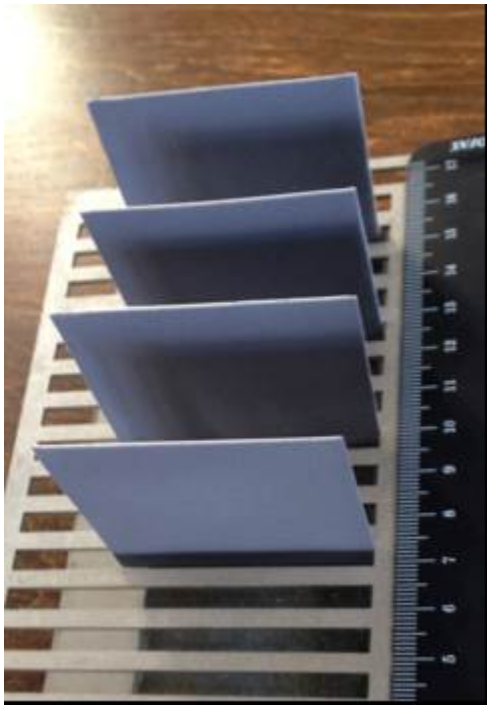
Thermal spray scanning velocity 3

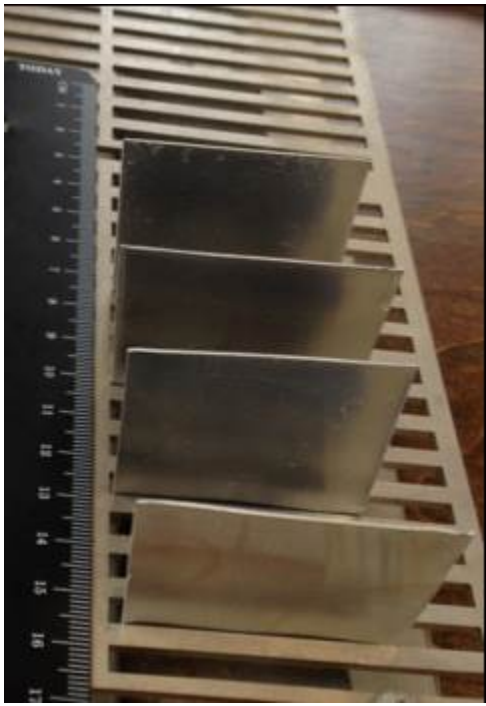


Thermal spray scanning velocity 5



Thermal Spray of Si powder on Al foil





Thermal Spray of Si powder on ceramic roof tile/Pyrogenesis

A ceramic roof tile, fully covered with Al/Si coatings

Thermal Spray of Si powder on natural stone and concrete

Si coating on natural stone

Si coating on concrete

Conclusions

- Recycled Si scrap can be used as a Si feedstock for Si PV (wafers/Si powder based layers)
- Refined Si kerf can be used for the growth of Si ingots
- Feasibility for wafering of Si kerf based ingots should be verified
- Si powder based ingots can be sintered from Si scrap based powders and can be wafered
- Feasibility to use sintered wafers for Si PV should be verified
- Thermal spray shows the potential for the in-situ low-temperature manufacturing of integrated c-Si layers on different substrates
- Low grade Si substrates can be used for the processing of Si wafer equivalents (at least via bonding of Si foils)

Thank you for your attention !