Design of CRC circuit for 5G system using VHDL

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ABSTRACT

In this document, we focus on how to design cyclic redundancy check (CRC) circuits with different 5G polynomial divisor using very high-speed integrated circuit (VHSIC) hardware description language (VHDL) to integrate in field-programmable gate array (FPGA) suitable kit using a suitable design code. The different between designed circuits came from the different of data size according to polynomials requirements conditions since there are huge data size in 5G system that required divide it with suitable method and then implemented the required circuit. CRC code as a polar code and short low density parity check (LDPC) is proposed in 5G new radio (NR) systems, CRC properties to divided data and CRC cod make it particularly very useful for codes with higher data rate and longer lengths, and for codes with low data rates and small length as an error detection method. The CRC encoder circuit (transmitter side) and CRC decoder circuit (receiver side) with different polynomial and data size have been designed using VHDL. Xilinx ISE 14.3 simulator, where the test bench simulation results give the expected simulator results of proposed decoding circuit scheme so to integrated using ZYNQ FPGA kit.

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1. INTRODUCTION

The A 5[rd] generation (5G) technology is one of most important wireless access technology, which is developed and improved by the 3rd generation partnership project (3GPP), 5G new radio (NR) is characterized many usage state to enhancing mobile broadband (eMBB), massive machine type communications (mMTC), critical machine type communication (cMTC), and ultra-reliable low latency communication (URLLC) [1]. 5G wireless technology is deliver high data rate with high speed, more reliability, more network capacity, higher performance, and connect a new industry [2]. 5G technology improved special types of internet of things (IoT) like internet of vehicles (IoV) is, since it provides suitable latency and higher mobility [3]. According to 5G new radio specification technology input data and control data stream are encoding and decoding through medium access control (MAC) layer to produce transport and control services to next processor stage [4].

5G NR consist of many physical channels explained in downlink channels and uplink channels, where downlink physical channels contain many channels like physical downlink shared channel (PDSCH), the physical broadcast channel (PBCH), physical downlink control channel (PDCCH), and the uplink physical channels consist of the physical uplink control channel (PUCCH) [5], [6]. Physical uplink shared channel (PUSCH), the physical random access channel (PRACH), and many other channels in downlink/ uplink channels. The mainly channels that used to transmitted data are PUSCH and the PDCCH. The enhanced mobile broadband eMBB required high transmission data rates channel coding scheme is depended on detection and correction of errors, interleaving rate, matching and control information mapping that splitting onto/physical channels [7], [8].

Cyclic redundancy check (CRC) code is a highly error detection method which is integrity mechanism used in 5G industrial use, CRC codes can be consider as a first line of defense against errors by detection data packets corruption between the transmitter and receiver in a communication link [9]-[11]. CRC code is used for error detection for many applications like digital communication, control system, data storage and data compression [12]. With a growth of 5G technology, a new technologies and attractive strategies have been appeared, which mean many challenges are appeared to error detection and correction strategies. Specifically, there are many applications involved in five generation technology like IoT applications; therefore, 5G required lightweight and robust error control algorithms to support these applications [13]. This paper is organized as follows. In section 1, introduction to 5G NR and CRC technique, section 2 we describe transport code and CRC polynomials that use in 5G. In section 3 we introduce proposed system result with different polynomials size. Finally, section 4 we conclude the paper results.

2. DESIGN METHOD

In this section, a brief description of the proposed CRC algorithm technique with different CRC polynomials code that suitable for 5G NR to detect error then corrected it using dynamic grant on PDCCH asynchronous hybrid-ARQ (HARQ) uplink and design it with VHDL to be integrated then using field-programmable gate array (FPGA) using kit like Xilinx evaluation kit ZYNQ-7000 ZC706+ADRV9371. The design circuits have been tested with different input data at the transmitter side and checked at the recived side to detected error with two cenario when data received is correct and when received data has an error. The CRC circuits in 5G NR required number of slices LUTs for each circuit with different polynomials are explained.

2.1. 5G and proposal system techniques

In 5G NR data has been organized in MAC layer at the transport block then transmits it to the physical layer, where the maximum size of transport block is 1,277,992. In transport layer instead of adding CRC bits at the end of data, CRC bits are distributed as segments with information bits. The segmentation of the transport block data and CRC code is explained in Figure 1 [6], [14].

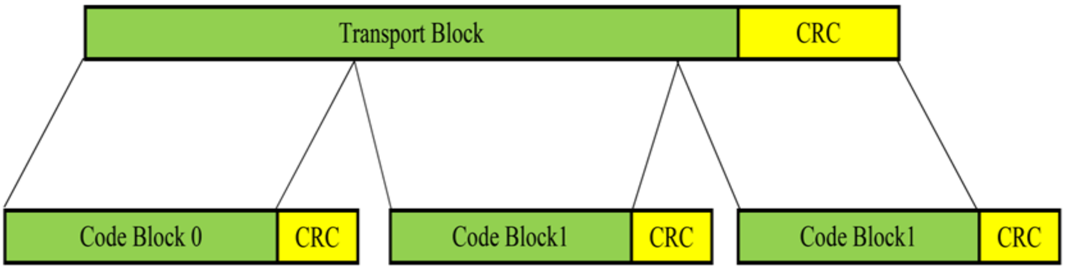


Figure 1. Transport block and code block

If transport data block size is more than 3,824, a (16-bit), then CRC is added as trailer to the transport block. Otherwise, a (24-bit) CRC is added to transport block. Then the transport block splits for many code blocks which are equal size when the transport block data size is exceed a threshold. The maximum code block size number in 5G NR is 8448. at the same time 24-bit CRC is redundant at each code block at segmentation processing, as consequence of the difference size of transport data block size and code block size make the CRC technique scheme is suitable to detected error in transport and code blocks. Let the input data bits computed by a_0, a_1, a_2,..., a_{A-1}, while parity bits as p_0, p_1, p_2,…, p_{L-1}, where A is the input sequence size and L is parity bit number. The parity bits are generated by one of the following cyclic generator polynomials which explained in explain in Table 1, while the CRC encoding is obtained in the following systematic form:

$$a0XA + L - 1 + a1XA + L - 2 + \cdots + aA - 1XL + p0XL - 1 + p1XL - 2 + \ldots + pL - 2X1 + pL - 1 \quad (1)$$

If the remainder of division data corresponding to CRC polynomial equal to zero then the data will pass to the next processing (data is correct), else data has a corrupted bit. Then the generated CRC bits (the remainder) are attachment by b_0, b_1, b_2,…, b_{B-1}, where:

$$B = A + L \quad (2)$$

In this paper six CRC polynomial codes are proposed to design in VHDL to different data size. These CRC polynomials codes are explained in Table 1 [15], [16]. Then, CRC code can be implemented by direct calculation which required linear feedback shift register (LFSR) and XOR-ing operations for each bit that give CRC to detect single and burst error, which make it suitable for any systems using Turbo code [17], [18]. Due to, this scheme is mainly used in many actual systems. So, CRC code is help to decided which the data was corrected or corrupted, then we can be implemented CRC circuit by as a serial processing or parallel processing [19].

For 5G NR the PDCCH for downlink channel data is scheduling, for down link control information (DCI), radio resource, timing information of the hybrid ARQ-acknowledgement (HARQ-ACK) feedback which is depended on CRC output data, the construction of transport block coding segmentation and CRC polar codes can be reduce the computational complexity of system and the required memory space [20], [21]. VHDL is a high-level computer language, which is used to design and described hard-ware structure of the circuit. There are many reasons to use VHDL, if you need to design any circuit you need (schematic of circuit or truth table or sum of product function or product of sum function) this method is suitable for small or medium circuit but for huge circuit like microprocessor or any communication system that will be hardly for that VHDL is provide as with simple and cheap method to design circuit, with property of redesign and modify of circuit companied with FPGA so VHDL is help to development the electronic design automation (EDA) tools to improving your design to more advanced without having to re-enter your circuit descriptions, and gives ability to implemented circuit into (ASICs, FPGAs, and complex PLDs) [22], [23].

Table 1. 5G polynomials with suitable CRC

CRC	Polynomial
CRC6	x^6+x^5+1
CRC11	$x^{11}+x^{10}+x^9+x^5+1$
CRC16	$x^{16}+x^{12}+x^5+1$
CRC24A	$x^{24}+x^{23}+x^{18}+x^{17}+x^{14}+x^{11}+x^{10}+x^7+x^6+x^5+x^4+x^3+x+1$
CRC24B	$x^{24}+x^{23}+x^6+x^5+x+1$
CRC24C	$x^{24}+x^{23}+x^{21}+x^{20}+x^{17}+x^{15}+x^{13}+x^{12}+x^8+x^4+x^2+x+1$

3. RESULTS AND DISCUSSION

In this paper the CRC transmitted circuit and CRC received circuit are designed with 6 CRC divisor with different data size and with two states error and corrected data using VHDL. The designed system with FPGA has been given many efficient properties, make it very confirm to building up constituents of 5G system. The FPGA kit is offer a less energy consumption for cellular system, good performance for channel coding such as turbo codes/low density parity check (LDPC) codes, flexibility in modifications, and implementation complex system with performance trade-off [24]-[27].

3.1. CRC6

For 5G NR the in the uplink control channel should be done using CRC6 to error detection when the transport block size A have a value 12≤A≤19 [8], so the CRC encoder and decoder circuit was design using VHDL, with random input data (16 bits). CRC6 transmitter circuit block explain in Figure 2, with input data bit (16 bits) and output data bits (23 bits). The CRC encoder circuit required 49 slice LUTs. On the other side CRC decoder circuit is received data and checking it, if it is correct (retrans=(00)HEX), else data has been corrupted, the CRC received circuit block is shown in Figure 3, which consist of 177 slice LUTs.

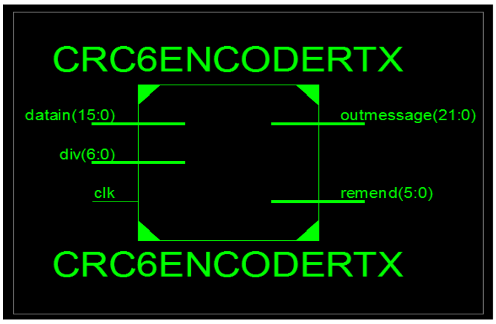


Figure 2. CRC6 transmitter circuit

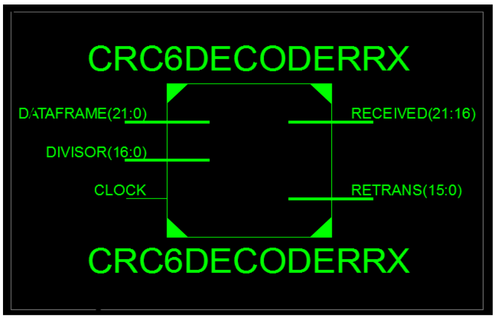


Figure 3. CRC6 receiver circuit

3.2. CRC11

CRC11 suitable for the downlink control channel when the transport block size is 20≤A≤1706. The transmitter circuit block diagram of CRC11 with random input data bits (1024 bits) and divisor with 12 bits where output data consist of 1035 bits and remainder signal which represented the redundancy data bits added to original data, CRC11 encoder circuit consist 6139 slice LUTs, and CRC11 decoder circuit contain 6205 slice LUTs CRC11 encoder and decoder circuit is explain in Figures 4 and 5.

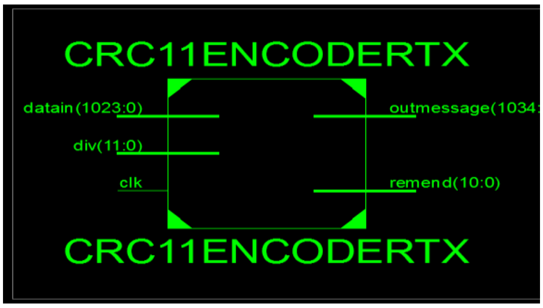


Figure 4. CRC11 transmitter circuit

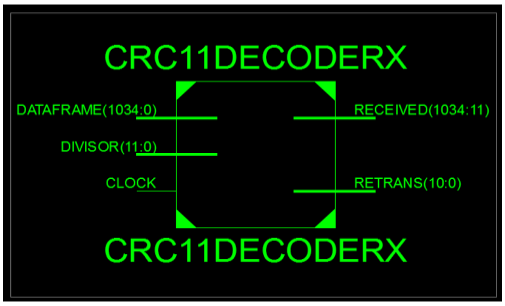


Figure 5. CRC11 receiver circuit

3.3. CRC16

CRC16 is used when the transport block size A for uplink shared channel and downlink shared channels is 1≤A≤3824, the random input data that selected is (3824 bits) to transmitted it after implemented CRC algorithm on it, CRC encoder and decoder circuit pins is explained in Figures 6 and 7, while CRC encoder circuit contain 30728 slice LUTs and CRC 16 decoder have 30856 slice LUTs.

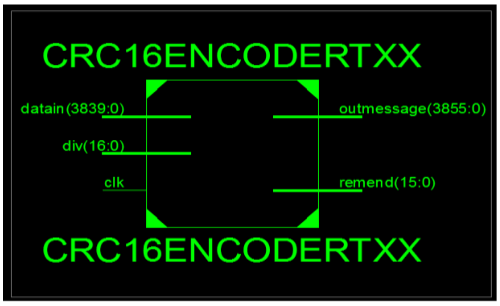


Figure 6. CRC16 transmitter circuit

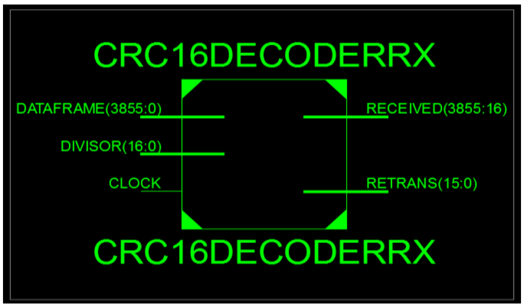


Figure 7. CRC16 receiver circuit

3.4. CRC24A

When transport block size between 3824≤A≤8424, CRC24A is proposed. We supposed a random data bit with size (3984 bits) that will be processed at CRC transmitter circuit is explained in Figure 8, that consist of 48,300 slice LUTs. Where CRC24A receiver circuit is explained Figure 9, and it have 48588 slice LUTs.

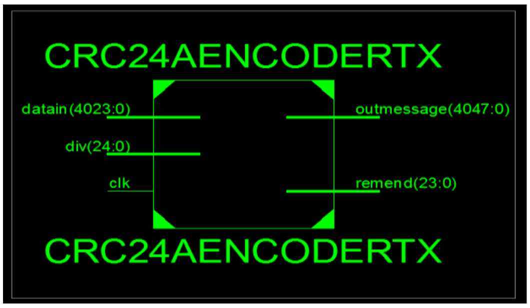


Figure 8. CRC24A transmitter circuit

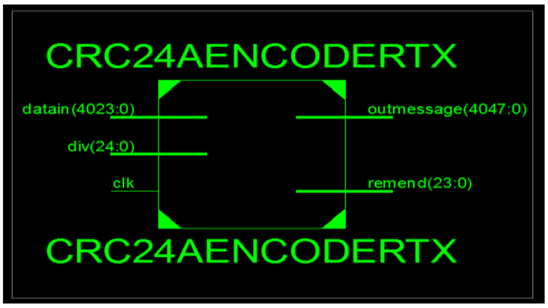


Figure 9. CRC24A receiver circuit

3.5. CRC24B

For the uplink shared channels and downlink shared channels, the CRC24B is suggested combining with LDPC with block sizes A≤8424. In this CRC code the random input data is (3,984 bits) after treatment with CRC code, as shown in Figure 10, which is need 48,300 slices LUTs on the other hand the received data circuit need 48,108 slices LUTs, and block received is explain in Figure 11.

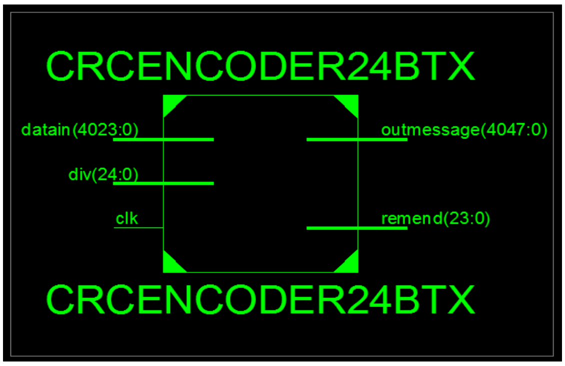


Figure 10. CRC24B transmitter circuit

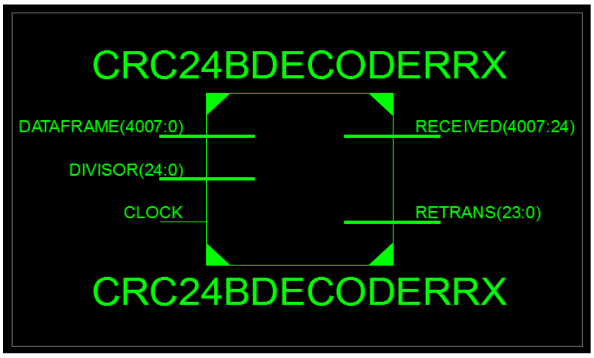


Figure 11. CRC24B receiver circuit

3.6. CRC24C

At the 5G downlink broadcast channel, if A is less or equal to 8,424 CRC24C is proposed, the input data size (3,984) which have been encoding in CRC24C at the transmitter side that obtained in Figure 12, which is required 48,300 slices LUTs. The decoder circuit at the receiver side is explain in Figure 13 which required 48,108 LUTs slice. The divisor value, input of encoder data bits, output of CRC encoder circuit data bits, input data of CRC decoder circuit which use the same divisor of CRC encoder, and output state is explained in Table 2.

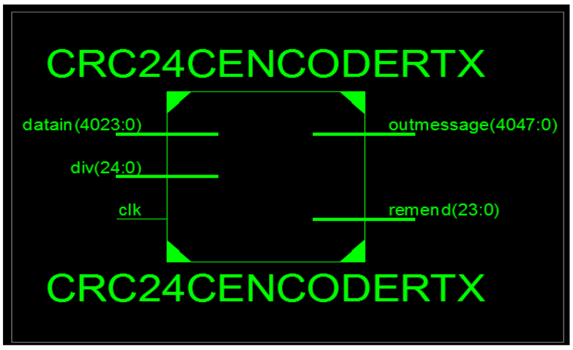


Figure 12. CRC24C transmitter circuit

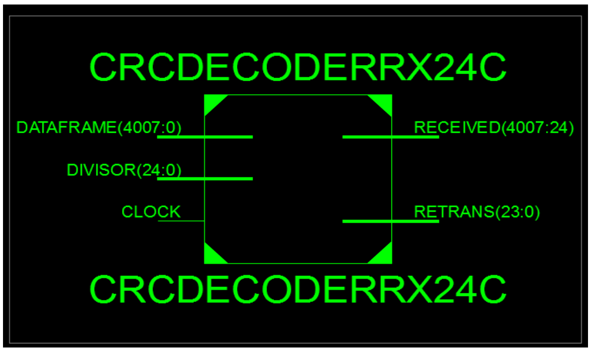


Figure 13. CRC24C receiver circuit

The output wave form that explained in Table 2 for CRC encoder and decoder circuits is shown in figures that explained below. At CRC6 the input data (FFFE)HEX is coded to (7FFF4C)HEX and transmitted through transmission medium as in Figure 14(a), at the receiver side the circuit have two state: the data has been received corrected (7FFF4C)HEX where (retrains=00) so CRC receiver circuit remove the redundancy bits and upload data to next process as in Figure 14(b), or data has been corrupted then CRC6 detected error and generated any other signal except (retrains=00) signal so receiver corrected error data as shown in Figure 14(c). This process is similar for all other CRC transmitter and receiver circuits waveform, which CRC11 is explained in Figures 15(a) and (b), CRC16 output wave form is obtained in Figures 16(a)-(c), CRC24A encoder and decoder output wave form is shown in Figures 17(a)-(c), CRC24B output wave form shown in Figures 18(a)-(c), and CRC24C encoder and decoder circuit is shown in Figures 19(a)-(c).

Table 2. CRC output waveform resulst for different CRC divisor and data

CRC type	Divisor for CRC encoder and decoder	Input data to CRC encoder	Output data to CRC encoder (transmitter circuit)	Input data to CRC decoder (received circuit)	Output error signal (RETRANS)	Received data state
CRC6	(61)$_{HEX}$	(FFFE)$_{HEX}$	(7FFF4C)$_{HEX}$	(7FFF4C)$_{HEX}$	(00)$_{HEX}$	Correct
				(7FFF0C)$_{HEX}$	(0D)$_{HEX}$	Corrupted
CRC11	(701)$_{HEX}$	(FFFFFFFFFF8000….FFFFFFFFFF)$_{HEX}$	(7FFFFFFFFFC0000……FFFFFFF7E1)$_{HEX}$	(7FFFFFFFFFC0000………FFFFFFF7E1)$_{HEX}$	(000)$_{HEX}$	Correct
				(557FFFFFFFC0000…………FFFFFFF7E1)$_{HEX}$	(155)$_{HEX}$	Corrupted
CRC16	(11021)$_{HEX}$	(FFFFFF000000….000000FFFFFF)$_{HEX}$	(FFFFFF0000……….00000FFFFFFDA68)$_{HEX}$	(FFFFFF0000000….000FFFFFFFDA68)$_{HEX}$	(0000)$_{HEX}$	Correct
				(FFF0000000…….000000FFFFFFDA68)$_{HEX}$	(AFAF)$_{HEX}$	Corrupted
CRC24 A	(1864CFB)$_{HEX}$	(FFFF000000000…………FFFF)$_{HEX}$	(FFFF000000000……………FFFFC57182)$_{HEX}$	(FFFF000000000……………FFFFC57182)$_{HEX}$	(000000)$_{HEX}$	Correct
				(0FFF000000000……………FFFFC57182)$_{HEX}$	(549F70)$_{HEX}$	Corrupted
CRC24 B	(1800063)$_{HEX}$	(FFFFFF0000000……FFFFFF)$_{HEX}$	(FFFFFF0000000……FFFFFFE85600)$_{HEX}$	(FFFFFF0000000………FFFFFF E85600)$_{HEX}$	(000000)$_{HEX}$	Correct
				(AEAFFF0000000………FFFFFFE85600)$_{HEX}$	(B7E60A)$_{HEX}$	Corrupted
CRC24 C	(1B2B117)$_{HEX}$	(AAAAAAAAAC00……FFFFFF)$_{HEX}$	(AAAAAAAAAC00…………FFFFFFDB8344)$_{HEX}$	(AAAAAAAAAC000……FFFFFFDB8344)$_{HEX}$	(000000)$_{HEX}$	Correct
				(AAAAAAAAAC000……FFFABFDB8344)$_{HEX}$	(83C318)$_{HEX}$	Corrupted

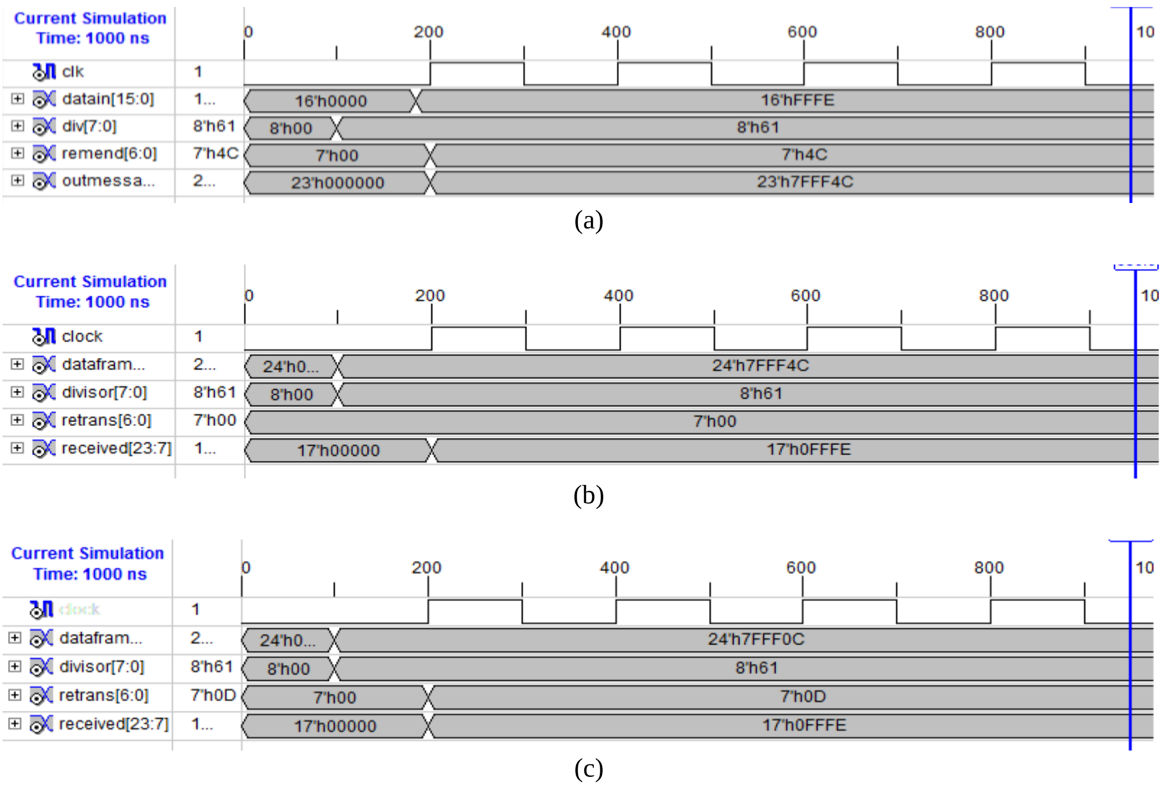
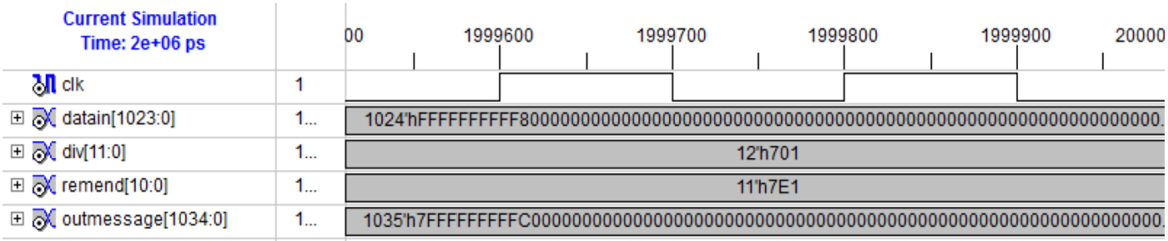
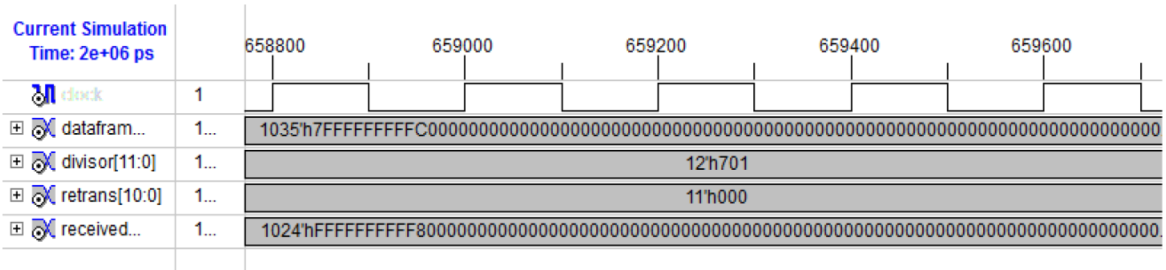


Figure 14. CRC6 (a) transmitter circuit waveform, (b) receiver circuit waveform (corrected data), and (c) receiver circuit waveform (corrupted data)

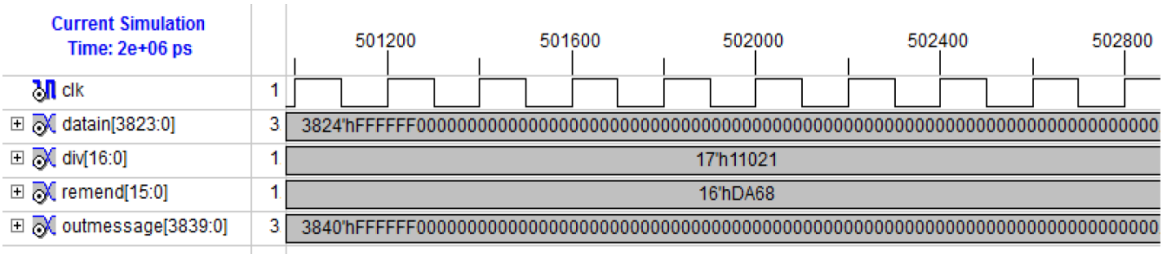


(a)

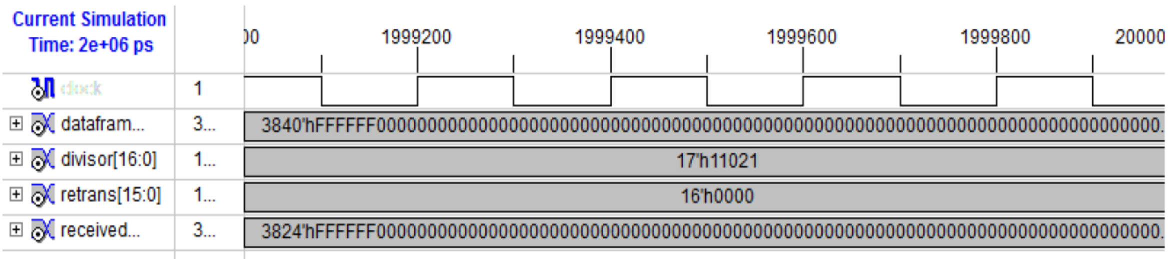


(b)

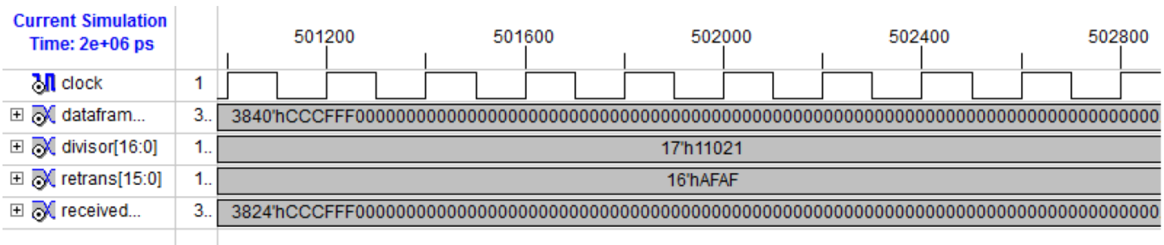
Figure 15. CRC11 (a) transmitter circuit waveform and (b) receiver circuit waveform (corrected data)



(a)

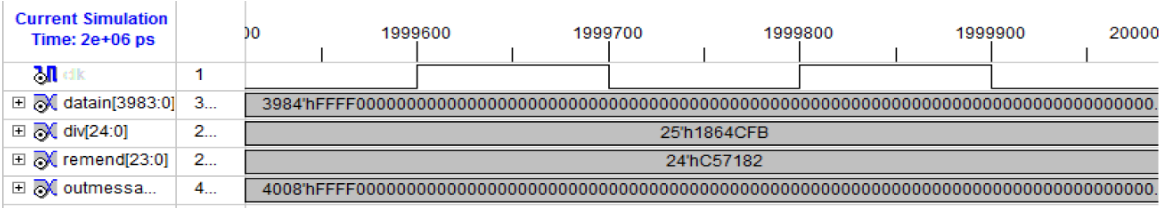


(b)

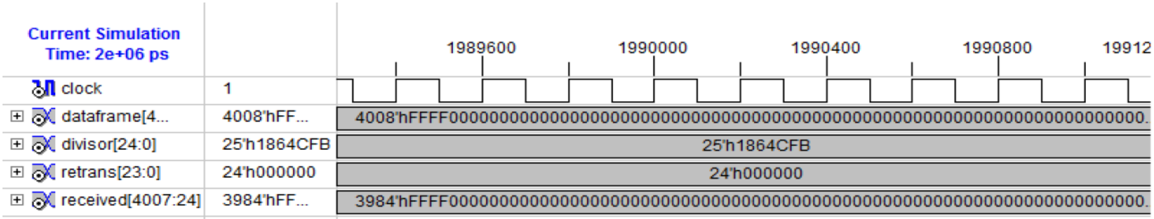


(c)

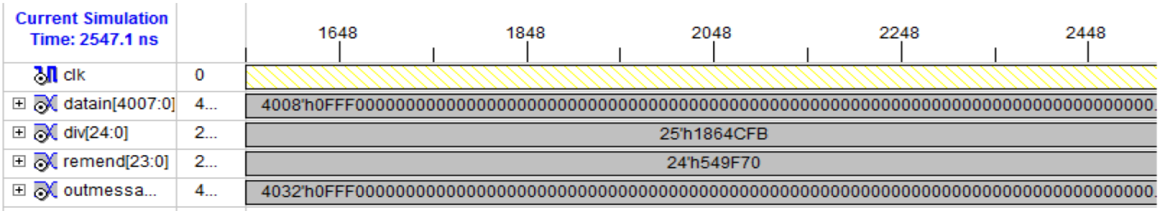
Figure 16. CRC16 (a) transmitter circuit waveform, (b) receiver circuit waveform (corrected data), and (c) receiver circuit waveform (corrupted data)



(a)

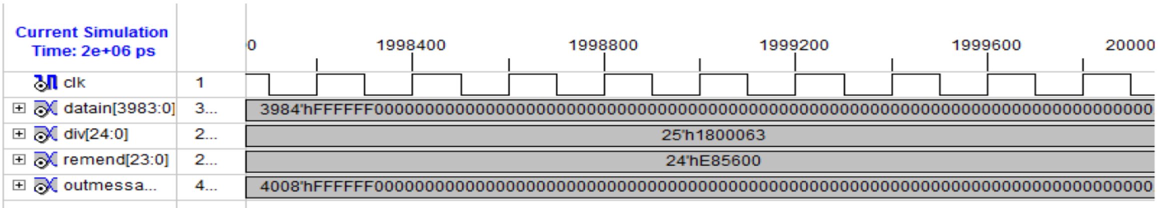


(b)

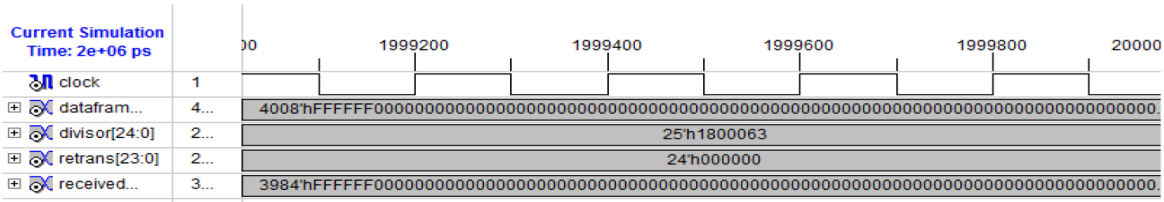


(c)

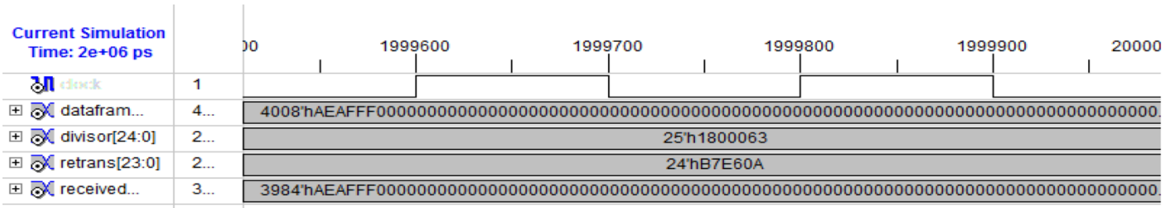
Figure 17. CRC 24A (a) transmitter circuit waveform, (b) receiver circuit waveform (corrected data), and (c) receiver circuit waveform (corrupted data)



(a)

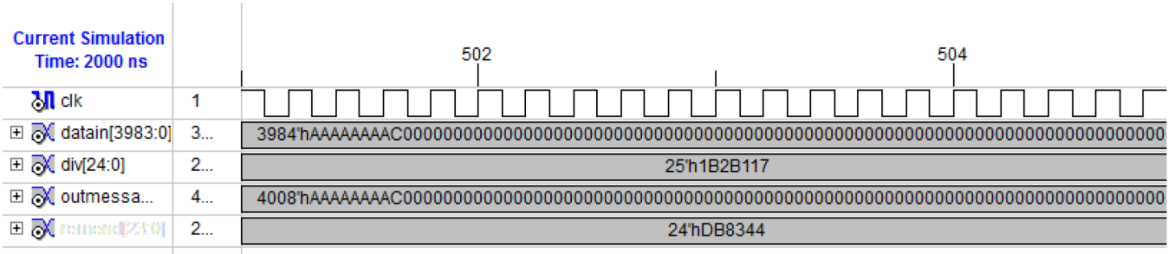


(b)

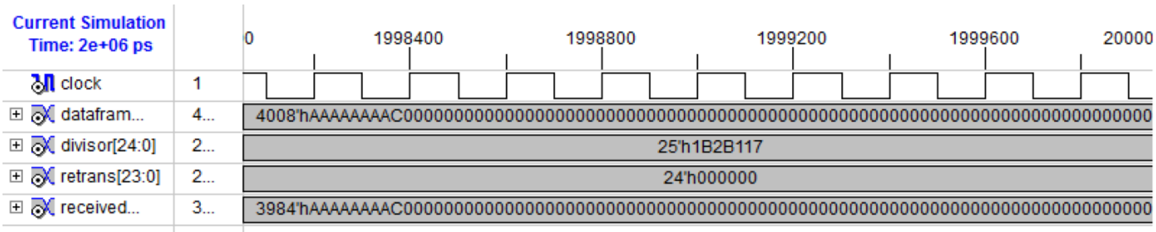


(c)

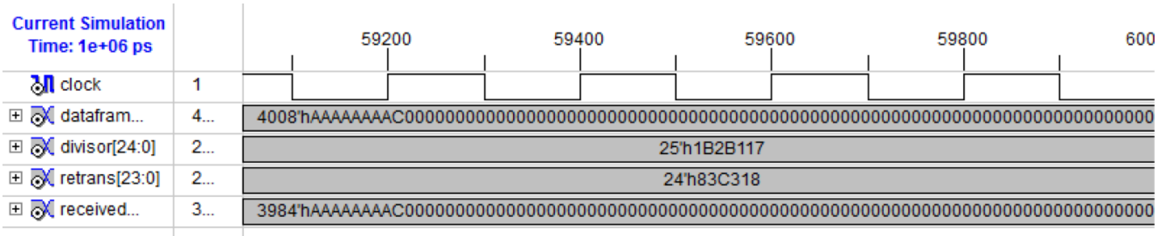
Figure 18. CRC 24B (a) transmitter circuit waveform, (b) receiver circuit waveform (corrected data), and (c) receiver circuit waveform (corrupted data)



(a)



(b)



(c)

Figure 19. CRC24C (a) transmitter circuit waveform, (b) receiver circuit waveform (corrected data), and (c) receiver circuit waveform (corrupted data)

4. CONCLUSION

CRC circuits with different generated polynomial (CRC6, CRC11, CRC16, CRC24A, CRC24B, CRC24B, and CRC24C) which is used in 5G NR are designed and implemented as an encoder and decoder circuits using VHDL successfully. The receiver output is referring to the data are correct or it has single or burst error through the output pin (retrans), if data correct (retrans=0) else data was ignored and need to be corrected; the output wave form results are match with expected output data. The proposed CRC circuits with different polynomials can be design and implemented using VHDL and FPGA kit and can be benefit of CRC properties and CRC implemented in serial and parallel form, that make this system suitable to be integrated.

REFERENCES

[1] Z. Lin, J. Li, Y. Zheng, N. V. Irukulapati, H. Wang, and H. Sahlin, "SS/PBCH Block Design in 5G New Radio (NR)," in *2018 IEEE Globecom Workshops (GC Wkshps)*, Dec. 2018, doi: 10.1109/glocomw.2018.8644466.

[2] L. Y. Hosni, A. Y. Farid, A. A. Elsaadany, and M. A. Safwat, "5G New Radio Prototype Implementation Based on SDR," *Commun. Netw.*, vol. 12, no. 01, pp. 1–27, 2020, doi: 10.4236/cn.2020.121001.

[3] K.-Y. Lam, X. Yi, and H. Wang, "Security and Privacy Protection for 5G-Enabled Internet of Things," *Hindawi*, Dec. 2021.

[4] T. Baicheva, P. Kazakov, and M. Dimitrov, "Some comments about CRC selection for the 5G NR specification." *arXiv*, Apr. 06, 2021, doi: 10.48550/arXiv.2104.02639.

[5] H. Saarnisaari, J.-M. Houssin, and T. Deleu, "5G New Radio Over Satellite Links: Synchronization Block Processing," in *2019 European Conference on Networks and Communications (EuCNC)*, Jun. 2019, doi: 10.1109/eucnc.2019.8802055.

[6] J. H. Bae, A. Abotabl, H.-P. Lin, K.-B. Song, and J. Lee, "An overview of channel coding for 5G NR cellular communications," *APSIPA Trans. Signal Inf. Process.*, vol. 8, no. 1, 2019, doi: 10.1017/atsip.2019.10.

[7] H. Ji, S. Park, J. Yeo, Y. Kim, J. Lee, and B. Shim, "Ultra-Reliable and Low-Latency Communications in 5G Downlink: Physical Layer Aspects," *IEEE Wirel. Commun.*, vol. 25, no. 3, pp. 124–130, Jun. 2018, doi: 10.1109/mwc.2018.1700294.

[8] A. S. Khirbeet and R. C. Muniyandi, "New Heuristic Model for Optimal CRC Polynomial," *International Journal of Electrical and Computer Engineering (IJECE)*, vol. 7, no. 1, pp. 521-525, Feb. 2017, doi: 10.11591/ijece.v7i1.pp521-525.

[9] A. H. Saleh, K. M. Saleh, and S. Al-Azawi, "Design and simulation of CRC encoder and decoder using VHDL," in *2018 1st International Scientific Conference of Engineering Sciences-3rd Scientific Conference of Engineering Science (ISCES)*, Jan. 2018, doi: 10.1109/isces.2018.8340557.

[10] A. H. Saleh, O. A. Imran, W. T. Ali, A. Taha, and W. Abed, "A novel hybrid error detection and correction method using VHDL," *Int. J. Eng. Technol.*, vol. 7, pp. 3048–3053, Jan. 2018, doi: 10.14419/ijet.v7i4.15685.
[11] R. Mahajan, K. Devi, and D. Bagai, "Area efficient parallel lfsr for cyclic redundancy check," *International Journal of Electrical and Computer Engineering (IJECE)*, vol. 10, no. 2, pp. 1755-1763, Apr. 2020, doi: 10.11591/ijece.v10i2.pp1755-1763.
[12] P. Visconti, R. Velazquez, S. Capoccia, and R. D. Fazio, "High-performance AES-128 algorithm implementation by FPGA-based SoC for 5G communications," *International Journal of Electrical and Computer Engineering (IJECE)*, vol. 11, no. 5, p. 4221, Oct. 2021, doi: 10.11591/ijece.v11i5.pp4221-4232.
[13] H. Wu, "A Brief Overview of CRC Implementation for 5G NR," in *Moving Broadband Mobile Communications Forward-Intelligent Technologies for 5G and Beyond*, IntechOpen, 2021, doi: 10.5772/intechopen.91790.
[14] T. Baicheva and P. Kazakov, "CRC selection for decoding of CRC-polar concatenated codes," in *Proceedings of the 9th Balkan Conference on Informatics*, Sep. 2019, doi: 10.1145/3351556.3351573.
[15] S. A. Hashemi, C. Condo, F. Ercan, and W. J. Gross, "On the performance of polar codes for 5G eMBB control channel," in *2017 51st Asilomar Conference on Signals, Systems, and Computers*, Oct. 2017, doi: 10.1109/acssc.2017.8335664.
[16] H. Wu, T. Liu, J. Xu, and F. Wang, "Parallel CRC architecture for broadband communication systems," *Electron. Lett.*, vol. 53, no. 21, pp. 1439–1441, Oct. 2017, doi: 10.1049/el.2017.1029.
[17] H. Zhou, C. Zhang, W. Song, S. Xu, and X. You, "Segmented CRC-Aided SC List Polar Decoding," in *2016 IEEE 83rd Vehicular Technology Conference (VTC Spring)*, May 2016, doi: 10.1109/vtcspring.2016.7504469.
[18] E. Dubrova, M. Naslund, and G. Selander, "CRC-Based Message Authentication for 5G Mobile Technology," in *2015 IEEE Trustcom/BigDataSE/ISPA*, Aug. 2015, doi: 10.1109/trustcom.2015.503.
[19] Y. Haifen, Y. Suxin, Z. Hao, R. Yan, H. Xiangdong, and L. Shuisheng, "A simplified decoding algorithm for multi-CRC polar codes," *J. Syst. Eng. Electron.*, vol. 31, no. 1, pp. 12–18, Feb. 2020, doi: 10.21629/JSEE.2020.01.02.
[20] B. G. Kumar, B. S. Kariyappa, and A. Gupta, "Integration and Verification of Physical Layer Modules for 5G Technology," in *2019 3rd International conference on Electronics, Communication and Aerospace Technology (ICECA)*, Jun. 2019, doi: 10.1109/iceca.2019.8822003.
[21] B. Bertenyi *et al.*, "5G NR Radio Interface," *J. ICT Stand.*, vol. 6, no. 1, pp. 31–58, 2018, doi: 10.13052/jicts2245-800x.613.
[22] S. D. Hasan, "Hardware implementation of hybrid intelligent systems based on FPGA," Doctoral dissertations Theses and Dissertations Master, University of Technology, Iraq, 2010. Accessed: Nov. 27, 2022. [Online]. Available: https://search.emarefa.net/en/detail/BIM-305034-hardware-implementation-of-hybrid-intelligent-systems-based-
[23] V. A. Pedroni, *Circuit Design with VHDL*. Cambridge, Mass: The MIT Press, 2004.
[24] V. Chamola, S. Patra, N. Kumar, and M. Guizani, "FPGA for 5G: Re-configurable Hardware for Next Generation Communication," *IEEE Wirel. Commun.*, vol. 27, no. 3, pp. 140–147, Jun. 2020, doi: 10.1109/mwc.001.1900359.
[25] J. C. Borromeo, K. Kondepu, N. Andriolli, and L. Valcarenghi, "FPGA-accelerated SmartNIC for supporting 5G virtualized Radio Access Network," *Comput. Netw.*, vol. 210, p. 108931, Jun. 2022, doi: 10.1016/j.comnet.2022.108931.
[26] S. Mhaske, H. Kee, T. Ly, A. Aziz, and P. Spasojevic, "FPGA-Based Channel Coding Architectures for 5G Wireless Using High-Level Synthesis," *Int. J. Reconfigurable Comput.*, vol. 2017, pp. 1–23, 2017, doi: 10.1155/2017/3689308.
[27] F. Kaltenberger, H. Wang, and S. Velumani, "Performance evaluation of offloading LDPC decoding to an FPGA in 5G baseband processing," in *WSA 2021; 25th International ITG Workshop on Smart Antennas*, Nov. 2021, pp. 1–4.

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