Deliverable 3.4: Report on fabricated MMICs and frontend performance

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Abstract

This deliverable summarizes the research on D-band fabricated RFICs and their measurement results used in ARIADNE, as an output in the second project phase of work in Task 3.2. Packaging of the radio frequency signal generation chain in combination with mandatory circuitry is also described in here, to finally build transmitter- and receiver-modules to be used for the planned project demonstrators of work package 5.

Deliverable 3.4 focuses on research activities regarding RFIC design, realization and performance measurements, which will cover all circuit design activities for the frontend modules. The project envisioned a multi-band radio that covers the major frequency sub-bands from 141 to 200 GHz (e.g. 141-148.5 GHz, 151.5-164 GHz, 167-174.8 GHz, 191.8-200 GHz).

The presented frontend RFICs were implemented in a high-speed 50 nm and 35 nm InGaAs HEMT technology on GaAs substrates fabricated in the IAF clean room facility. High-tech cost-efficient RF packaging is used to enclose the RFICs while maintaining their superior performance.

Coordinator of this deliverable is IAF. The technical quality is assured by the technical management UPRC Prof. Angeliki Alexiou and the WP / Task Leader IAF.

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Executive summary

The deliverable “D3.4 – Report on fabricated MMICs and frontend performance” presents the manufactured RFIC transceiver designs in combination with their respective on-wafer characterization results as well as their in-package performance accomplished in the second half of the ARIADNE project. The fabricated RF frontend modules are being used for the experimental investigations of dual-polarized transmission at high spectral efficiency and the cross-polarization interference cancellation with the developed algorithms and baseband hardware of partner ICOM (demonstrator 1). Also, the non-line-of-sight demonstrator based on reconfigurable intelligent surfaces (demonstrator 2) realized in work package 5 is run with presented modules.

The report summarizes state-of-the-art at D-band RFIC designs and measurements and introduces appropriate packaging methods and comparison of their on-wafer versus in-package performance. The work comprises research conducted as part of Task 3.2 though the overall radio concepts of interest in ARIADNE as well as the contributions and ideas of partners in other WP3 tasks, i.e. baseband, antenna and RIS design, also determined the course of the RFIC outcomes.

The main topics and highlights of this report are:

- System topology for high spectral efficiency communications links
- Summary of D-band radio frontend MMICs as well as their measurement results
- Summary of packaging process of presented MMICs in combination with overall in-package performance evaluations

List of authors

Organization/Company	Author	Contribution
IAF	Benjamin Baumann	Public summary of RFIC & frontend module performance report
IAF	Christian Zech	Document review
IAF	Sébastien Chartier	Document review
UPRC	Angeliki Alexiou	Final editing / review
EUR	Halid Hrasnica	Final review

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Abbreviations

Abbreviation	Description
CG	Conversion Gain
CS	Common-Source
FET	Field-Effect Transistor
GCPW	Grounded Coplanar Waveguide
HEMT	High Electron Mobility Transistor
HPA	High power amplifier
I/O	Input / output or Input / output pads of an IC
I/Q	In-phase/Quadrature
IC	Integrated Circuit
IF	Intermediate Frequency
InAlAs	Indium Aluminum Arsenide
InGaAs	Indium Gallium Arsenide
LNA	Low-Noise Amplifier
LO	Local oscillator
LoS	Line of Sight
LSB	Lower Sideband
MBE	Molecular Beam Epitaxy
MIM	Metal-Insulator-Metal
MMIC	Monolithic Millimeter-wave Integrated Circuit
MS	Microstrip
NF	Noise Figure
NiCr	Nickel Chromium
OP1dB	(Linear) P1dB Output Power
PA	Power amplifier
PCB	Printed Circuit Board
PDM	Polarization division multiplexing
PLL	Phase-Locked Loop
QAM	Quadrature amplitude modulation
RF	Radio Frequency
RFIC	Radio Frequency Transceiver Integrated Circuit
RIS	Reconfigurable Intelligent Surface
RX	Receiver
TX	Transmitter
USB	Upper Sideband
WP	Work Package
XPIC	Cross-polarization interference cancellation

1 Introduction

This deliverable report of the research work of WP3 (designs and prototypes), focusing on radio frontend monolithic microwave integrated circuit design, performance evaluation, and packaging, is hereby presented. This is a continuation of work defined by D3.2 “Report on simulations of first RFIC implementations”, closing the loop and completing the radio frequency frontend part. The description of the developed state-of-the-art D-band radio frequency (RF) transceiver integrated circuits (RFICs), their on-wafer and in-package performance and design methods as well as packaging measures to maximize their possible performance are given here.

This document is structured to provide a comprehensive overview of the work, starting with a detailed description of the RFIC design process. Key design considerations, such as noise figure, power gain, linearity, and frequency response, will be outlined, and how these parameters were optimized to meet targeted specifications of high spectral efficiency communication links will be discussed. The design methodology incorporated advanced techniques, including layout optimization, electromagnetic simulation, and optimization algorithms, to achieve the desired performance metrics. Furthermore, the performance evaluation section will delve into a thorough analysis of the designed RFICs. The various performance metrics, such as gain, noise figure, linearity, and power consumption, will be discussed, and detailed measurement results will be provided. The rigorous evaluation process ensures that the manufactured RF frontend modules meet stringent requirements since they are to be used in the D-band demonstrator systems of work package (WP) 5. Lastly, the crucial aspect of RF packaging will be explored, which plays a vital role in the overall performance and reliability of the RFICs. The packaging technique employed will be discussed, emphasizing considerations such as thermal management, electrical parasitics, and mechanical stability. Furthermore, insights into the selection of appropriate packaging methods to ensure optimal electrical performance of the RFICs will be provided and the performance of the packaged signal chains is evaluated.

Confidence is held that this deliverable will provide a comprehensive understanding of the design process, performance evaluation methodologies, and packaging strategies used in ARIADNE task 3.2. For an overall introduction to the project concepts and focus in WP3, the reader is referred to D3.1, D3.2 and D3.3.

2 System topology for ARIADNE communication links

Regarding the overall system design, as written in deliverable D3.2, there is the need for a transmitter (TX) and receiver (RX) front-end architecture and a respective chipset that need two synchronous channels to enable the targeted dual-polarization transmission for doubled data-rates in ARIADNE, which as well share the uplink and downlink frequency band as shown in Figure 1. Per transmission / reception block, a common local oscillator (LO) signal source is used, which generates baseband signals to be multiplied (Xn) into the targeted frequency band for the application, using monolithic millimeter-wave integrated circuits (MMICs). This signal is split to drive both TX / RX building blocks per polarization. A method of polarization division multiplexing (PDM) is introduced to split the signal in a linearly polarized vertical and a linearly polarized horizontal polarization, Pol-V and Pol-H, respectively, to transmit data via 90 ° In-phase (I) and quadrature (Q) up-/down-conversion mixing.

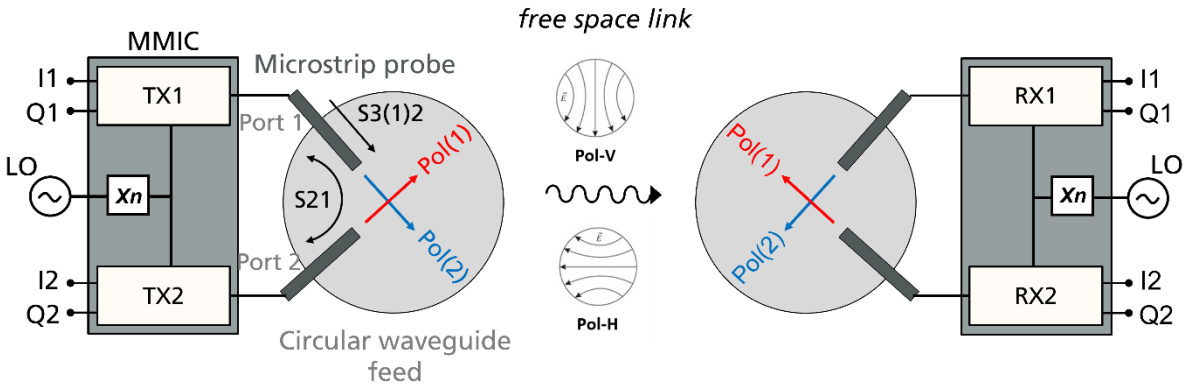


Figure 1: System topology for dual-polarization transmission / reception in ARIADNE.

For both polarizations of the transmission / reception, the same frequencies are used due to the synchronous nature of the LO distribution. This makes a good cross polarization suppression inevitable for being able to generate radio frequency (RF) links with targeted highest order modulation rates.

3 High-performance D-band radio frontend MMICs

3.1 MMIC fabrication details and chosen technology

As discussed in the previous deliverable regarding MMIC and RF-frontend development D3.2, there should have been two different approaches for the realization of the RF integrated circuits (RFICs). Despite the information given in deliverable D3.2, the RFICs finally were implemented using 35 nm and 50 nm InGaAs (Indium Gallium Arsenide) HEMT (High Electron Mobility Transistor) technology of the clean room facilities at Fraunhofer IAF. During the second phase of the project, it was tried to extend this procedure by a transfer process onto silicon substrates by completely remove the GaAs wafer substrate, to eliminate most of the hazardous III-V materials from the final product. Though, due to personal shortage as well as sick leave introduced by the pandemic, it was never possible to manufacture a working chipset based on the hybrid silicon wafer substrate process.

Hence, the subsequent evolution of the ARIADNE chipset has been realized by making use of IAF's classical high-performance and world class InGaAs (metamorphic) HEMT technology. Multiple compact sized MMICs for TX- & RX-signal chains have been developed and manufactured which allow further integration towards single chip solutions to ease the package integration point of view in future endeavors.

As shown in Figure 2, the TX MMIC chain per polarization is realized by a frequency multiplier-by-four (X04013MB076) fed with an external input signal at around 20 GHz creating an output signal at around 80 GHz, a subharmonic mixer (MSH011MB165) with a multiplication factor of two, which is fed with I/Q input data at the intermediate frequency (IF) port, generating D-band signals around 160 GHz, as well as a power amplifier (PA) (AMP015MF_D) to boost the signal to an appropriate level due to link-budget considerations. The generated D-band signal is finally fed to a passive polarization multiplexer structure which will be included in a waveguide-based metal housing of the MMICs, as well as the antenna structure to emit the signal accordingly.

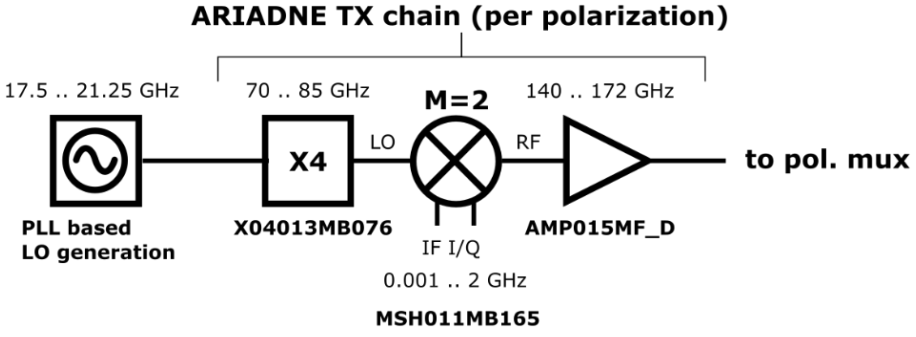


Figure 2: ARIADNE TX MMIC chain, fed by an external PLL-stabilized LO signal and I/Q data signals.

For the reception path (per polarization), the MMIC chain is depicted in Figure 3. A received D-band signal coming from the PDM device is amplified by a low-noise amplifier (LNA) (ALN002MD160), before it hits the RF port of a subharmonic mixer, now acting as a down

converter. Over-the-air transmitted I/Q data can subsequently be obtained at the IF port of the receiving mixer. The multiplier-by-four as well as the subharmonic mixer are the same in this MMIC arrangement like it was in the case of the TX chain.

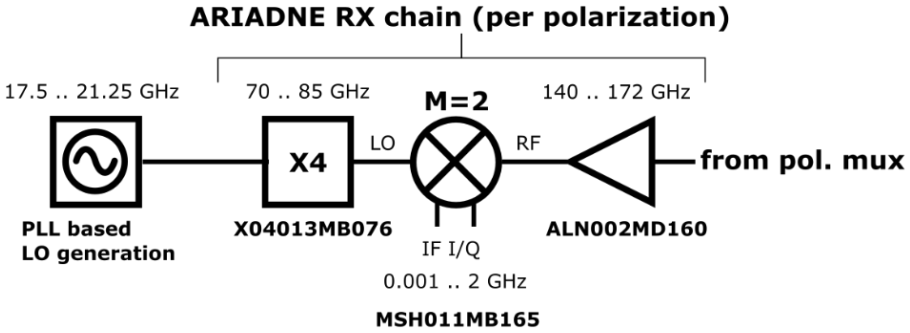


Figure 3: ARIADNE RX MMIC chain, fed by an external PLL-stabilized LO signal.

To establish a stable communication link, the LO signal of the RX unit is set to the exact same frequency around 20 GHz as for the TX unit. In both cases, an (external) phase-locked-loop (PLL) compares a highly stable signal of a temperature compensated crystal reference oscillator with the signal of a commercially available voltage-controlled oscillator to largely improve its spectral purity and phase noise.

3.1.1 Fraunhofer IAF 50 nm technology

Some of the presented MMICs, namely X04013MB076 and MSH011MB165, have been realized in Fraunhofer IAF´s in-house metamorphic HEMT technology with a gate length of 50 nm [1]. The metamorphic buffer and single InGaAs main channel were grown by molecular beam epitaxy (MBE) on 100 mm semi-insulating GaAs substrates [2]. The maximum channel current of a 50 nm HEMT device is 1200 mA/mm. At a drain voltage of 1 V, the maximum transconductance is more than 1800 mS/mm. An extrinsic transit frequency of 380 GHz was extrapolated for this process, and a maximum oscillation frequency of more than 670 GHz is calculated from the on-wafer measured current gain and Masons unilateral gain of a 2 x 10 µm common-source (CS) HEMT device. The off-state and on-state breakdown voltages are 2.2 V and 1.6 V, respectively. Based on a failure criterion of 10 % drain current degradation, an activation energy of 1.8 eV and a median time to failure of 4 x 105 h at 100 °C ambient temperature was extrapolated. This process offers two metallization layers, metal-insulator-metal (MIM) capacitors, nickel chromium (NiCr) thin-film resistors, airbridges and a full wafer backside process including wafer-thinning to 50 µm, thru-substrate via-holes and backside metallization.

3.1.2 Fraunhofer IAF 35 nm technology

The ALN002MD160 as well as the AMP015MF_D presented here are processed in Fraunhofer IAF's 35-nm InAlAs/InGaAs metamorphic HEMT IC technology due to their higher working frequencies. The via molecular-beam epitaxy grown layers boast a channel mobility of 9800 cm^2/Vs and carrier density of 6.1E12 cm^{-2}. The front-end-of-line process of the HEMT devices, which are also fabricated on 100 mm GaAs wafers, is described in detail in [3]. The multilayer back-end-of-line process consists of a total of three metal layers separated via

benzo cyclobutene, a thin sheet of chemical vapor deposited silicon nitride - utilized in the layout of MIM capacitors - and NiCr thin-film resistors. The utilized HEMT transistors are processed with an increased gate-drain recess, allowing for drain-source voltages of up to 1.5 V, with the OFF-state breakdown voltage above 4 V. The technology boasts a transition and maximum oscillation frequency of greater than 500 GHz and greater than 1000 GHz, respectively, with a peak transconductance of 2500 mS/mm and drain current density of 1300 mA/mm.

3.2 D-band frequency multiplier-by-four MMIC

An essential part of almost every active millimeter-wave system is a signal source with a high spectral purity. In the TX path of a radio, a signal source is needed to generate the carrier signal while in the RX path it is used as local oscillator signal for the down-converting mixer. There are two kinds of signal sources for generated RF signals based on solid-state devices: A frequency oscillator circuit that generates the desired signal at its fundamental or harmonic tone and a frequency multiplier circuit that multiplies a low frequency signal to the desired frequency range. The needed low frequency signal may be generated with an external PLL-stabilized oscillator, with a frequency synthesizer or with a direct digital synthesis device.

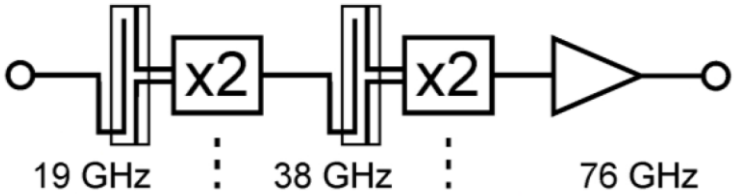


Figure 4: Multiplier-by-four signal chain integrated on proposed MMIC (X04013MB076).

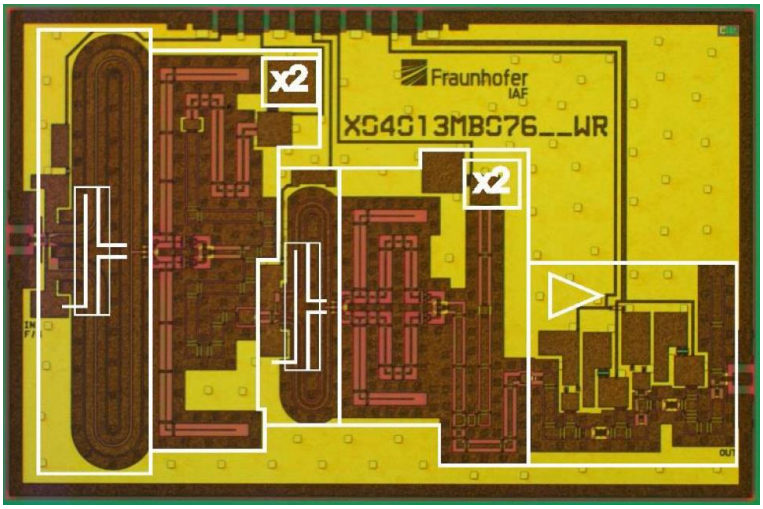


Figure 5: Chip photograph of the multiplier-by-four MMIC (X04013MB076). Chip size: 3 x 2 mm^2.

As depicted in Figure 4, a multiplication factor by four is achieved by cascading two frequency doubler stages. To boost the output power, a buffer amplifier is added after the second frequency doubler stage. All stages were realized in grounded coplanar waveguide (GCPW)

technology with a ground-to-ground spacing of 50 µm. A chip photograph of this frequency multiplier MMIC is shown in Figure 5. The main design challenge in every stage was to keep the suppression of unwanted harmonics as low as possible. Every step to achieve this goal is described in the following sections.

Both multiplier stages are designed as balanced frequency doublers. Using a balanced topology in a frequency doubler has the advantage that the odd harmonics are cancelled out by default. However, as a consequence, the input of the frequency doubler needs to be a differential signal. As the input of each stage is single-ended, it has to be converted into a differential signal. Therefore, Marchand baluns were used in the design. Two identical input matching networks are routing the differential input signal to the gate terminals of the field-effect transistors (FETs). Each network consists of an open-ended stub between two transmission lines. Each FET generates several harmonics of the input signal due to its non-linearity. But not only the frequency itself is multiplied; the phase of the harmonics is also affected. By connecting the drains of both FETs together, the even harmonics are added constructively while the odd harmonics are cancelled out. This effect helps to get rid of the most harmful harmonics directly next to the wanted 2nd harmonic of each stage, which leads to a cleaner spectrum. The output matching network fulfils three functions. Providing the drain bias, matching the output frequency and blocking the input frequency. The last two points are mainly achieved by a two-stage shorted stub with a parallel capacitor in the middle. The lower part of that stub mainly affects the higher frequency while the whole stub transforms the lower frequency. The first frequency doubler uses a 4 x 30 µm FET in CS configuration while the second frequency doubler uses a 4 x 15 µm device. For stability reasons, a resistor-capacitor combination, which consists of a resistor in series with a capacitor-to-ground, is placed in the bias lines. To avoid a drain-voltage drop, the resistor-capacitor combination is placed parallel to the second RF-blocking capacitor. For a better understanding, the schematic diagram of one frequency doubler stage is depicted in Figure 6.

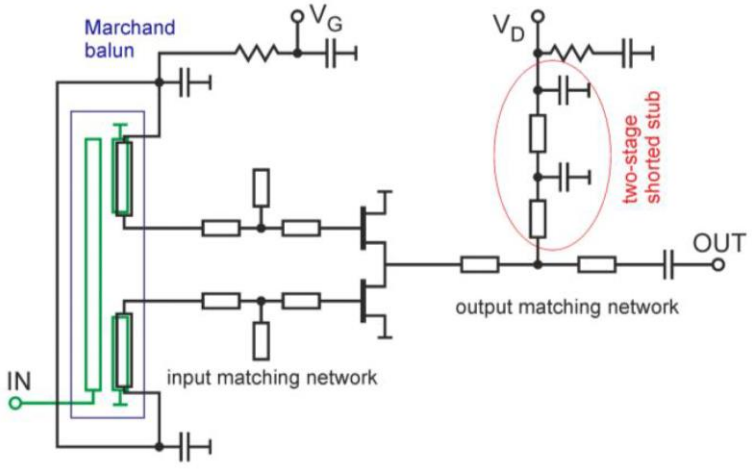


Figure 6: Schematic diagram of one of the frequency doubler stages in the X4 MMIC.

The differential input signal of each frequency doubler stage is provided by a Marchand balun. The Marchand balun has two main advantages: the differential output signal has a nearly constant phase shift of 180° over a wide frequency range and the power level of both branches

are in a relatively good agreement. The drawback of this balun is its large area consumption on the chip due to its electrical length of around lambda-half. Thus, to reduce the chip size as much as possible both Marchand baluns are folded. They are equipped with a very useful feature: the gate bias is routed over both output branches to the gates of both FETs. As Figure 6 explains this behavior, the output branches and the gate bias lines were capacitively coupled. The Marchand balun is inside the blue rectangle. The lines that are responsible for the balun operation are drawn in green while the gate bias lines are black.

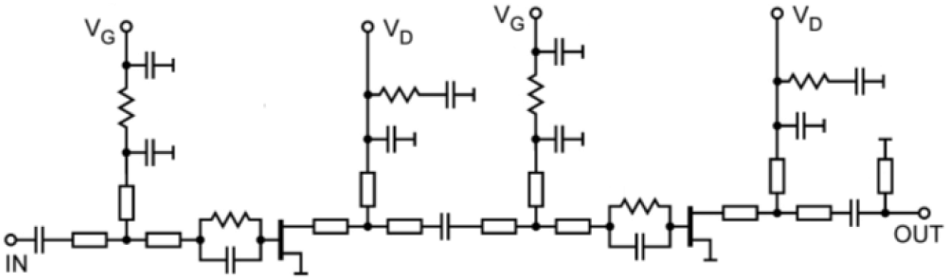


Figure 7: Schematic diagram of the buffer amplifier in the X4 MMIC.

Finally, the buffer amplifier at the output of the second frequency doubler stage has to fulfil multiple functions. It has to boost the output power and to suppress the unwanted harmonics further. Therefore, its frequency response was designed to be as sharp as possible. Because both functions are easier to achieve with a multi-stage topology, a two-stage design has been used. Figure 7 shows the schematic diagram of the buffer amplifier. Both stages use 4 x 40 µm CS FETs as active devices. To ensure a stable device for all impedance conditions a 9.3 Ω resistor was added at the gate terminal of the FET. Parallel to that resistor, a series capacitor with 235 fF was placed. This minimizes a performance degradation over the operating bandwidth. The input and output matching networks consist of a shorted stub between two transmission lines, which are used for biasing the FET. Therefore, they were terminated with an RF-blocking capacitor. The elements of the buffer amplifier were computationally optimized to realize a sharp gain curve next to the operation bandwidth between 70 GHz and 82.5 GHz. For additional filtering, a shorted stub was also placed at its output. To further minimize the chip space consumption, its transmission lines were also folded. For further stability improvement, resistive and capacitive elements were placed into the gate and drain bias paths in an identical way like at the frequency multiplier stages.

3.2.1 Measurement results of X04013MB076

The scalar small-signal measurements are performed by using a vector network analyzer device in a 50 Ω environment. As to be observed in Figure 8, the output buffer of the multiplier-by-four MMIC achieves a small-signal gain of 12.7 dB and a 3-dB bandwidth from 67.5 GHz to 84.5 GHz. The reflection coefficient is better than -6.5 dB at the input and -9.4 dB at the output. The remaining 6^{th} harmonic is suppressed by 17 dBc and the 8^{th} harmonic by 34.7 dBc.

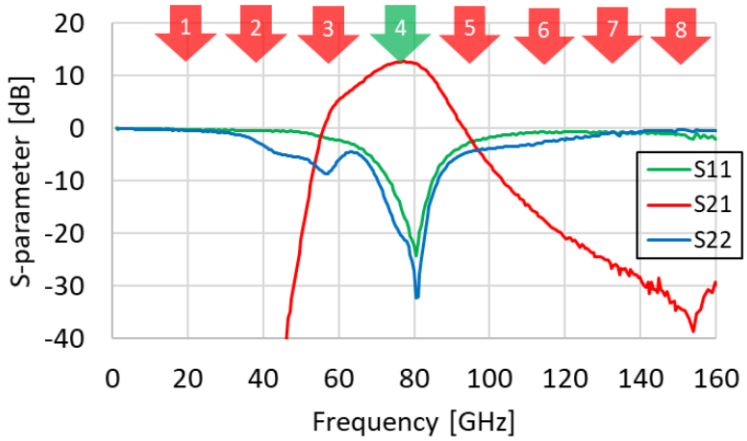


Figure 8: Measured S-parameters of the buffer amplifier in the of multiplier-by-four MMIC with the wanted (green arrow) and all unwanted harmonics (red arrows).

Regarding non-linear power measurements, the MMIC has been characterized with a scalar on-wafer measurement setup, also in a 50 Ω environment, shown in the measurement setup of Figure 9. The input signal is generated by an E8257D synthesizer from Keysight, which is connected via a coaxial cable to an ACP50 probe tip. The complete output spectrum with the wanted and all unwanted harmonics is analyzed via an Anritsu MS2760A spectrum analyzer. It is connected directly on a I145-A-GSG-75 probe tip. Both probe tips were manufactured by Cascade Microtech. The spectrum analyzer captures all harmonics up to the 7th harmonic during the measurement. All the losses of the used probes and the cable were taken into account during the measurement and the power levels were calibrated to the on-wafer reference plane (end of the probe tips). Figure 10 (a) shows a sweep over the input power at an output frequency of 76 GHz. The output power is saturated and constant with Pout = 9.9 dBm at an input power of Pin = 3 dBm and above. The minimum suppression of unwanted harmonics also remains constant at about 61 dBc between Pin = 3 dBm and Pin = 10 dBm.

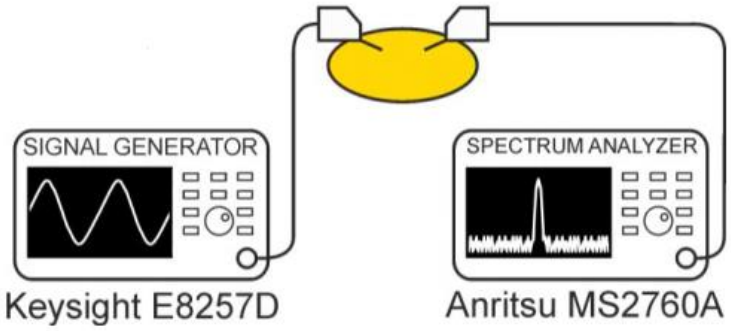
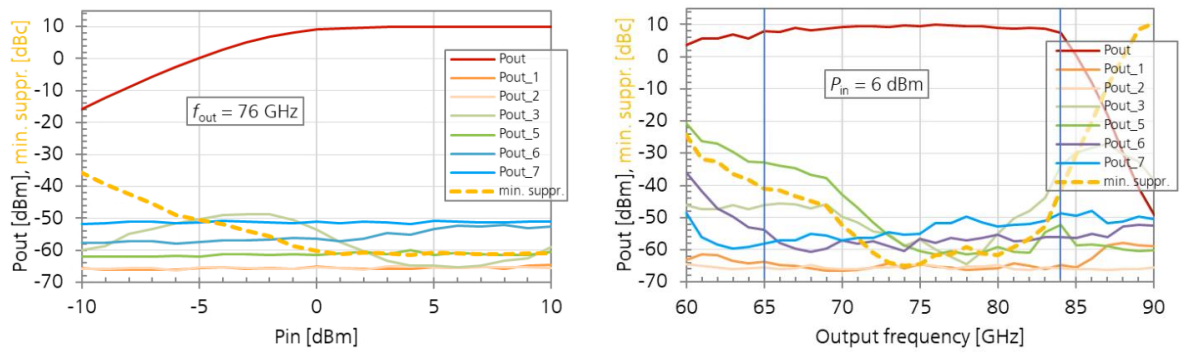


Figure 9: Measurement setup for all non-linear power on-wafer characterization in this deliverable.



(a) (b)

Figure 10: Output power measurement results of multiplier-by-four MMIC (X04013MB076) of wanted (4th, red) and all unwanted harmonics. (a): Input power sweep at 76 GHz. (b): Frequency sweep over E-band.

Figure 10 (b) shows the performance of the X4 frequency multiplier device, in terms of output power and harmonic suppression in the entire E-band between 60 GHz and 90 GHz. In the frequency band between 70 GHz and 85 GHz, which corresponds with input frequencies between 17.5 GHz and 21.25 GHz, the output power of the wanted 4th harmonic varies only around 8.8 and 9.9 dBm, which is a flatness of 1.1 dB. The highest unwanted harmonic, that is generated given this input frequency range, is suppressed by at least 45 dBc. The 3-dB bandwidth is from 65 GHz to 84 GHz which is a bandwidth of 19 GHz or 25.5 %. The output power is 9.0 dBm ± 1.3 dB and over this band, the highest unwanted harmonic is suppressed by at least around 40 dBc. The mean suppression of the device is around 55 dBc, while the power consumption of the MMIC is as low as 104 mW at a drain voltage of 0.8 V. This divides into 36 mW for both frequency doublers and 68 mW for the buffer amplifier at the chain's end.

3.3 Up- and down-converting subharmonic quadrature mixer

The subharmonic quadrature mixer chipset presented here features ultra-broadband IF terminals which enable the direct up and down conversion of signals commonly used in backhauling communication networks.

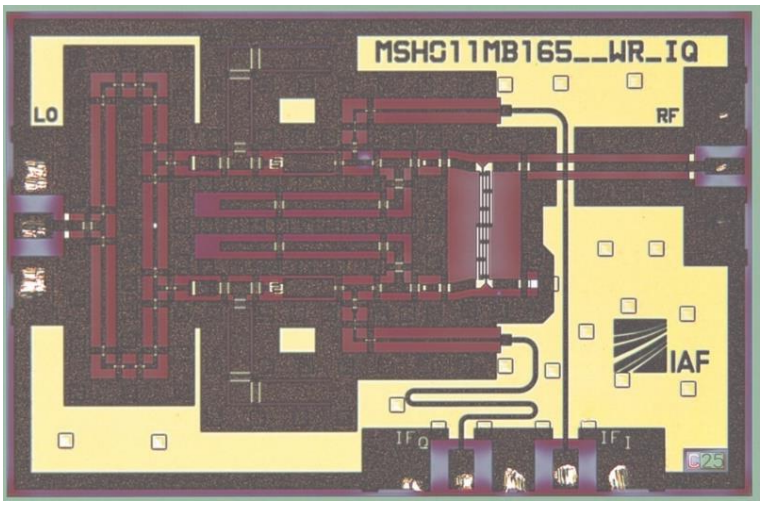


Figure 11: Chip photograph of the subharmonic quadrature mixer MMIC (MSH011MB165). Chip size: 1.5 x 1.0 mm².

This chip, as shown in Figure 11, comprises two resistive mixer cells which use a transistor as voltage-controlled resistor. The RF is split equally in amplitude but 90° out of phase between both mixer cells by a Lange coupler. The LO input signal is divided using a classical broadband Wilkinson power divider. The chipset is designed to operate at fixed LO frequencies in a subharmonic up- or down-conversion scenario. A balanced approach is necessary to ensure a sufficient LO to RF isolation at the transmitter. Otherwise, the leakage of the high power LO signal could saturate the receiving amplifier. Due to the fixed LO frequency and the subharmonic operation, a balanced operation is achieved by another split of the LO signal after the Wilkinson divider using a Lambda-half delay line at the fundamental LO frequency. The signal is then fed into a 4 × 20 µm transistor where two fingers are driven in phase while the remaining two fingers are driven by the 180° delayed signal. The LO signal cancels itself at the transistor's drain while the mixing products at the doubled frequency are interfering constructively. Due to the 90° Lange coupler the resulting IF is also 90° out of phase offering complex IF in-/ and outputs (I/Os). With this chipset, an active integrated receive, transmit chipset for wireless gigabit communication has been successfully realized in a 50 nm HEMT technology.

3.3.1 Measurement results of MSH011MB165

For measuring the output power and conversion gain (CG) over RF and IF frequencies of the presented mixer cell, a similar measurement setup as presented in section 3.2.1 is used, although one additional signal synthesizer is added to either feed the RF or the IF port, depending on the chosen up- or down-converting configuration. I/Os all are calibrated again to the reference plane, which is the end of the probe tips.

For better comparability, the measurements over IF power and IF frequency are performed at the same fixed LO frequency of 160 / 2 GHz, which means 80 GHz as LO input frequency. Figure 12 (a) shows the up-conversion measurement of the RF-port output power vs. IF-Port input power using an LO drive power of 10 dBm and an IF frequency of 1 GHz. Using linear extrapolation of the upper sideband (USB) and lower sideband (LSB) measurement data, the

linear P-1dB output power (OP1dB) point can be extracted at around -2 dBm of IF input power. For other frequencies in D-band, the point is located at the same input power point. Hence, we get a maximum OP1dB of the device in up-conversion mode of around -25 dBm, in combination with a moderate LO suppression of around 25 dBc. Taking into account higher order modulation schemes claiming around 10 dB of input power for back-off operation, the LO suppression is then reduced to around 15 dBc, depicted by the small blue vertical arrow.

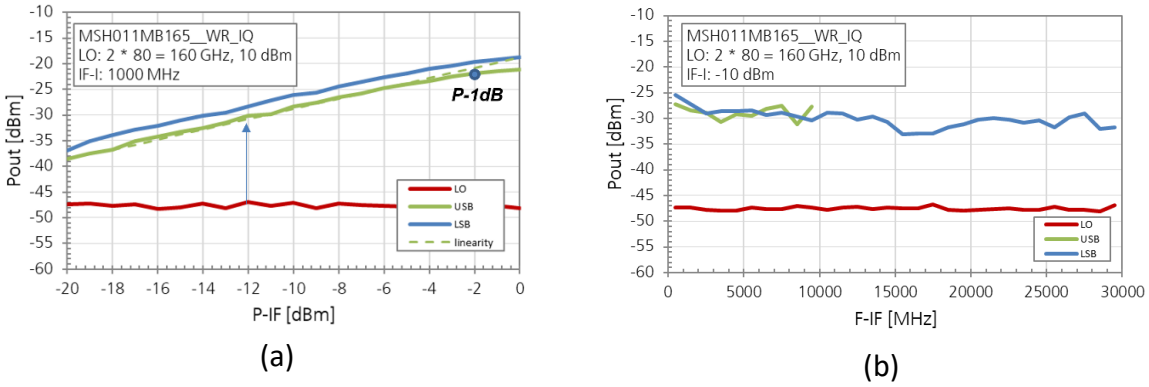


Figure 12: Up-Conversion output power measurement results of MSH011MB165. (a): IF power sweep at 1 GHz IF frequency. (b): IF frequency sweep at -10 dBm IF power.

By fixing the IF power at -10 dBm (back-off operation) but sweeping its frequency from 10 MHz to 30 GHz, we get the measurement curve depicted in Figure 12 (b). It shows a relatively constant behavior of output power over the whole frequency range of around -30 dBm, due to the reduced input power of -10 dBm at the IF port. Also, the LO suppression is quite constant over bandwidth, with its minimum suppression of approximately 15 dBc at around 17 GHz of IF frequency. However, it should be noted, that the targeted application in ARIADNE has to support only 2 GHz of IF bandwidth at least, which seems to be no issue at all, since the conversion gain and the LO suppression shows the best performance in those (lower) frequency ranges. The same statements regarding output power and LO suppression are true when sweeping the RF frequency instead of the IF frequency, as shown in Figure 13.

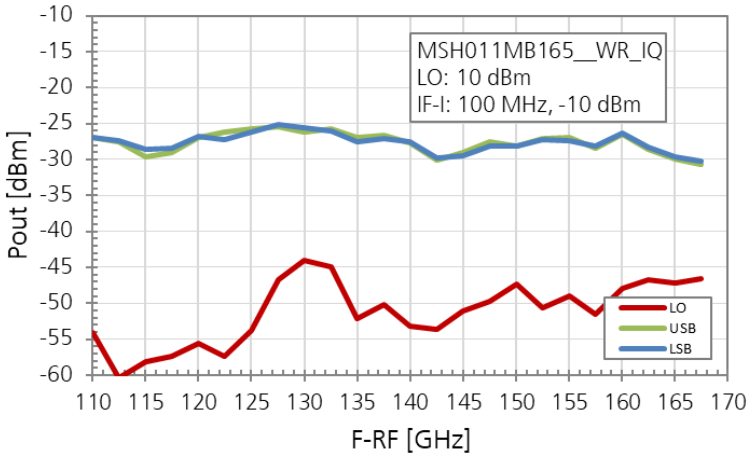
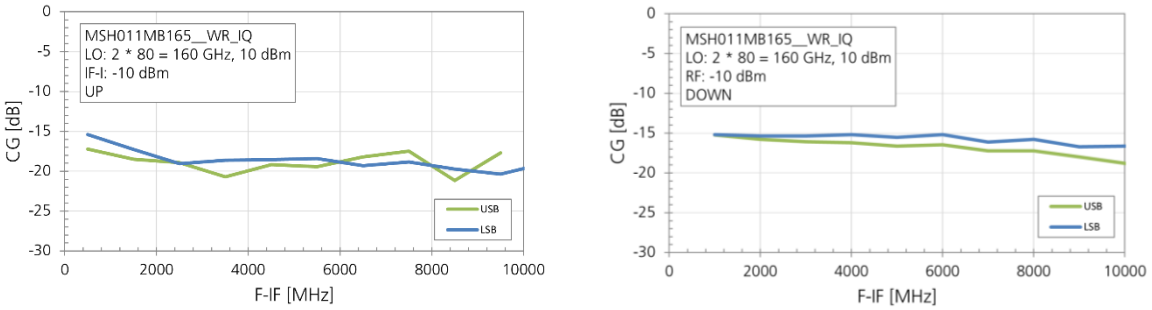


Figure 13: Up-Conversion output power measurement results of MSH011MB165 over RF frequency with fixed LO- and IF frequencies and powers.

Here, one can obtain a variation between around -25 dBm to -30 dBm of output power in the range of the whole D-band frequency range. The LO suppression is worst at around 130 GHz, 150 GHz and 165 GHz, with an effective LO suppression of around 18 dBc.

By using the presented subharmonic quadrature mixer MMIC in a down-converting configuration, small differences in conversion gain can be obtained. This is shown in Figure 14, where – using the same frequency and power constellations for LO, IF and RF signals, respectively – for the up-conversion case, the conversion gain is around -20 dB in the targeted IF frequency range up to 2 GHz, whereas it is around -15 dB for the down-conversion case. Thus, the designed subharmonic quadrature mixer is better suitable for down-conversion scenarios but offers superb performance for the up-conversion case as well.



(a) (b)

Figure 14: Comparison of conversion gain of presented mixer in up-converting (a) and down-converting (b) scenario.

3.4 D-band balanced two-way four-stage power-amplifier

As a post-amplifier in the TX path, a four-stage InGaAs HEMT PA MMIC (AMP015MF_D) is designed to cover the targeted D-band frequency range of 140 GHz to 170 GHz. This PA circuit is implemented in IAF's InGaAs-channel HEMT technology with 35-nm gate length as described in section 3.1.2 with the realized MMIC shown in Figure 15.

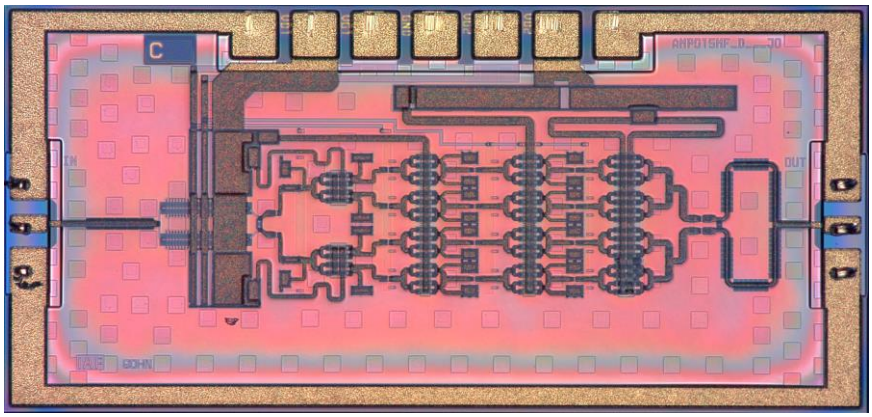


Figure 15: Chip photograph of the 2-way four-stage MPA MMIC (AMP015MF_D). Chip size: 1.5 x 0.75 mm².

Being a two-way balanced design as depicted in Figure 16, the PA features highly optimized I/O matching networks, by making use of Wilkinson power dividers at the respective port of the device. This also reduces insertion losses in the power combining networks. By using different gate- and drain-biasing (V_{GX}, V_{DX}) pads, the optimal drain current density for the respective stage can be adopted. The PA also includes an additional output stage with two parallel 8 × 16 µm HEMTs in CS configuration. The 8-finger cascode devices in the input stages are implemented to provide high gain, while the CS transistors in the output stage permit the maximization of the total gate width, increasing the achievable output power at the given chip size, incorporating adjusted load targets.

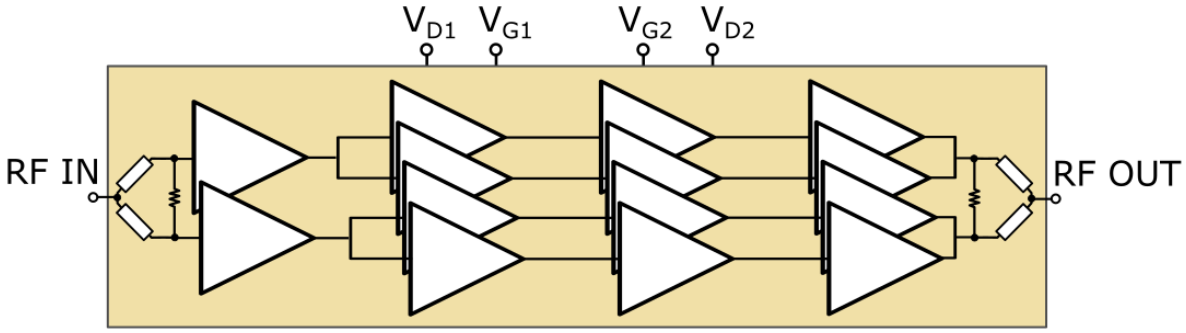
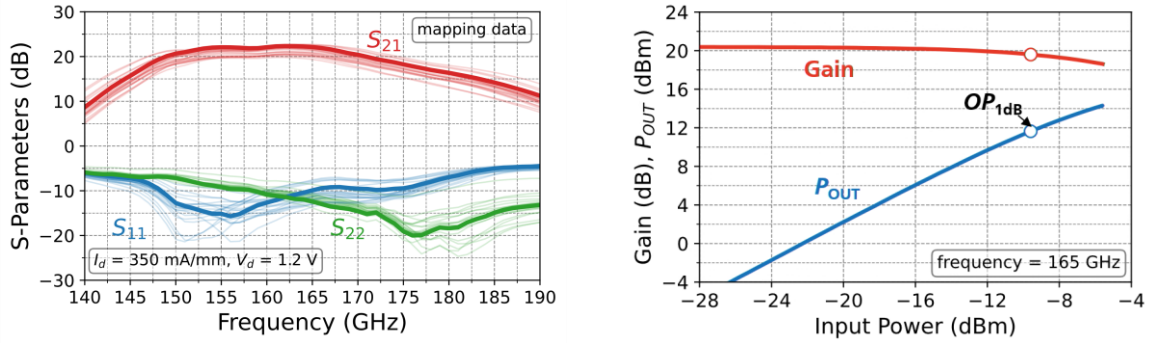


Figure 16: Block diagram of proposed balanced four-stage power-amplifier (AMP015MF_D).

3.4.1 Measurement results of AMP015MF_D

The MMIC was tested and characterized in small-signal as well as large-signal operation with a VNA and scalar PM5 measurement setup, respectively. The measured small- and large-signal characteristics of this 2-way combined PA MMIC are depicted in Figure 17 (a) and Figure 17 (b), respectively.



(a) (b)

Figure 17: Measured S-parameters over frequency (a) as well as gain and power vs. input power characteristics (b).

As can be seen in the large-signal characteristics, this PA typically provides up to 12 dBm OP1dB incorporating a gain of around 20 dB with a saturated output power around 16 dBm at a frequency of 165 GHz. The small-signal gain is in the range of 20 dB to 22 dB in the frequency

range between 150 GHz to 170 GHz. Unfortunately, for the majority of measured cells, the gain shows large drops at frequencies below 150 GHz, thus limiting usable RF sub-band frequencies for a later demonstration.

An overview on the electrical characteristics of the amplifier circuit, including direct current (DC) biasing information, is summarized in Table 1. As to be seen, the device is biased with a nominal drain voltage of 1 V and a respective drain current of 350 mA/mm, which transits to an overall power consumption of around 1 W.

Table 1: Electrical on-wafer specifications at circuit level of AMP015MF_D MMIC.

Port	*Parameter*	*Typical*	*Min*	*Max*
DC	Drain bias voltage (V_D)	+ 1–1.2 V	--	+1.3 V
	Drain current all stages (I_D)	+ 620 mA	--	+1000 mA
	Gate bias voltage (V_G)	0.1 to 0.3 V	–0.6 V	+0.5 V
	Power consumption ($P_{DC,MAX} = V_D * I_D$)	0.75 W	--	1.3 W
RF	RF frequency range	--	150 GHz	175 GHz
	RF input power (P_{in})	--	--	0 dBm
	Saturated RF output power	>16 dBm	--	--
	Linear RF output power (OP_{1dB})	12–14 dBm	--	--
	Linear gain (S_{21})	20–22 dB	--	--
	Power Added Efficiency (*PAE*) (P_{in} = 0 dBm)	appr. 2 %	--	--

3.5 D-band low noise amplifier

Achieving good signal-to-noise ratio (SNR) is an essential need of nearly every RF system. Most effect on the SNR has the noise performance of the first receiver stage after the antenna. The better that noise performance is, the weaker signals can be analyzed which correlates directly with the sensitivity of a communication system. Improving the noise performance of a receiver is the main task of a low-noise amplifier. Thus, for low-noise reception, a four-stage D-band LNA MMIC was designed to achieve high gain and large bandwidth in combination with low noise figure. Therefore, a cascode configuration consisting of a series connection of one HEMT in common source and one in common gate configuration was utilized. The chip photograph of the fabricated LNA MMIC is shown in Figure 18. The use of space saving microstrip (MS) waveguide technology resulted in an overall die size of only 1.5 × 0.75 mm^2.

The heart of each stage is a CS HEMT with symmetrical source lines together with a common-gate HEMT in cascode configuration, both with a gate width of 2 x 15 µm in a MS environment. This combination has several advantages. Compared to a CS device, the cascode configuration has a higher minimum noise figure but taking the noise contribution of the second stage into account the minimum noise figure is lower in total due to the higher gain of the cascode.

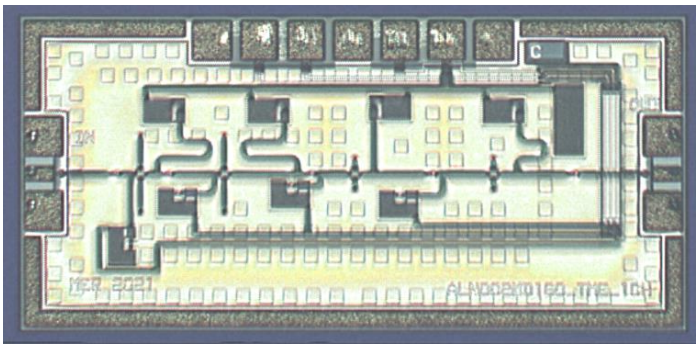


Figure 18: Close-Up of realized D-band LNA (ALN002MD160). Chip size: 1.5 x 0.75 mm².

3.5.1 Measurement results of ALN002MD160

The LNAs were characterized using motorized wafer probers that allow the mapping of all cells on a wafer. On-wafer S-parameter measurements were performed using an Agilent PNA-X vectorial network analyzer, two WR-6 Oleson TX/RX frequency extension modules and two microwave probes. For an LRL-type calibration at the probe tip, a Cascade 138-356 calibration substrate was chosen.

The noise figure performance of the LNAs has been characterized by the noise figure measurement setup as shown in Figure 19. The Agilent N8975A noise figure analyzer controls an Elva ISSN06 noise source and the synthesizer for the generation of the LO of the external sub-harmonic D-band mixer from VDI, to generate an IF signal to be measured by the noise figure analyzer with a frequency of around 100 MHz. The calibration of the noise source is regularly verified with hot/cold measurements using liquid nitrogen to ensure accurate and reliable measurement results.

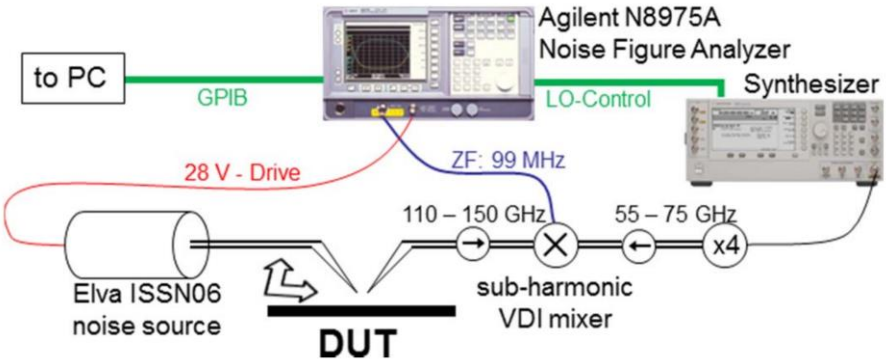


Figure 19: Noise figure measurement setup in D-band.

The on-wafer measured S-parameters as well as the noise figure in the respective frequency band of the amplifier circuit are depicted in Figure 20.

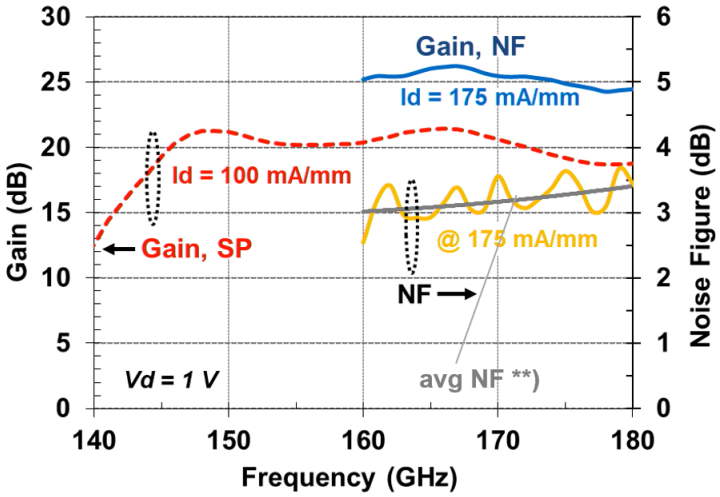


Figure 20: Measured small-signal gain and noise figure of the LNA MMIC over D-band frequencies.

As shown, using a drain voltage of 1 V and a respective drain current of 175 mA/mm, the LNA boasts a small signal gain of 20 dB ± 1.5 dB in the frequency range of 145 GHz to 175 GHz (measurement system is extended over the end of the D-band). The OP1dB shows good linearity for an output power of -1 dBm. Also, the MMIC shows a record average noise figure of around 3 dB to 3.5 dB in the frequency range from 150 GHz to 180 GHz.

3.6 Conclusions on MMIC design & evaluation

Given the good results of presented MMICs, which were manufactured in sufficient quantities, they are able to be used in TX and RX frontend modules including the presented signal chain in section 2 while using a multi-chip configuration. Taking into account previous link budget calculations in combination with the achieved noise figures and (linear) output power levels, this chipset makes it possible to achieve a communication link with a targeted 256 quadrature amplitude modulation (QAM) with a distance of 226 m in D-band as to be presented by the line-of-sight (LoS) project demonstrator 1, described in the respective deliverables of WP 5. However, as shown in the previous sections, by combining the various MMICs to TX and RX signal chains as proposed, the targeted frequency range will be limited to around 150 GHz to 170 GHz, or rather 150 GHz to 160 GHz, to stay inside of the respective -3 dB bandwidths of proposed MMICs. Future endeavors are to be fixing those issues, by incorporating the presented designs into a single-chip solution choosing IAF's 35 nm technology due to superior noise figure performance.

4 RF housing integration

The RF MMICs presented in chapter 3 are powerhouses of advanced semiconductor technology, able to drive the wireless communication links to be presented in the project demonstrators. However, beneath their remarkable capabilities lies a critical necessity: appropriate packaging. The packaging of RF MMICs is not just an afterthought; it is an essential element that empowers these circuits to reach their full potential.

- Due to the usage in different project demonstrators and at different sites (outdoors / indoors) in the project, the MMICs have to be protected from external elements that could compromise their functionality and reliability. Thus, packaging acts as a mechanical shield, providing a robust barrier against moisture, dust, temperature fluctuations, and mechanical stresses. By safeguarding RF MMICs, packaging ensures their longevity and uninterrupted performance, allowing them to excel in demanding environments.
- As the presented RF MMICs operate at high frequencies and power levels, they generate substantial heat due to the relatively low power added efficiency. If left unmanaged, this heat can impair their performance and even lead to premature failure. The targeted packaging has to offer a crucial thermal management solution to ensure consistent performance and extend their lifespan.
- All of the developed RF MMICs thrive on maintaining signal integrity, especially at targeted D-band frequencies where losses and distortions are potential challenges for communication scenarios. Packaging plays a vital role in preserving the integrity of these signals. By incorporating specialized transmission lines on high-frequency printed circuit board materials and fused silica substrates as well as employing proper shielding techniques, the targeted packaging minimizes signal losses, reflections, and electromagnetic interference. This ensures that the results presented stay in their intended performance while being packaged.
- In the pursuit of technological advancement, size reduction and integration are key goals. Packaging facilitates the integration of RF MMICs into compact systems. Through advanced packaging techniques such as wire-bonding and chips-on-board, multiple MMICs can be combined onto a single substrate or into a single module, enabling miniaturization and reducing system complexity. This integration not only saves valuable space but also enhances system performance, as it eliminates the need for bulky external components and optimizes electrical intermediate connections.
- For the usage in the demonstrators of WP 5, there are specific needs for different antenna gains due to different use-case scenarios as to be seen in previous deliverables of said WP. Thus, the package form factor has to enable the integration of different antennas with sizes (or gains) varying tremendously, which is why the RF modules need a general waveguide interface for an easy antenna replacement. This interface furthermore has to be able to support two different polarizations for a targeted polarization multiplexing in demonstrator 1.

4.1 RFIC packaging concept

A package concept has been evolved out of the requirements given in the previous section. The package supports a circular waveguide (CWG) interface to enable PDM and is based on cost-efficient printed circuit board (PCB) technology, with hybrid usage of metallic bodies for an enhanced heat dissipation and precision MMIC cavities for best overall RF performance.

Due to the similarity of the TX and RX frontend signal chain as shown in chapter 2, the module concept is thought in a way, that most of the hardware of a possible packaging is re-usable to decrease the needed variation complexity to ease and speed-up the manufacturing and assembly process. Hence, a concept depicted by Figure 21 has been developed, in which a universal low-frequency PCB acts as a carrier for a high-frequency sub-mounting part, both consisting of PCB technology in combination with board-to-board connectors to supply the necessary signals to the respective boards. Having a modular design also eases possible debugging steps for an initial operation. Embedded on the low-frequency part there is a microcontroller circuit acting as a tool to safely boot-up the modules by performing stable power-up sequences while also supervising any kind of biasing failure. The microcontroller as well controls multiple digital-to-analog converter ICs to generate all the various gate- and drain-voltages for the respective MMIC. Also, switched power supply (SPS) as well as low-dropout linear regulator (LDO) ICs are embedded there to supply the necessary voltages to the board-to-board connectors. A metal body at the bottom of the low-frequency part is used to improve heat dissipation, for example, to a metallic heatsink, due to the high-power demands of the PA MMICs. By choosing LDOs as the last step in the power-supply circuitry, the MMICs get the lowest power-supply induced noise as possible, since the power-supply rejection ratio (PSRR) of chosen LDOs is very high, leading to lowest spurious artifacts in the transmitted / received signals.

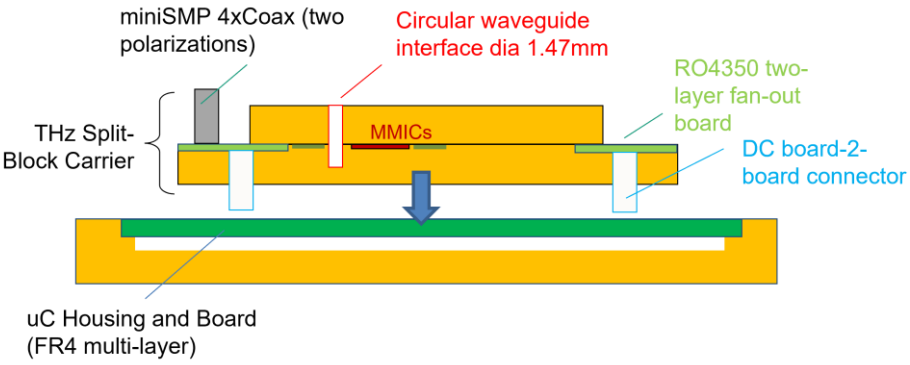


Figure 21: ARIADNE RF module concept.

The high-frequency part is a hybrid split-block package including all of the presented RF MMICs shown in Figure 2 or Figure 3 for the TX or RX module, respectively. This part also incorporates a high-frequency PCB with RO4350 substrate material to guide the LO baseband signals around 20 GHz as well as the IF signals around 2 GHz by using low-loss and low-noise GCPW configuration. To reduce the number of needed transitions and therefore keeping the losses as low as possible, mini-SMP coaxial connectors are placed on the high-frequency part to feed-

in the LO signals and feed-in or feed-out the IF signals as well to be connected to a baseband system externally.

4.2 Realization of MMIC integration

Shown in Figure 22, a detailed assembly plan of the designed and realized high-frequency part of the package is shown. In this case, the assembly plan for the RX front end module is shown. As to be seen, low-loss fused silica transmission lines (parts 9 and 10) between the separate MMICs (parts 3, 4 and 5) are used. All the transitions from and to the MMICs are realized via wire-bonding, using 18 µm thick gold wires. To reduce the pitch sizes for wire-bonding the DC-connections, fused silica pieces (parts 7 and 8) are used as well, since the pitch of the used PCB technology would be too high for the spacing of the DC pads of presented MMICs. Decoupling capacitors (parts 14 and 15) are also embedded into the high-frequency part in close vicinity of the MMICs for each DC connection to suppress unwanted oscillation introduced by long supply traces.

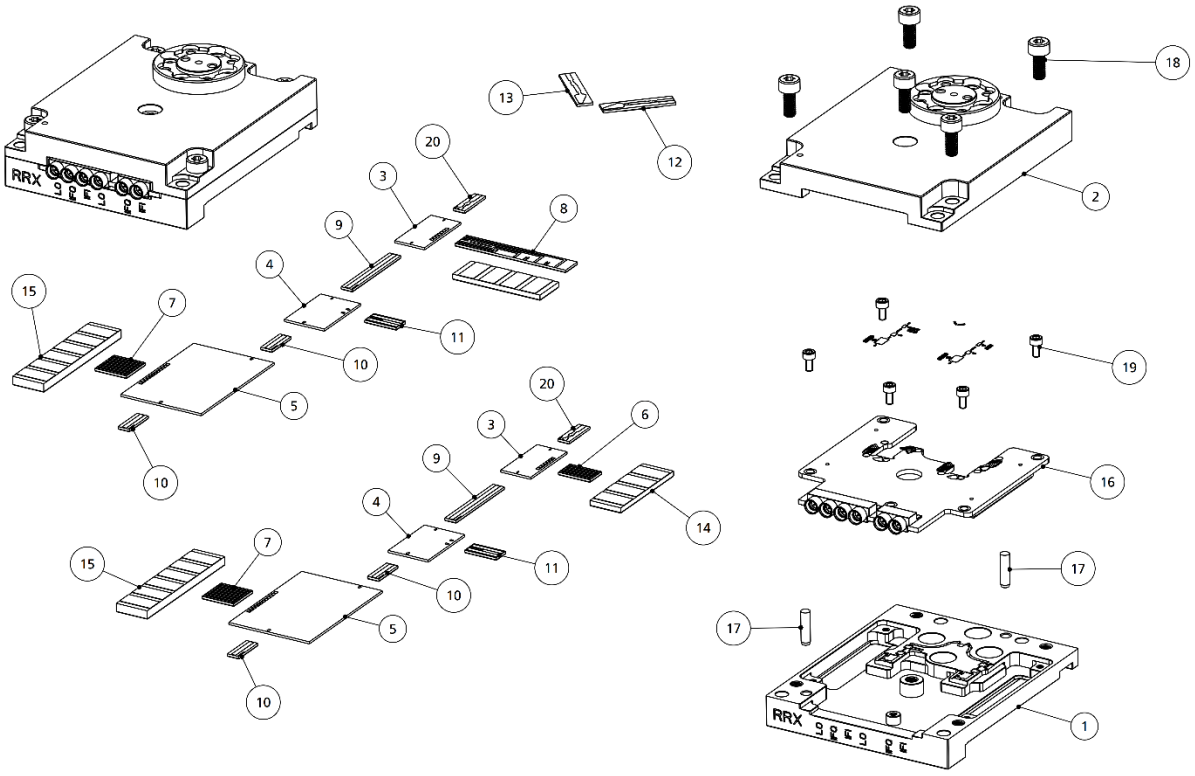


Figure 22: MMICs & fused silica passive DC & RF structures to be included into the RF Frontend.

To feed into the split-block circular-waveguide structure, a by-simulation optimized E-field probe (part 20) is used. Due to the dual-polarization nature of the package, the MMIC chain of course has to be implemented twice per module, to support two independent IF data streams for doubled data rates. Meanwhile, fused silica PDM antenna structures (parts 12 and 13) feed into or receive from the CWG flange, though better to be observed in Figure 23.

In this figure, a rendered image of the fully assembled frontend module is shown. Furthermore, the high amount of needed external IC components (microcontroller, SPS, LDO)

can be observed on the low-frequency DC carrier board, referring to section 4.1. The high-frequency RF sub-mount is attached to the bottom part by using four screws, which also creates a firm and stable analog RF-ground connection. An external DC power supply connector as well as a micro-USB connector is placed on the low-frequency board as well which supports appropriate voltages and currents and which can be used to re-program bias voltages or read-out module parameters, respectively.

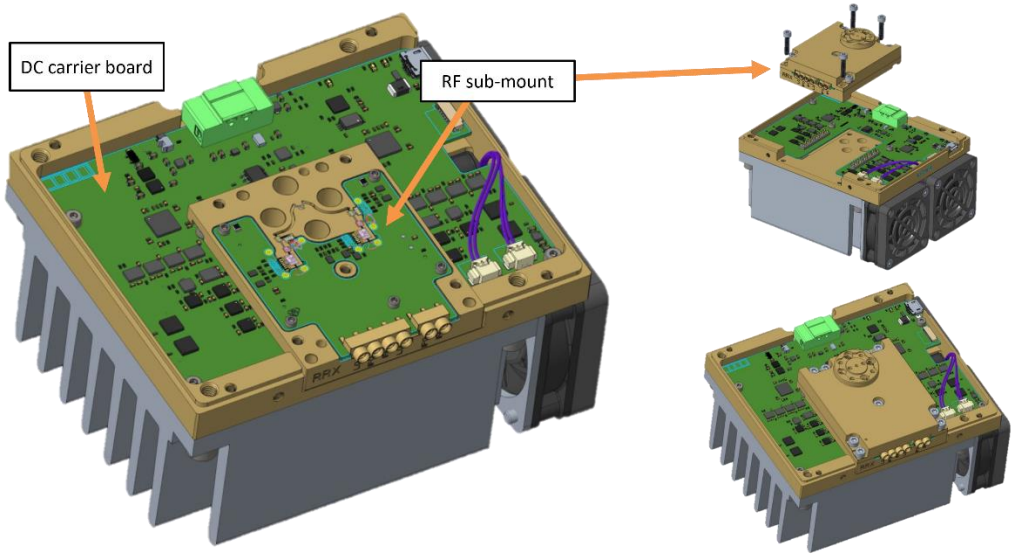


Figure 23: Finalized CAD design of RF module by combining the DC carrier (low-frequency) part with the RF sub-mount (high-frequency) part (rendered images).

4.3 Manufactured frontend modules

To test the performance of realized modules, multiple low-frequency and high-frequency parts were manufactured, gold-plated and their PCBs were assembled. In Figure 24, there is an exemplary photograph of one of the TX high-frequency sub-mount parts of a frontend module. Embedded on the PCB of this hybrid assembly, the mini-SMP connectors, as well as the GCPW lanes, the MMICs and the CWG with the passive polarization multiplexing structure are clearly visible. It should be noted that the LO lines are several centimeters long - and although GCPW structures and PCB material suitable for RF frequencies are used - the losses for those signals around 20 GHz are to be expected quite high. As to be observed in the upper part of the RF sub-mount (right), individual filtering structures for the respective MMIC cavities were developed and realized by using precision milling tools as well.

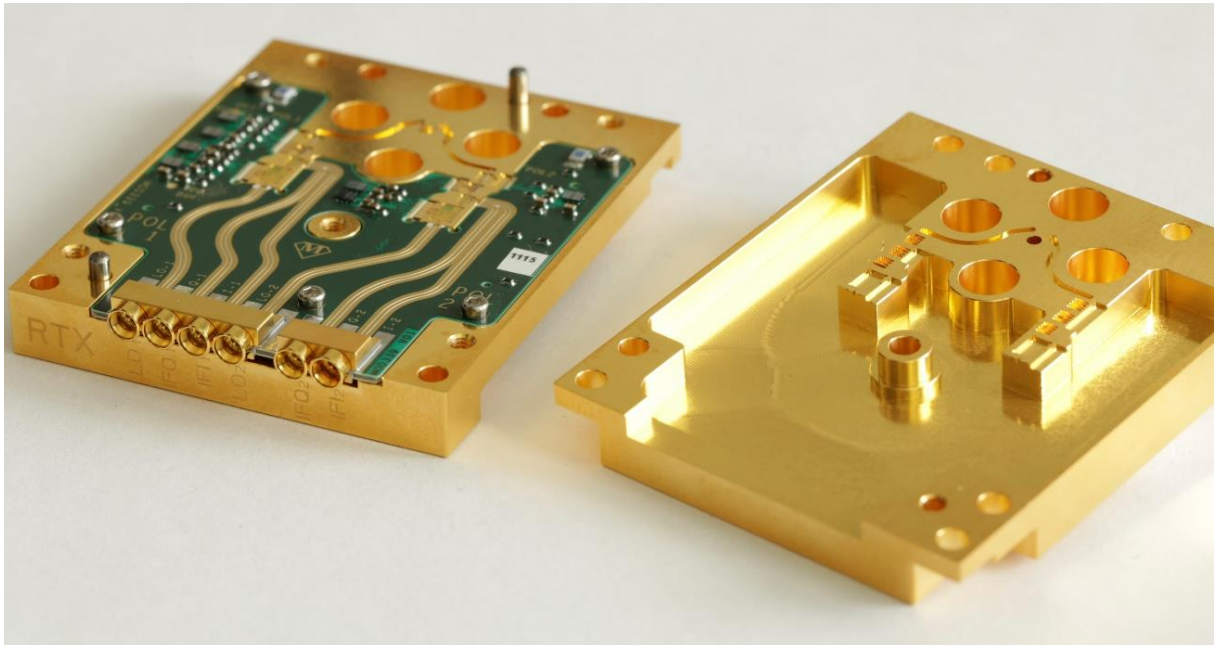


Figure 24: Bottom and top part of the realized RF mechanical housing for MMICs (here: TX sub-mount part).

As depicted in Figure 25, a conjunction of the high-frequency and low-frequency part is possible. The top lid, which is a 3D-printed part, is missing in this image for a better visibility of all the used components. By using this lid, only the mini-SMP connectors, the DC connector, the micro-USB connector as well as the CWG flange are accessible for an in-system embedding process. Also to be observed in this image is the big heatsink on the bottom of the module, which is accompanied by two 40 mm fans to increase power dissipation even more.

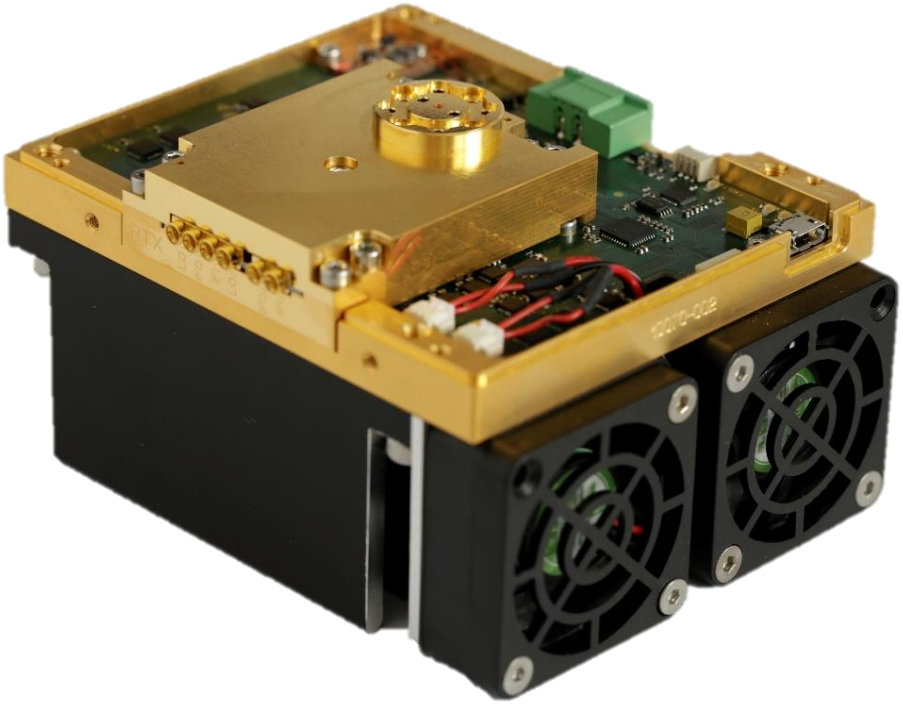


Figure 25: Photograph of a finalized ARIADNE frontend module (top lid removed for better visibility. Here: TX frontend module)

The external connections (RF-wise) are depicted in detail in Figure 26. In case of the TX module, the waveguide connection is an output and the IF connections for both polarizations are inputs, whereas in case of the RX module, the waveguide connection is an input and the IF connections for both polarizations are outputs. In both cases, the LO connections are inputs to be supplied by an external signal synthesizer device or PLL-stabilized voltage-controlled oscillator circuit.

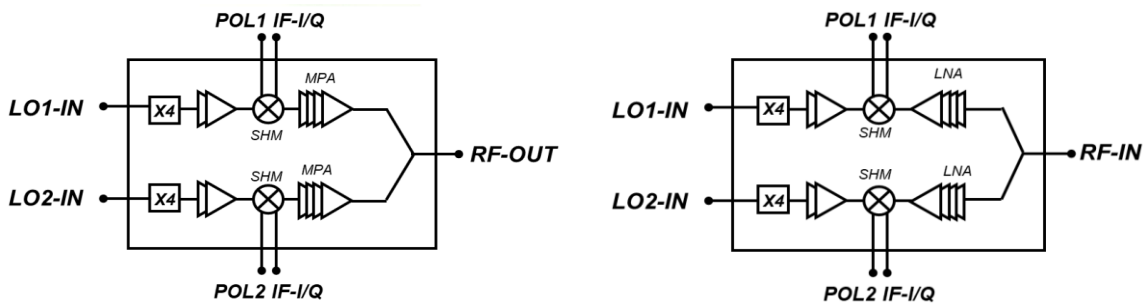


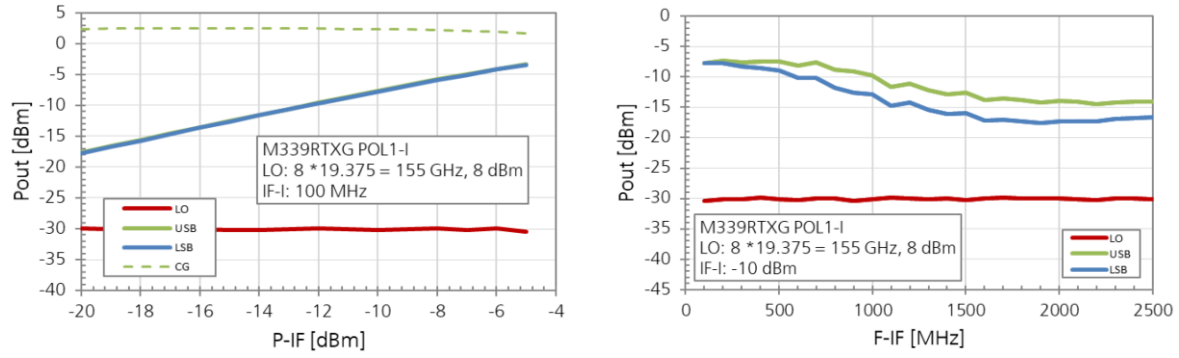
Figure 26: External interfaces of TX (left) and RX (right) RF module, used for measurements

4.4 RF & DC measurements of frontend modules

In this subsection, RF & DC measurements of the manufactured frontend modules, as shown exemplarily in Figure 25, are described. Now being fully integrated devices, the performance of particular MMICs inside of the modules can't be evaluated anymore, thus the overall performance of the full TX or RX chains as given in section 2 are reported here. Only up- and down-conversion characterization is possible now, while the PA in the TX and the LNA in the RX devices virtually increase the measured conversion gain. Due to the shear amount of measurement data generated by characterizing multiple assembled modules as well as multiple polarization paths per module and multiple IF signal connections per path due to their quadrature nature as well, the following performance results show the average module behavior and are to be applied for other polarizations, IF paths and RF modules as well. However, datasheets for each specific module including all measurement information were generated to be used for initial operation in the project demonstrators. It has to be noted, that the mini-SMP connectors are directly connected to the respective MMICs in the module, thus measures against electrostatic discharge must be taken before handling the devices to not damage the MMICs.

4.4.1 TX module measurements (M339RTXG)

Using the same measurement setup as described in section 3.3.1 but calibrated to the end of multiple RF waveguide flanges instead of on-wafer probes, multiple up-conversion mixer measurements of realized TX modules have been performed, to characterize the output power behavior over various system parameters. The internal denotation of the TX frontend module is "M339RTXG".



(a) (b)

Figure 27: Up-Conversion output power measurement results of an exemplary TX frontend module at 155 GHz with an LO power of 8 dBm. (a): IF power sweep at 100 MHz IF frequency. (b): IF frequency sweep at -10 dBm IF power.

As to be observed in Figure 27 (a), the output power reachable using a back-off IF power of -10 dBm at an IF frequency of 100 MHz boosted to -7 dBm at the CWG flange interface by making use of the large gain of the D-band PA device. By keeping the IF power at -10 dBm (back-off operation) and sweeping the frequency in a range the demonstrator is going to use, the output power varies between -7 dBm to -17 dBm as depicted in Figure 27 (b). This slope in output power is particularly visible by observing the output power versus LO frequency plot in the range of 155 GHz to 157 GHz, shown in Figure 28. The quasi-sinusoidal oscillation in output power probably arises by non-ideal suppression of unwanted cavity oscillations by the designed filtering structures as described in section 4.3 or by parasitic coupling of field energy into the cavity openings of the fused silica RF interconnects as shown in Figure 22. Due to the long LO traces as described in section 4.3, the LO power, here being the LO input power at the mini-SMP connectors, is increased to 8 dBm to deliver an input power of around 4 dBm to the multiplier-by-four MMIC.

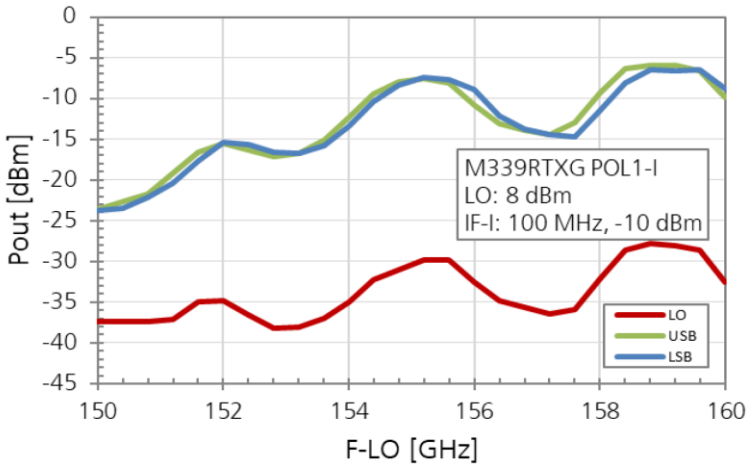


Figure 28: Up-Conversion output power measurement results of an exemplary TX frontend module over various LO frequencies with fixed IF frequencies and powers.

To conclude, the average output power of the manufactured TX frontend modules is oscillating between around -25 dBm to -5 dBm in the frequency range of 150 GHz to 160 GHz. Thus, the link frequency for planned demonstrator has to be chosen carefully.

In Table 2, necessary electrical specifications of an exemplary TX frontend module are given. It has to be noted, that the maximum DC voltage to be applied must not exceed 3.5 V, as well as the IF input power must not exceed -5 dBm to protect the mixer from being destroyed. The LO input power must not exceed +10 dBm to not destroy the multiplier-by-four MMIC.

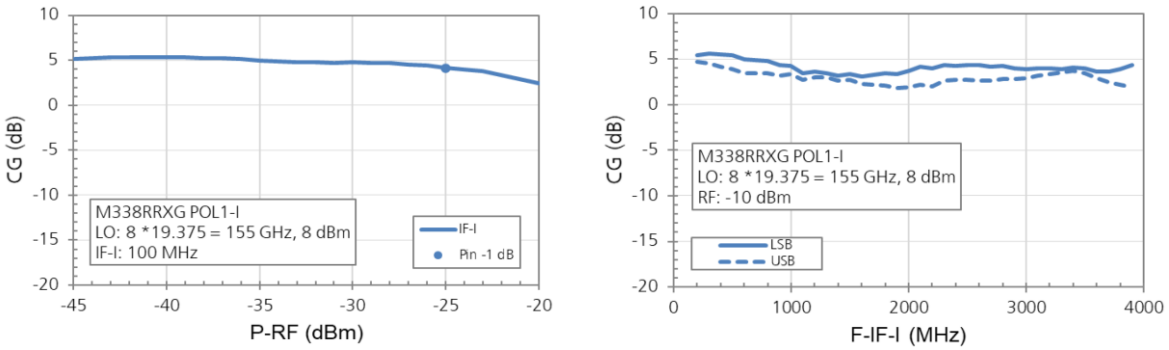
Table 2: Electrical specifications of developed TX frontend module.

Port	*Parameter*	*Typical*	*Min*	*Max*
DC	DC voltage @ connector	3.5 V	3.3 V	3.5 V
	DC current	1590 mA		1645 mA @ P-LO 8 dBm
LO-IN	LO-IN input power	8 dBm	6 dBm	10 dBm
POL1 RF-OUT	RF-OUT output power			-3 dBm
	RF-OUT frequency range		150 GHz	160 GHz
POL1 IF-I/Q-IN	IF-I/Q input power	-10 dB		-5 dBm
	IF-I/Q input frequency		0 GHz	2.5 GHz
POL2 RF-OUT	RF-OUT output power			-3 dBm
	RF-OUT frequency range		150 GHz	160 GHz
POL2 IF-I/Q-IN	IF-I/Q input power	-10 dB		-5 dBm
	IF-I/Q input frequency		0 GHz	2.5 GHz

*) all values referred to module interface

4.4.2 RX module measurements (M338RRXG)

Using the same measurement setup as described in section 3.3.1 but calibrated to the end of multiple RF waveguide flanges instead of on-wafer probes, multiple down-conversion mixer measurements of realized RX modules have been performed, to characterize the CG behavior over various system parameters. The internal denotation of the RX frontend module is “M338RRXG”.



(a) (b)

Figure 29: Down-Conversion CG measurement results of an exemplary RX frontend module at 155 GHz with an LO power of 8 dBm. (a): RF power sweep while maintaining a constant IF frequency of 100 MHz. (b): IF frequency sweep at -10 dBm IF power with an RF power of -10 dBm.

As already observed in the sole MMIC down-conversion measurements in section 3.3.1, the overall RX frontend module performance is superior compared to the up-conversion results as well. This probably results in the already present LO-RF-compression of presented subharmonic mixer cell in the up-conversion case. However, for the receiving case, there now are way lower power levels present at the HEMT devices as shown in Figure 29 (a). The OP1dB point can be extracted for an RF input power of around -25 dBm. In case of an up-conversion scenario, the achieved power levels would be much higher, as presented in the previous section. So, the CG of an RX frontend module is able to boast a solid 5 dB over input RF power levels at an IF frequency of 100 MHz by making use of the additional LNA in front of the subharmonic mixer. Regarding the IF frequency sweep shown in Figure 29 (b), there is no oscillation present as it was in the up-conversion case before. This reinforces the claim of being a systematic problem of the assembly techniques used in the TX frontend module, probably at the TX PA device. The RX frontend module shows a rather constant CG of 5 dB ± 1 dB over targeted IF frequencies in the range of 0 to 2 GHz using an LO power of 8 dBm Due to the long LO traces as described in section 4.3, the LO power is increased to supply the multiplier-by-four MMIC with an approximate input power of around 4 dBm.

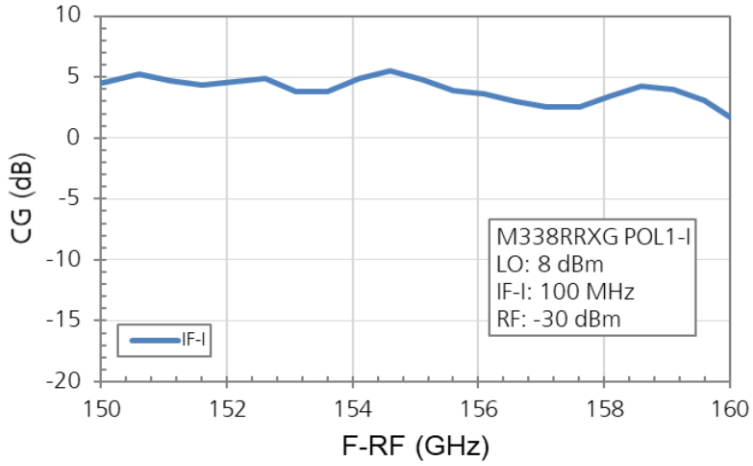


Figure 30: Down-Conversion CG measurement results of an exemplary RX frontend module over RF frequency with fixed LO- and RF frequencies and powers to generate an IF signal at 100 MHz.

Finally, sweeping the RF frequency and keeping a constant IF frequency of 100 MHz in combination with an input RF power of -30 dBm, the non-oscillating CG of developed RX modules can be observed in Figure 30. The worst-case CG value is around 2 dB at a RF frequency of 160 GHz .

In Table 3, necessary electrical specifications of an exemplary RX frontend module are given. It has to be noted, that the maximum DC voltage to be applied must not exceed 3.5 V. No DC-offset is allowed at the IF output ports as well; thus, appropriate coupling has to be ensured for a safe operation of the devices. As for the TX module case, the LO input power must not exceed +10 dBm to not destroy the multiplier-by-four MMIC.

Table 3: Electrical specifications of developed RX frontend module.

Port	*Parameter*	*Typical*	*Min*	*Max*
DC	DC voltage @ connector	3.5 V	3.3 V	3.5 V
	DC current	355 mA		385 mA @ P-LO 8 dBm
LO-IN	LO-IN input power	8 dBm	6 dBm	10 dBm
POL1 RF-IN	RF-IN input power			-25 dBm
	RF-IN frequency range		150 GHz	160 GHz
POL1 IF-I/Q-OUT	IF-I/Q conversion gain	4 dB		
	IF-I/Q frequency		0 GHz	2.5 GHz
POL2 RF-IN	RF-IN input power			-25 dBm
	RF-IN frequency range		150 GHz	160 GHz
POL2 IF-I/Q-OUT	IF-I/Q conversion gain	4 dB		
	IF-I/Q frequency		0 GHz	2.5 GHz

*) all values referred to module interface

4.5 Conclusions on RF housing integration

By hybrid combination of state-of-the-art split-block RF packaging methods and low-cost PCB-based embedding techniques, it is possible to retain the RF performance of presented MMICs to a very high degree while enabling cost-efficient and easy-to-debug designs. The presented RF module results shown make it possible to use the targeted ARIADNE signal chains as presented in chapter 2 in hardware demonstrators of WP 5 with a back-off output power of up to -7 dBm for the up-converting (TX) case and a CG of up to 5 dB for the down-converting (RX) case. Due to the high DC-consumption as given in Table 2 due to the PAE of approximately 2 % of the PA MMIC used in the TX modules, a rather big heatsink is used to ensure safe operation without possibly damaging the devices.

5 Conclusion

A summary of this investigation of the second RFIC design phase in ARIADNE reveals several key findings that need to be highlighted. From a project perspective, the primary objective of the second phase was the finalization of the design, manufacturing and performance evaluation of a broadband baseline transceiver chipset to provide hardware input to the project's experimental phase in WP 5. The chipset to be designed and manufactured meant to enable the demonstration and exploration of communication links with high spectral efficiency, including modulation schemes up to 256-QAM and PDM transmission. Investigating a system-topology for a multi-chip solution while maintaining flexible channel selection and configuration of uplink and downlink frequencies were of particular interest. It is worth noting that the results presented in this report are unique, as there is currently no commercially available chipset suitable for implementing the targeted frequencies in a PDM configuration with given performance. The realization of an initially targeted transfer process onto silicon substrates in task 3.2 posed more challenges than initially expected due to personnel shortage and sick leave due to the pandemic. This reduced the in-house manufacturing capabilities tremendously which triggered the decision to make use of a more traditional multi-chip concept with MMICs realized in a classical 35 nm and 50 nm InGaAs HEMT technology as described in section 3.1.

Nevertheless, after discussing the design decisions for each single RFIC device, their performance is evaluated using state-of-the-art RF measurement equipment and methods. As described in section 3.2.1, 3.3.1, 3.4.1 and 3.5.1, the chipset boasts good performance for D-band transmission links in some of the targeted major frequency sub-bands. The MMICs were manufactured in sufficient quantities. Taking into account link budget calculations of previous deliverables in combination with the achieved receiver noise figure being as low as 3 dB to 3.5 dB and (linear) OP1dB of up to 12 dBm of output power incorporating a gain of around 20 dB at the transmitter output in the frequency range of 150 GHz to 180 GHz, this chipset makes it possible to achieve a communication link in a high spectral efficiency and long-range scenario. This is to be presented by the LoS point-to-point project demonstrator 1, described in the respective deliverables of WP 5. However, as also shown in the previous sections, by combining the various MMICs to TX and RX signal chains as proposed, the targeted frequency range is limited to around 150 GHz to 170 GHz, or rather 150 GHz to 160 GHz, to stay inside of the respective -3 dB bandwidths of proposed MMICs, due to a non-wideband behavior of the PA.

By hybrid combination of state-of-the-art split-block RF packaging methods with low-cost PCB-based embedding techniques, it was possible to retain the RF performance of presented MMICs to a very high degree while enabling cost-efficient and easy-to-debug designs. The presented RF module results shown in section 4.4.1 and 4.4.2 boast an output power in a -10 dB back-off operation of up to -7 dBm for the up-converting (TX) case and up to +5 dB of CG for the down-converting (RX) case. Due to the high DC-consumption of the TX module through the use of a PA MMIC the use of appropriate power dissipation by using chunky heatsinks are indispensable.

For more detail on to the usage of the RF frontend modules in the project demonstrators, the reader is referred to the deliverables of WP 5, especially D5.3.

6 Bibliography

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