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Five-level cascaded H-bridge inverter for renewable energy applications

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ABSTRACT

This paper presents a five-level inverter based on the phase-disposition pulse width modulation (PD-PWM) technique for renewable energy applications. The conventional cascaded H-bridge (CHB) five-level inverter structure is reproduced, and an LC filter is designed to get optimum results from the inverter output. Two batteries are used as renewable energy sources to investigate the performance of the designed inverter. The system can provide 220 volts and 50 Hz AC supply with a 6.9 kW power supply to the load/grid. The designed output is compared with filter and without filter circuit. It provides sinusoidal voltage and current output with a very low total harmonic distortion (THD) of 2.75% which is compliant with IEEE 519 standards. MATLAB/Simulink software tool is used for the entire design. The inverter's output is graphically represented, and discussed various parameters like switching frequency, THD, modulation index, and rated voltage.

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1. INTRODUCTION

Inverters have been used to get a sinusoidal wave by converting DC to AC waveform. Though two-level and three-level inverters are most common in academic research and industrial use purposes, multilevel inverters (MLI) are often preferred for their number of voltages steps, because it assists to make a sinusoidal wave of output voltage or current [1]. Nowadays, wide-bandgap semiconductors materials are used for the operation of higher voltages and frequencies as it has many advantages. Multilevel inverters are used in a system where high voltage is required and consequently flying capacitor-based multilevel converters are used to divide high blocking voltages through switching cells like The metal oxide semiconductor field effect transistors (MOSFETs) or insulated gate bipolar transistor (IGBT) [2]. The compact size of inverters used in residential and commercial grids is one of the important aspects for researchers to minimize installation, operation, and maintenance costs.

The multilevel inverter can work on higher switching frequency which permits the inverter to make input and output voltage regulation more effective, but it causes higher switching loss and lower efficiency. On the other hand, a lower switching frequency causes lower switching loss and provides high efficiency.

Multilevel inverter reduces the total harmonic distortion (THD) by improving output power quality [3]. H-bridge inverter topology provides less THD in the output voltage/current waveform when it is based on pulse width modulation (PWM) technique compared to non-PWM inverters; because PWM techniques push the unwanted frequency content to near the switching frequency [4]. MLI has staircase waveform quality, reduced problems of electromagnetic compatibility (EMC), and smaller common mode voltage [5]. There are four different types of multilevel inverter technologies that exist neutral point clamped (NPC) based, diode clamped (DC) based, flying capacitor (FC) based, and cascaded H-bridge (CHB). Comparatively, cascaded H-bridge (CHB) MLI provides low THD, and it is suitable for various power supply applications like regenerative type motor drive, and electric vehicles based on fuel cells [6].

To filter inverter circuits for eliminating THD, active or passive components are broadly used due to their availability, cheapness, and simplicity in design. Generally, the inverter's filter design is based on ripple current calculation and optimizing power loss. Iterative algorithms can be used to filter THD and get pure sinewave voltage/current output. There are several filter networks like LC, LCL, and series, and parallel LCL damping is used in inverter filtering circuits. Lower-order harmonics can be eliminated using the selective harmonic elimination (SHE) technique [7].

The author of the paper [8] presented a five-level inverter by using a reduced number of switches compared to the conventional five-level inverter, and it provides 23.83% THD on output voltage using the phase-disposition pulse width modulation (PD-PWM) technique. By using the hybrid PWM method (Hsin3w or Htrig3w) in the five-level inverter, the smallest THD is found with zero sequence sinewave shape of the modulating voltage compared to the phase opposition disposition (POD PWM) or alternative phase opposition disposition (APOD PWM) method [9]. The effect of the modulation index on THD of the five-level inverter is shown in [10]. The paper presented that voltage and current THD are 43.3% and 3.9% when the modulation index is 0.6. When the modulation index is 0.4, voltage and current THD are found 76% and 7% respectively. Besides, fuzzy logic is presented for controlling the PWM of the five-level inverter in the paper [11]. The inverter is powered with a single DC source and coupled inductors, where coupled inductors have a vital role in making five-level voltage. A five-level inverter using nine switches is presented in the paper [12], which a provides THD of 17%. This inverter's output frequency varies from 25 to 50 Hz, and it cannot be used for many applications.

Higher switching frequency causes higher loss due to changing of switching state a greater number of times [13], [14]. Rotor losses are analyzed of the PWM inverter by calculating finite elements in the paper [13]. The author proved that losses in the solid rotor core increased with decreasing switching frequency and suggested getting the optimum switching frequency to minimize losses. The relation between switching frequency and cable length was discussed in [15]. It mentioned that appropriately selected wave characteristics of the power cable and cable length may decrease the THD of voltage and current waveforms. The efficiency is investigated for a three-phase five-level inverter in the paper [16]. It showed that carrier disposition (CD) based inverter causes decreasing in inverter efficiency. Also, the inverter provides three voltage levels when the modulation index is less than 0.5. The inverter worked on five voltage levels when the modulation index is over 0.5, and provided high efficiency when the modulation index is over 1.15. Decreased THD factor is found in increased modulation index using lower than 400 Hz carrier frequencies [17]. But THD was not changed significantly when carrier frequencies were greater than 400 Hz.

Photovoltaic (PV) cells become more popular due to the rapid growth of energy demand. A multilevel inverter can be synchronized with a PV system to use high solar energy. Moreover, it has a positive effect on the environment. A separate DC source using a PV array is suitable for DC power supply to the multilevel inverter [18]. The maximum power point tracker (MPPT) is connected to with DC/DC converter in the PV system to obtain high power and increase the inverter's efficiency. A transformerless five-level single-phase inverter was presented in [19], which can provide at least 1.2 kW power. A single-phase five-level inverter with PV application was proposed in [20]. Though the designed inverter has reduced switch count, but it provides a high THD of 46.25%.

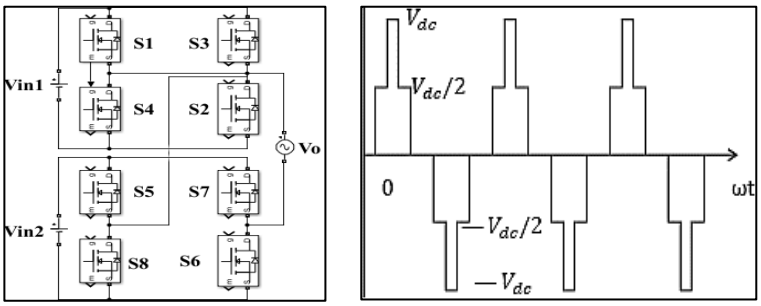
So, the discussion suggested that there is a lot of scope for research and develop multilevel inverters. In this paper, a cascaded H-bridge five-level inverter is designed with an LC filter circuit. This paper is divided into the following sections: proposed method is described in section 2; results and discussions are described in section 3; finally concluded in section 4.

2. METHOD

2.1. Cascaded H-bridge five-level inverter design

The proposed configuration of five level H-bridge inverter is shown in Figure 1. From Figure 1(a) represented switching combinitation with two separate DC sources and the output voltage (phase) waveform of the five-level inverter has been shown in Figure 1(b). The design is made with 8 switching devices for two single-phase full bridge inverters, where each bridge consists of 4 switching devices. There are 16 possible

inverter states for each full bridge, where 4 inverter states work for a fixed output voltage and bi-directional current flow. The designed inverter will provide five levels of AC output voltage, where each bridge provides three different voltage levels. The formula for calculating output voltage levels and voltage steps is 2n+1 and Vdc/n respectively, where n is denoted as the cascaded number of H-bridge required for designing five level inverter. Table 1 shows the switching states among the MOSFETs for making a five-level inverter. Switch S2, S4, S6, and S8 are turned OFF when the output voltage level is 0 (zero). Switch S1, S2, S6, and S8 are turned ON when the output voltage level is $V_{dc\,/2}$.



(a) (b)

Figure 1. Proposed five-level (a) H-bridge inverter and (b) voltage waveform, switch S1, S2, S5, and S6 are turned ON when the output voltage level isV_{dc}. Switch S3, S4, S6, and S8 are turned ON when the output voltage level is— $V_{dc/2}$. S3, S4, S7, and S8 are turned ON when the output voltage level is — V_{dc}

Table 1. Switching sequence

O/p Voltage	S1	S2	S3	S4	S5	S6	S7	S8
0	0	1	0	1	0	1	0	1
$V_{dc}/2$	1	1	0	0	0	1	0	1
V_{dc}	1	1	0	0	1	1	0	0
$-V_{dc}/2$	0	0	1	1	0	1	0	1
$-V_{dc}$	0	0	1	1	0	0	1	1

2.2. Inverter control design strategy

In the designed five-level inverter, PD-PWM technique is used to generate a pulse signal for each switch (S1 to S8), so that five-level voltage can be found. PD-PWM requires N number of identical triangular carriers which are displaced equally and compared with the reference signal to get the output phase voltage level. The PWM output will be high or low respective to the carrier signal being lower or higher than the reference signal. In the PD-PWM method, the carrier's phase in the zero-reference line is the same as the reference line [18]. In other words, the triangular carriers need to be arranged in the same phase and one over the other, so that they can be compared with reference wave and control the switching sequence operations for the multilevel inverter switches. PD-PWM technique assists to create the lowest THD in line-to-line voltage [21]. Besides, the PD-PWM method helps to decrease overall power rating, enhance control strategy for higher switching frequency and higher efficiency-based inverter, and it can be implemented in different conventional PWM techniques such as space vector pulse width modulation (SVPWM), and sinusoidal pulse width modulation (SPWM) [22]. The output arrangement of carrier waves and reference waves is illustrated in Figure 2 for the designed inverter. Here four carrier signal is used for two single-phase full-bridge inverters to modulate one reference signal.

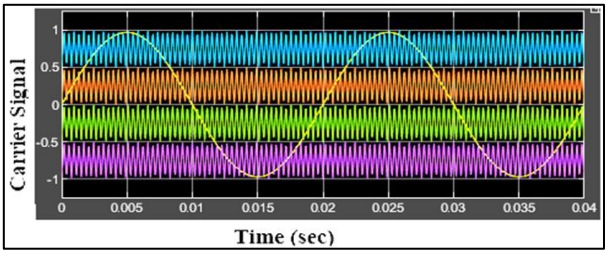


Figure 2. PD-PWM technique for carrier signals with the reference signal

2.3. LC filter circuit design

LC filter is made of two components: an inductor and a capacitor. Both of the components are known as energy storage components. The inductor is connected in series and the capacitor is connected in parallel to the load. In PPWM-based inverters, the LC filter effects significantly on inverter performance as it reduces the high-frequency distortion of output voltage. Besides, it can be used for controlling the switching current.

In this proposed LC design, IEEE. 519 standards are followed to get THD less than 5%. The inductance of the filter is found in (1) from the paper [23]. Acceptable peak-to-peak ripple current $\left(\Delta i_{\mathrm{Lpp|max|}}\right)$ is 20% of the rated current [24]. Modulation index (M) can be calculated using (2) from the paper [23], and the corresponding switching frequency is chosen at 2,750 Hz for the designed inverter to get optimum output. Sathik and Almakhles [25], the cutoff frequency ($\mathrm{f_c}$) is limited to 1/10 of the switching frequency (f_{sw}). Then the capacitor's value is obtained using (4) from the paper [7]. The calculated values (approximate) are shown in Figure 3.

$$L = \frac{\mathrm{V_{dc}}}{8\Delta i_{\mathrm{Lpp|max|\ \ desired\ f_{sw}}}} 0.5 < M < 1 \quad (1)$$

$$M = \frac{220\sqrt{2}}{V_{in}} \quad (2)$$

$$\mathrm{f_c} \leq \frac{\mathrm{f_{sw}}}{10} \quad (3)$$

$$C = \frac{1}{L\times(2\pi f_c)^2} \quad (4)$$

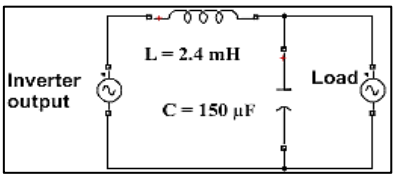


Figure 3. LC filter for the designed 5-level H-bridge inverter

3. RESULTS AND DISCUSSION

The simulation is completed using MATLAB/Simulink version R2021a. Assuming output PV groups i.e., DC sources are $\mathrm{V_{in1}} = \mathrm{V_{in2}}$=160 volts, which are used function proposed five-level inverter and its output performances. The simulation was performed with a load of series R-L branch (R=10 Ω and L=1 mH). Figure 4 depicts the output five-level voltage of the designed inverter without a filter. The designed inverter used both DC sources to get five levels according to the switching states presented in Table 1.

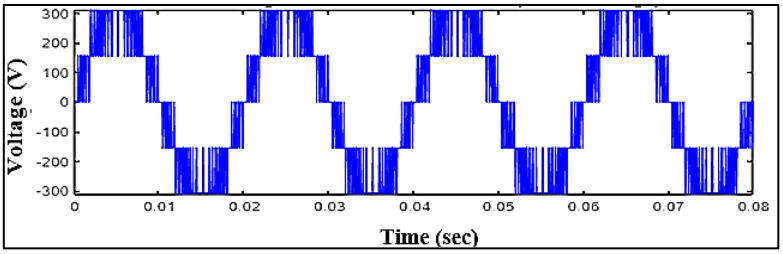


Figure 4. Inverter's output voltage wave without filtering

The output voltage waveform of an inverter without filtering is typically a square wave or a pulsed waveform. This means that the voltage changes abruptly between its maximum and minimum values, with no smooth transition in between. The frequency of the waveform is determined by the inverter's switching frequency and its output voltage can be adjusted by changing the duty cycle of the square wave. Without filtering, the output voltage waveform of an inverter is not suitable for most applications that require a stable and clean DC voltage. The square waveform contains high-frequency harmonics that can cause interference in sensitive electronic devices, such as radio receivers, and can also cause damage to motors and other electrical

devices. To overcome these problems, a low-pass filter is often used to smooth out the waveform and reduce the level of harmonics. The inverter output-rated voltage is found 221 volts, which is shown in Figure 4. Besides, Figure 5 depicts that the inverter' output voltage is 30.26%.

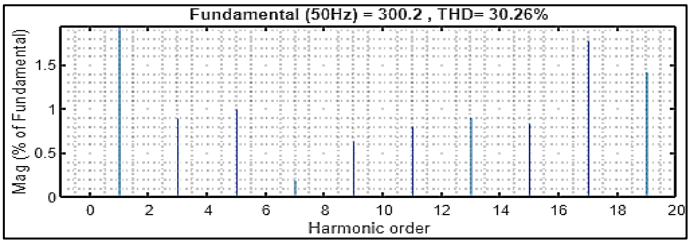


Figure 5. Inverter's output voltage THD without filtering

The output load current is 30.7 A, shown in Figure 6. The current wave is almost sinusoidal which is advantageous. Figure 7 depicts that inverter's output current THD is 11.12%, which is low compared to inverter's output voltage THD without using filter circuit.

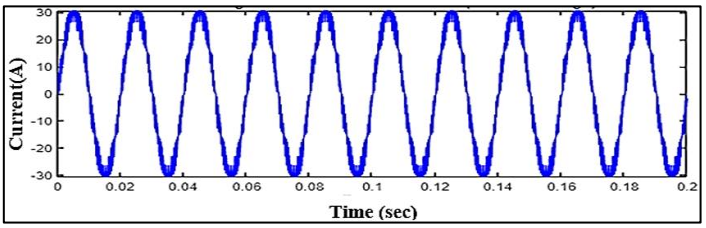


Figure 6. Inverter's output current wave without filtering

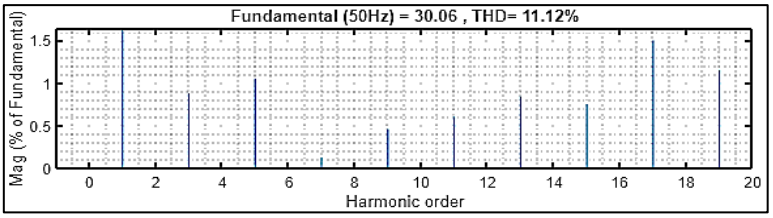


Figure 7. Inverter's output current THD without filtering

The designed five-level inverter is simulated again using an LC filter with the value of C=150 µF and L=2.4 µH. Figure 8 illustrates that the output voltage wave is sinusoidal and the output-rated voltage is 221.1 volts. The THD of the output voltage is 2.75%, shown in Figure 9.

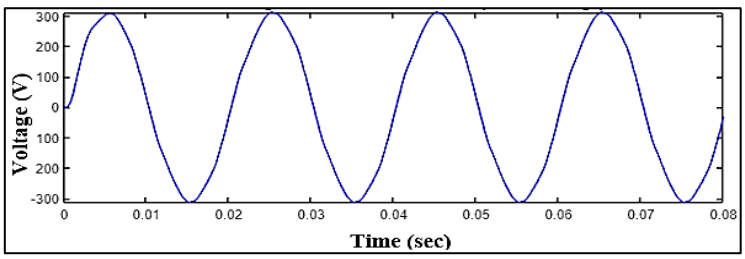


Figure 8. Inverter's output voltage wave after LC filtering

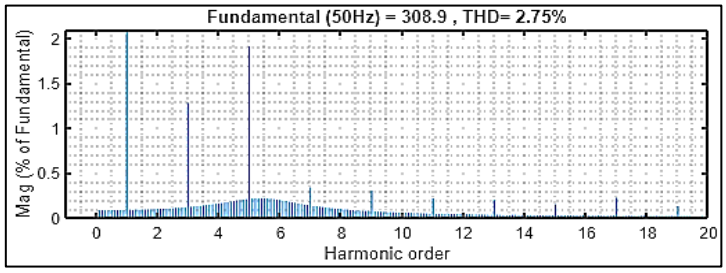


Figure 9. Inverter's output voltage THD after LC filtering

The output load current is found 31.2 A with LC filtering, shown in Figure 10, and its THD is 2.75%, shown in Figure 11. So, the inverter's output THD is compliant with IEEE 519 standards. The relationship between the modulation index has been illustrated in Figure 12. From Figure 12(a), it is clear that the THD of the output voltage is 2.75%, when the modulation index is 0.972. In this case, the output-rated rated voltage is 221.1 volts. In addition, from Figure 12(b) the simulated modulation index is found 0.8, the output-rated voltage is 183.8 volts and the THD is found 2.49%. Figure 13 illustrates the experimented relation between THD and the switching frequency of the designed five-level inverter. THD of the output voltage is increasing for both cases when the switching frequency is increased or decreased by 2,650 Hz as shown in Figure 13(a). A 10 Ω resistor and a 1 mH inductor are chosen as RL series branch to investigate output current for the designed inverter. Figure 13(b) illustrates the load stability investigation for the designed inverter.

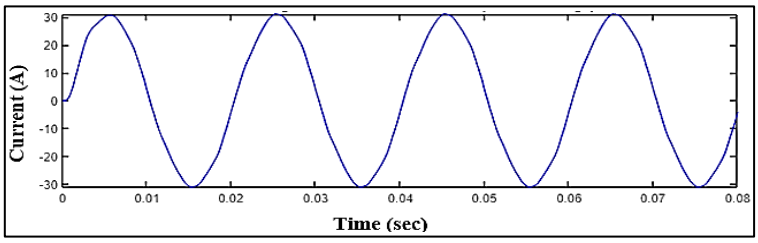


Figure 10. Inverter's output current wave after LC filtering

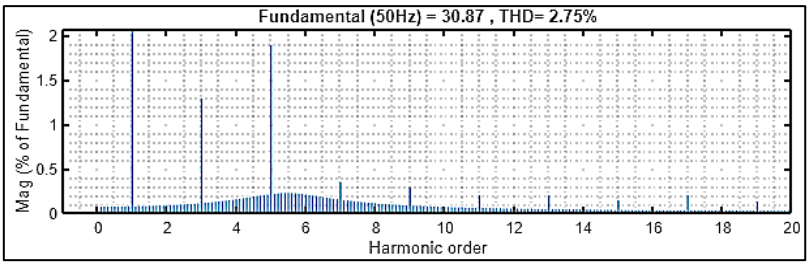
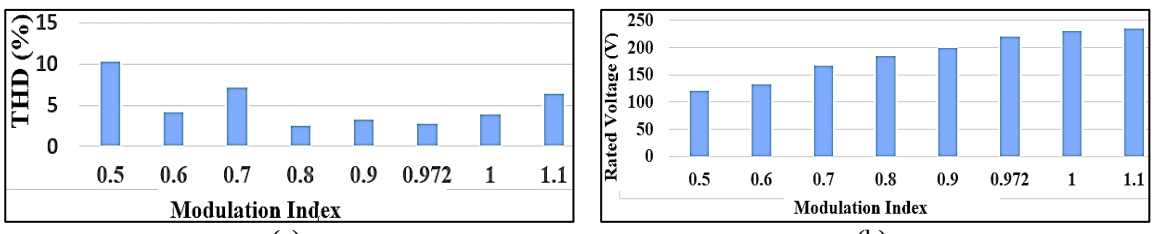
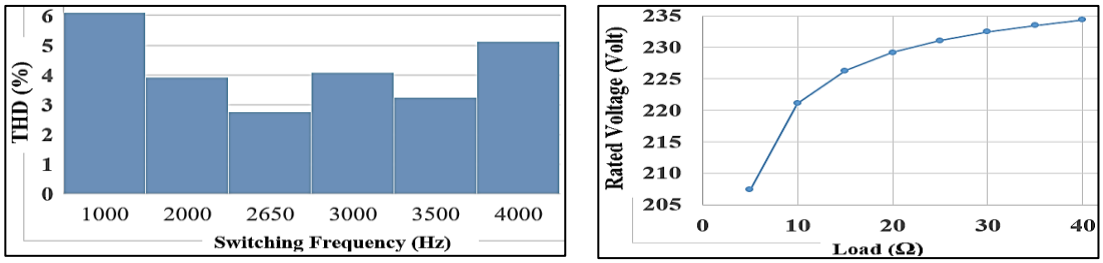


Figure 11. Inverter's output current THD after LC filtering



(a) (b)

Figure 12. Relationship between (a) modulation index vs THD and (b) modulation index vs rated voltage



(a) (b)

Figure 13. Relationship between (a) THD vs switching frequency and (b) rated voltage vs various load

For this test, the load resistance is changed from 5 to 40 Ω, and it is found 221.1 to 234.4 volts respectively. In general, it is important to match the rated voltage of a device to the voltage of the power source that it is connected to. Operating the device at a voltage that is too high or too low can result in reduced performance or damage to the device. For a resistive load, the rated voltage and the operating voltage should be the same. If the voltage is too high, the resistance of the load will cause an increase in current, which can result in overheating and damage to the device. Figure 14 shows that the proposed inverter's output voltage and output load current are at the same phase in the second simulation scenario, when the load is series RL branch of R=10 Ω and L=1 mH.

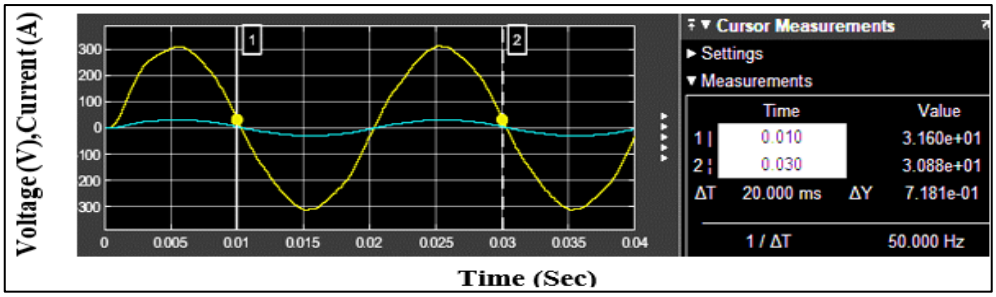


Figure 14. Phase of the output voltage and current of proposed 5-level inverter

It is clear from the figure that the inverter provides $\frac{1}{\Delta T}$= 50 Hz AC supply. The power factor is calculated as 0.99, and thus output power is found 6.9 kW. The summary of the proposed inverter is shown in Table 2.

Table 2. Summary of proposed five-level inverter

Parameters	Types
DC battery	160 volt×2
Filter capacitor, C_f	1 Pcs (150 µF)
Filter inductor, L_f	1 Pcs (2.4 mH)
Load resistance, R	10 Ω
Load inductance, L	1 mH
Switching frequency f_{sw}	2650 Hz
Output voltage, V_{out}	221.1 volt
Output current, I_{out}	31.2 A
Output power, P_{out}	6.9 kW

The entire design of the proposed 5-level H-bridge inverter is shown in Figure 15. This paper is only focused on a single-phase inverter. It will be developed in three phases with a grid connection. Besides, a photovoltaic (PV) cell will be designed to make two 160-volt batteries as input to the proposed inverter. The filter LC circuit will be redesigned to reduce capacitor size.

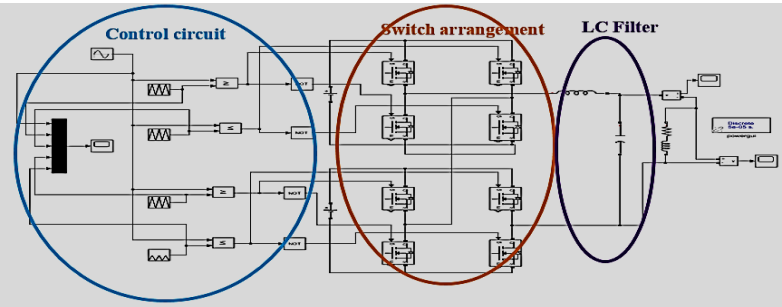


Figure 15. The entire design the of proposed 5-level inverter

3.1. Performance comparison and future trends

To check the performance of the proposed inverter, it is compared with some renowned papers. It is clear from Table 3 that the proposed filter-based inverter provides very low THD. The main cause of the low THD is the filtering circuit. The future trends are given: i) it will be developed by reducing switches, and prototype testing; ii) switching loss calculation will be investigated; and iii) other controlling methods will be investigated so that the performance of PD-PWM can be compared.

Table 3. Performance comparison with some recent literature

Ref/Year	6/2021		10/2021		24/2020		26/2022		Proposed	
THD (%)	V_{THD} = 17.63	I_{THD} = 17.62	V_{THD} = 26.2	I_{THD} = 2.5	V_{THD} = 21.1	I_{THD} = 21.2	V_{THD} = 34.64	I_{THD} = 2.19	V_{THD} = 2.75	I_{THD} = 2.75

4. CONCLUSION

A single-phase CHB five-level inverter has been developed using the PD-PWM method. Before filtering, it is found 30.26% and 11.12% THD of output voltage and current accordingly. The LC (L=2.4 mH and C=150 µF) filtering circuit is used to minimize THD of voltage and current waveforms. It is found 2.75 % THD for both the voltage and current output. The relationship between modulation index and THD, and modulation index and rated voltage are analyzed. It is clear that the inverter provides 2.75% THD when the modulation index is 0.972, and the rated voltage is 220 volts with a 50 Hz AC supply. The optimum switching frequency is found at 2,650 Hz by investigating it with THD and rated voltage. A load of series RL branch of R=10 Ω and L=1 mH are used to investigate its supply energy 6.9 kW. The system stability is checked out by using various loads between 5 to 40 Ω, and it is clear that the rated voltage does not change significantly.

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