From Ferroelectric Material Optimization to Neuromorphic Devices

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Abstract

Due to the voltage driven switching at low voltages combined with nonvolatility of the achieved polarization state, ferroelectric materials have a unique potential for low power nonvolatile electronic devices. The competitivity of such devices is hindered by compatibility issues of well-known ferroelectrics with established semiconductor technology. The discovery of ferroelectricity in hafnium oxide changed this situation. The natural application of nonvolatile devices is as a memory cell. Nonvolatile memory devices also built the basis for other applications like in-memory or neuromorphic computing. Three different basic ferroelectric devices can be constructed: ferroelectric capacitors, ferroelectric field effect transistors and ferroelectric tunneling junctions. In this article first the material science of the ferroelectricity in hafnium oxide will be summarized with a special focus on tailoring the switching characteristics towards different applications.The current status of nonvolatile ferroelectric memories then lays the ground for looking into applications like in-memory computing. Finally, a special focus will be given to showcase how the basic building blocks of spiking neural networks, the neuron and the synapse, can be realized and how they can be combined to realize neuromorphic computing systems. A summary, comparison with other technologies like resistive switching devices and an outlook completes the paper.

1 Introduction

Semiconductor memories are an important ingredient for information systems.[1] Classically, the random access memory, that is directly interacting with the processing unit, was the domain of semiconductor memories, while magnetic and optical systems were used for nonvolatile storage of large amounts of data. For very fast access speed static random access memories (SRAMs) are used, while for higher density dynamic random access memories (DRAMs) offer a lower cost solution and can still provide very fast random access. With the success of Flash memories and in particular NAND Flash, semiconductor memories have also entered the field of nonvolatile storage. Classically all semiconductor memories were based on charge storage. In SRAM a positive feedback keeps the internal nodes charged or discharged, in DRAM the charge on a capacitor is used to represent the information and in Flash memory either a floating gate or a charge trapping layer is introduced into the gate stack of a metal oxide semiconductor field effect transistor (MOSFET) to store charge that can modify the threshold voltage of the device. However, charge storage has some severe shortcomings. Due to the voltage–time dilemma,[2] nonvolatility, and fast random access cannot be reached at the same time and high voltages in the order of 10–20 V are required to write and erase charge based nonvolatile memory cells. Finally, scaling down of such devices has reached its limits. Therefore, since many years, concepts based on using an alterable material property like the remanent polarization of a ferroelectric,[3, 4] the magnetization

direction of a ferromagnetic material,[5] the phase of a chalcogenide[6, 7] or the conductance of certain materials modulated by forming conductive channels, switching the barrier height at an electrode or other mechanisms[8, 9] have become the focus of intense research and development activities. Among these switching mechanisms, ferroelectric switching has the advantage of being a purely field driven mechanism that can be activated at reasonably low voltages and, therefore, has the unique property of combining very low write power consumption with nonvolatility. Already in the 1950s the first attempts to realize a ferroelectric memory have been undertaken.[10] When silicon-based integrated circuit technology became available, such devices were integrated into semiconductor technology and this lead to the first commercial devices.[11] However, although it was possible to integrate materials like lead–zirconium titanate (PZT) or strontium–bismuth tantalate (SBT) into a metal-oxide semiconductor (MOS) technology, the complexity of these materials hindered scaling at the pace of competing devices and the interest of industry rapidly declined. The first reports on ferroelectricity in hafnium oxide immediately revived the interest in ferroelectric memory devices, since hafnium oxide has been used in complementary metal oxide semiconductor (CMOS) processes since 2007[12] and, therefore, it was clear that this material will solve the integration challenge. Since then, research on all three basic memory devices possible with ferroelectric materials, namely capacitor based ferroelectric random access memories (FeRAM), ferroelectric field effect transistors (FeFET), and ferroelectric tunneling junctions (FTJ) has gained more and more critical mass. At the same time, it became clear that the traditional von-Neumann architecture of computing devices has reached its limits. Concepts were the data storage and the computing are no longer separated have received more and more interest. Among them, approaches, that mimic the human brain promise to solve tasks related to recognizing complex patterns in large amounts of data are extremely promising. In the most simple approach, input nodes are connected to output nodes via several hidden layers of nodes (see **Figure** 1a). Such a neural network, called an artificial neural network (ANN) in the following, is widely used and often implemented in software and run on a conventional von-Neumann computer. This solution is very power hungry and specialized hardware accelerators are being developed that can perform the task more efficiently. Performing the necessary vector-matrix multiplications directly in the memory taking advantage of Ohm's Law and Kirchhoff's Law is particular interesting, since this approach can overcome the limitations of the von-Neumann bottleneck.[13, 14] A spiking neural network (SNN) as illustrated in Figure 1b is going one step further on the path toward a network that is inspired by the brain. Here neurons and synapses, as found in the brain, are mimicked. Since the neurons only produce spikes at certain events, such SNNs have the potential to further reduce the power consumption of the neural network. In the following, we will show how ferroelectric materials can help to realize both ANNs and SNNs. As a starting point, we will look at the material and its optimization itself. Then we will discuss ferroelectric nonvolatile memory cells, which are the basis for realizing specific circuit elements that can be used in neural networks. Finally we will discuss concepts and the state of the art in realizing functions for brain inspired computing using ferroelectric devices.

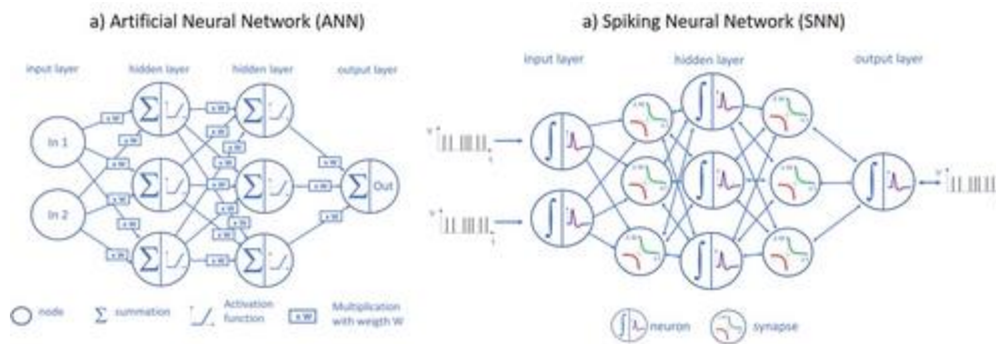

Figure 1

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Simplified schematic of a) an artificial neural network and b) a spiking neural network.

2 Ferroelectric Materials

History of Research on Ferroelectric Materials

The concept of ferroelectricity with two spontaneous polarization states P_s was first suggested in 1912 by Schroedinger introducing the German term “ferroelektrisch.”[15] It was first experimentally demonstrated in Rochelle salt not earlier than 1920 by Valasek.[16] During the first decade after its discovery, there have been extensive studies to understand the ferroelectricity in Rochelle salt, but the ferroelectric properties of Rochelle salt were strongly influenced by environmental conditions including humidity. The second ferroelectric material discovered by Busch et al.[17] was KH_2PO_4 with better chemical stability, and it was followed by the discovery of ferroelectric crystals with similar structure such as KH_2AsO_4, $NH_4H_2PO_4$, and $NH_4H_2AsO_4$. However, these materials still have a Curie temperature lower than room temperature, so they were not suitable for practical applications.

A material's breakthrough for the practical applications of ferroelectricity was the discovery of $BaTiO_3$ having the perovskite structure during World War II. $BaTiO_3$ soon became an important ferroelectric material for applications utilizing high permittivity (even higher than 1000) or piezoelectricity.[18, 19] Today, $BaTiO_3$ is still an important dielectric materials used in multi layered ceramic capacitors. The perovskite-structured ferroelectrics have a chemical formula of ABO_3, where A and B are different cations. Below Curie temperature, the B-site cations have two stable locations deviating from the center of the unit cell along the *c*-axis of the tetragonal phase resulting in two polarization states P_s. The discovery of $BaTiO_3$ was followed by the development of a phenomenological theory to describe ferroelectricity by Landau, Ginzburg, and Devonshire,[20-22] and by the discovery of numerous perovskite-structured ferroelectrics.

$Pb(Zr, Ti)O_3$ (PZT) was the most important perovskite-structure ferroelectric discovered at that time with its high Curie temperature (~400°C), and high remanent polarization (P_r = 10–40 μC cm^{-2} in thin films), as well as a high piezoelectric coefficient.[23, 24] Despite the environmental issue related to Pb, PZT is still an industrially important material. Moreover, it should be noted that compositions at the morphotropic phase boundary (MPB) have been intensively studied for PZT, and it triggered research on improving properties of various ferroelectric materials. Another important Pb-containing material is

with its typical relaxor behavior and resulting strong piezoelectricity.[25, 26]

Ferroelectric materials with two P_s states have been considered theoretically ideal for nonvolatile memories, and the concept of ferroelectric random-access-memory (FeRAM) was first suggested by Buck in 1952,[10] and could be commercialized in the 1990s.[11, 27] Searching for ferroelectric materials suitable for the semiconductor devices has been the key task in research on FeRAMs. **Table** 1 summarizes the properties of conventional ferroelectric materials such as PZT and $SrBi_2Ta_2O_9$ (SBT) as well as emerging ferroelectric materials such as doped HfO_2 and (Al,Sc)N.

Table 1. Summary of frequently observed material properties of Pb(Zr, Ti)O_3, $SrBi_2Ta_2O_9$, doped HfO_2, and (Al, Sc)N[28]

Parameters	Pb(Zr, Ti)O_3	$SrBi_2Ta_2O_9$	Doped HfO_2	(Al, Sc)N
P_r [µC cm^{-2}]	10–40	5–10	10–40	80–110
E_c [kV cm^{-1}]	50–70	30–50	800–2000	2000–5000
k	400	200	30	25
Min. thickness in solid state device	50	–	Lower than 5	Lower than 10

For FeRAMs, the perovskite-structured PZT thin film was extensively studied, but it suffered from a limited switching endurance.[29] and a pronounced sensitivity toward reducing gases like H_2.[30] The endurance could be improved by adopting new electrode materials such as Ir, IrO_2, RuO_2, and $SrRuO_3$, which are hard to be integrated into the CMOS technology.[29, 31, 32] The Aurivillius class of ferroelectrics such as SBT attracted interest at that time due to their higher switching endurance achievable on Pt electrodes,[29] but with the ferroelectric materials available at that time, the advance of FeRAM was halted at the 130 nm technology node due to the incompatibility of the materials with CMOS processing[33] and the inability to achieve high polarization values in 3D structures.[34] Instead, other emerging devices such as resistive switching RAM, magnetic RAM, and phase change RAM have attracted stronger interest than FeRAMs in the first decade of the 21st century. However, the situation abruptly changed after the discovery of ferroelectricity in fluorite-structured HfO_2-based ultra-thin films,[35, 36] which will be discussed in detail in the next chapter. Moreover, other binary an ternary ferroelectric materials such as Mg:ZnO and (Al,Sc)N are also attracting increasing interest.[37, 38] Especially, (Al,Sc)N can have a high bandgap and E_c with rather low dielectric constant k, and can reach a P_r as high as 80–110 µC cm^{-2}.[37]

Besides the inorganic ferroelectrics described above, organic ferroelectric materials have also been extensively studied especially for applications in flexible electronics.[39, 40] The most extensively studied organic ferroelectric material is poly(vinylidene fluoride trifluoroethylene) (PVDF-TrFE) and variations of this system. These organic ferroelectric materials have not just been studied for nonvolatile memory applications,[41] but also applications in neuromorphic computing have been persued, as recently reviewed by Li and coworkers.[40] 2D Van der Waals materials like In_2Se_3[42] or $CuInP_2S_6$ (CIPS)[43] can also be interesting candidates especially in the case when 2D materials should unfold their potential for future electronic devices.

Discovery of Ferroelectricity in Hafnia-Based Thin Films

The ferroelectricity in HfO_2-based thin films was discovered in 2006 by Boescke et al. at the semiconductor manufacturer Qimonda, and was first reported in 2011.[35] **Figure** 2a,b show the crystallographic structure of the ferroelectric orthorhombic phase (space group: $Pca2_1$) and the first reported polarization–electric field (P–E) curve of a Si: HfO_2 thin film.[35] This

pioneering work was followed by numerous reports on HfO_2 doped with various dopants such as Zr, Y, Gd, Sr, and La within a few years.[44-48] Different from the perovskite-structured ferroelectrics with polarization switching by the displacement of B-site cations as well as the distortion of oxygen octahedra, the polarization switching in HfO_2-based ferroelectrics occurs by a displacement of four among the eight oxygen anions in the unit cell.[35] The theoretical P_s value is 50–55 μC cm^{-2} according to the previous simulation work, and P_r values of 10–40 μC cm^{-2} have been frequently reported from experiments.[36, 49] The coercive field E_c which is required for the polarization switching is generally 0.8–2.0 MV cm^{-1}. It is affected by dopant species as well as external factors such as interfacial layers and electrode materials.[36, 49] The high E_c of these fluorite-structured ferroelectrics enabled to induce sufficient memory window (in the range of 1 V) in ferroelectric field effect transistors (FeFETs) even with a thickness below 10 nm. This is different from the perovskite-structured ferroelectric thin films having an E_c in the range of 0.1 MV cm^{-1} or even below.[28, 36, 49-52] The eye-catching advantage of fluorite-structured ferroelectrics is its compatibility with CMOS technology using established deposition techniques like ALD.[28, 36, 49-53] It should be noted that HfO_2 is a current gate insulator used in MOSFETs and ZrO_2 is the most common cell capacitor dielectric in DRAMs.[28, 36, 49-52] Only by minute doping and subsequent annealing, nonvolatility can be additionally induced by the formation of a ferroelectric crystallographic phase, which was a surprisingly promising news for ferroelectric memories. This can become a potential game changer in semiconductor industry based on another material's breakthrough similar to the breakthrough of the amorphous HfO_2 phase previously replacing SiO_2 as the gate insulator in MOS transistors.

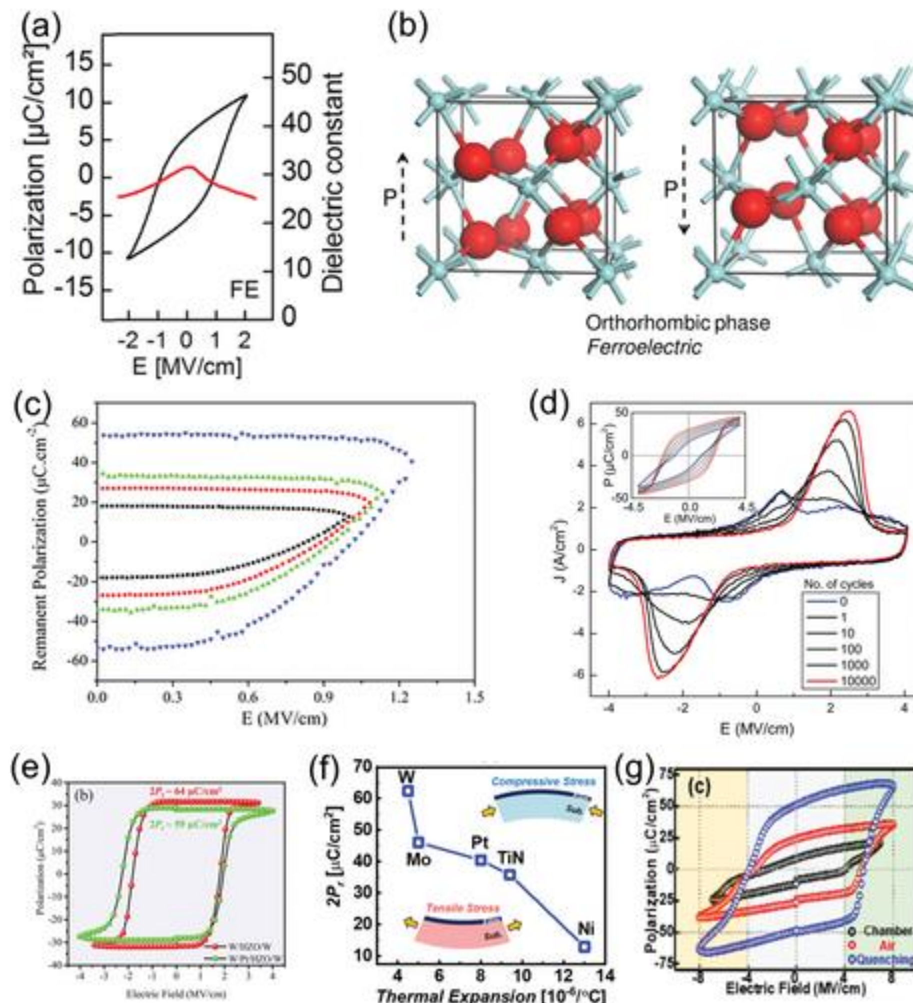

Figure 2

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The first reported a) polarization-electric field (*P–E*, black curve, left *y*-axis) and b) dielectric constant-electric field (red curve, right *y*-axis) curves for ferroelectric and the schematic unit cell structure of Si: HfO_2 thin films. Reproduced with permission.[35] Copyright 2011, American Institute of Physics. c) *P–E* curves of a capacitor containing a film. Reproduced with permission.[56] Copyright 2021, American Institute of Physics. d) *J–E* and *P–E* (inset) curves of a TaN/Gd: HfO_2/TaN capacitor after different numbers of cycles. Reproduced with permission.[58] Copyright 2015, American Institute of Physics. e) *P–E* curves of a W/$Hf_{0.5}Zr_{0.5}O_2$/W and a W/Pt/$Hf_{0.5}Zr_{0.5}O_2$/W capacitor. Reproduced with permission.[59] Copyright 2011, American Chemical Society. f) $2P_r$ of $Hf_{0.5}Zr_{0.5}O_2$ thin films as a function of the thermal expansion coefficient of the applied metal electrodes. Reproduced with permission.[61] Copyright 2020, American Institute of Physics. g) *P–E* curves of capacitors containing $Hf_{0.5}Zr_{0.5}O_2$ thin films after chamber cooling (slow cooling rate), air cooling (medium cooling rate), and quenching (fast cooling rate). Reproduced with permission.[62] Copyright 2020, IEEE.

3 Optimization of Hafnia-Based Ferroelectric Thin Films

The ferroelectric properties in HfO_2 thin film doped with various dopants are promising for nanoelectronic devices since this material system enables much better dimensional scaling compared to perovskite ferroelectrics. Moreover, they are much easier to integrate into CMOS. However, to meet all the requirements for the different device concepts including reliability, there are still open material issues which require urgent solutions. Even more, achieving properties suitable for neuromorphic computing still has barriers that need to be overcome. It should be noted that solid-state-devices with ferroelectric films having a thickness below 10 nm could not be extensively studied before ferroelectric HfO_2 became available. There have been important signs of progress for improving the material properties of HfO_2-based ferroelectrics for different applications. These are reviewed in this chapter.

P_r is an important parameter which reflects the quantity of charged stored in the ferroelectric capacitor structure. Therefore, having a high P_r value is important for 1 transistor–1 capacitor FeRAMs. In ferroelectric field-effect-transistor (FeFET), in contrast, a too high P_r can cause a high depolarization field E_{dep} and a high concentration of trapped charges, which would deteriorate the device reliability.[54, 55] There have been efforts from numerous researchers to induce high P_r in fluorite-structured ferroelectrics. P_r is strongly affected by the dopant species and some dopants seem to be more favorable to produce high P_r values. One typical example is La with which P_r values even above 40 μC cm^{-2} have been reported.[44] However, similar high values have not been reproduced by other research groups so far. Luo et al.[56] reported P_r values up to 53 μC cm^{-2} in

thin films as shown in Figure 2c. But in there work the high leakage current could have affected the measured P_r value although the leakage current contribution was minimized using the PUND measurement technique.[57] The other important factor is the electrode material, which can affect the crystallographic structure and resulting ferroelectricity of HfO_2-based ferroelectrics. Hoffmann et al.[58] reported that a P_r of up to 35 μC cm^{-2} could be achieved in $Hf_{0.5}Zr_{0.5}O_2$ with a TaN electrode (see Figure 2d) and suggested that oxygen vacancy formation due to the TaN electrode might be the reason. Kashir et al.[59] reported that a P_r of up to 32 μC cm^{-2} could be achieved in $Hf_{0.5}Zr_{0.5}O_2$ with W electrodes (see Figure 2e). In these samples the wake-up effect was additionally mitigated. Kim et al.[60] suggested that

the tensile stress induced by the top electrode would affect the P_r value of $Hf_{0.5}Zr_{0.5}O_2$ thin films. In their work, the highest P_r of 24 μC cm^{-2} could be achieved with the highest thickness of the top TiN electrode of 180 nm. For this thickness the highest tensile strain was observed by X-ray diffraction. Goh et al.[61] reported that the P_r value of their $Hf_{0.5}Zr_{0.5}O_2$ thin films was strongly correlated to the thermal expansion coefficient of the bottom electrode materials, implying that the thermal stress affects the ferroelectricity. Among the examined W, Mo, Pt, TiN, and Ni electrodes, the highest P_r of 31.2 μC cm^{-2} was achieved for W electrodes for which the coefficient of the thermal expansion was the lowest as shown in Figure 2f. Ku et al.[62] showed that the P_r value of their $Hf_{0.5}Zr_{0.5}O_2$ thin film could be strongly enhanced by increasing the cooling rate of the rapid thermal annealing process. In their work, a P_r of up to 50 μC cm^{-2} could be achieved in $Hf_{0.5}Zr_{0.5}O_2$ thin films directly grown on a Si substrate as shown in Figure 2g.[62]

The coercive field E_c is one of the most important material parameters of a ferroelectric. On one hand, achieving sufficient E_c is important to have a large enough memory window for a practical FeFET device. On the other hand, a too high E_c value and its wide distribution increases the electric field required for the saturated polarization switching, and deteriorates the switching endurance. Thus, the high E_c of fluorite-structured ferroelectrics is called a "double edged sword." The general E_c values are 0.8–2.0 MV cm^{-1} and are strongly dependent on the dopant species. It is known that larger dopants generally increase the E_c value although the origin of this influence is not clearly understood yet.[49]

Polarization switching speed is also highly important, especially in order to achieve high speed memory devices. There have been numerous research activities to understand the polarization switching kinetics of HfO_2-based ferroelectrics. Kim et al. studied the polarization switching kinetics of

thin films under various electric field strengths and different temperatures as shown in **Figure** 3a.[63] From the observed domain wall velocity measured using PFM under various electric field strengths, the activation field could be calculated as shown in Figure 3b. The activation field, which is strongly related to the field required for the domain wall propagation, was reported to be 9.3 MV cm^{-1}. This value is several times higher than typical values for perovskite-structured ferroelectrics.[63] Owing to the existence of energy barriers and pinning sites for the domain wall propagation, the speed of domain wall propagation was reported to be lower compared to that of conventional ferroelectric materials based on a piezoresponse force microscopy (PFM) study.[64] The maximum velocity of domain walls (0.16 m s^{-1} as shown in Figure 3c) observed in that study was lower than that of PZT thin films.[64] The overall polarization switching occurs with nucleation and growth of oppositely polarized domains, and the switching kinetics have been an important classical research topic of ferroelectric materials. In Figure 3d an example is shown were data measured using PFM is compared to the nucleation limited switching (NLS) and the Avrami–Ishibashi (KAI) models. To date, the nucleation limited switching (NLS) model and the inhomogeneous field model (IFM) model are generally accepted to describe the polarization switching in polycrystalline HfO_2-based ferroelectrics.[64-66] In the NLS model, the distribution in the nucleation time originating from various factors are considered by adopting a Lorentzian distribution function. In the IFM the distribution of the local electric field is considered as an origin of the rather wide distribution of switching time as shown in Figure 3e.[67] In HfO_2-based thin films, there are numerous potential causes of the distribution in switching time such as grain boundaries, residual impurities, and oxygen vacancies. Therefore, it is reasonable to accept that the polarization switching could be well described by the NLS

model or IFM. In a nanoscale electronic device, in which only a few grains are included in the ferroelectric layer, stepwise polarization switching could be observed as shown in figure 2f.[68] This is associated with an accumulative switching effect[69] which was suggested to be applicable to artificial neurons for spiking neural networks.[70]

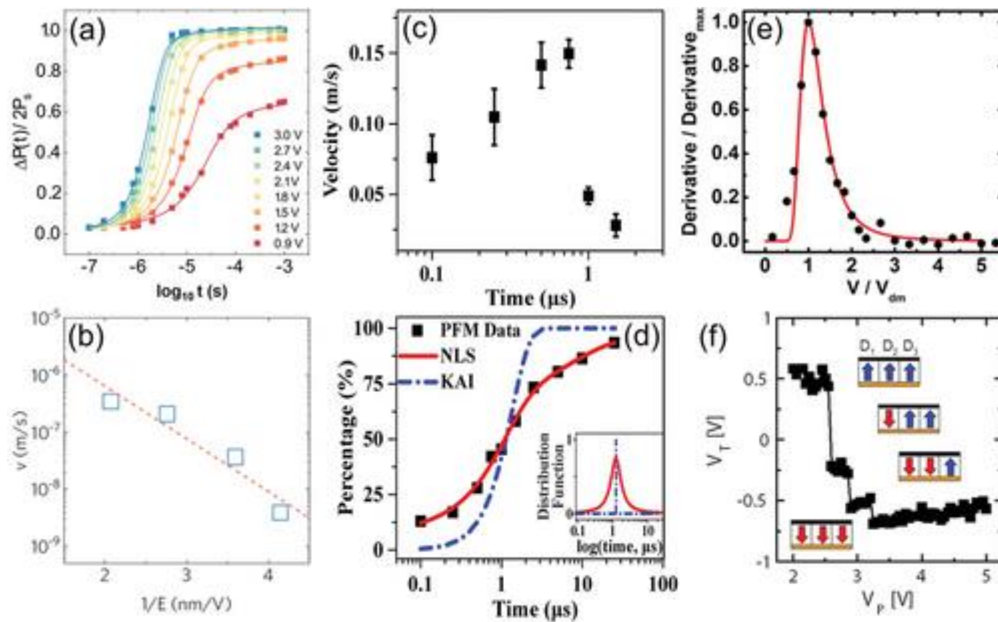

Figure 3

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a) Time and voltage dependence of the switched polarization *P*(*t*) measured at room temperature. The solid lines represent the fitting results using the NLS model considering the Lorentzian distribution of the characteristic switching time for ferroelectric nucleation. b) Domain wall velocity versus the inverse electric field for the 8 nm-thick Si: HfO_2 thin film. (a,b) Reproduced with permission.[63] Copyright 2019, American Chemical Society. c) Domain wall velocity as a function of time obtained from piezoresponse force microscopy (PFM) studies. d) Fitting of the PFM switching data by the KAI and NLS models. The inset shows the distribution functions for the corresponding models. (c,d) Reproduced with permission.[64] Copyright 2018, American Institute of Physics. e) Normalized derivative of polarization reversal as a function of normalized voltage and fitted curve based on the IFM model (red line). Reproduced with permission.[67] Copyright 2018, American Chemical Society. f) Threshold voltage after programming versus the corresponding programming voltage V_P. Three discrete and abrupt V_T shifts corresponding to separate switching of three domains within the stack (inset) can be observed. Reproduced with permission.[68] Copyright 2017, American Chemical Society.

For the practical application of a nonvolatile memory cell, reliability is a very critical issue. Although the term reliability itself is more related to the device performance, it also plays a key role in the material engineering of HfO_2-based ferroelectrics. [71] Here, we will discuss retention, endurance, and imprint of simple capacitors with HfO_2-based ferroelectrics. Retention has been a critical issue in FeFETs because rather high depolarization fields E_{dep} can originate from the physical distance between the polarization of the ferroelectrics and the corresponding compensating charges in the semiconductor. The retention issues of polarization in metal/ferroelectric/metal capacitors are not as severe as those in the metal/ferroelectric/insulator/semiconductor stack, which is the core gate stack of FeFETs. Especially on Si, the unavoidable formation of a low-*k* SiO_2 interface layer is a critical source

of a high E_{dep}. Because of the high E_c and rather low k value of HfO_2-based ferroelectrics, the E_{dep}/E_c ratio within general dimensions of SiO_2 IL for HfO_2-based ferroelectrics is much lower than the one in PZT and SBT, suggesting that adopting HfO_2 gate ferroelectric can significantly enhance the retention of FeFETs.[50, 54]

However, in ferroelectrics specifically the opposite state retention is more critical than the classical retention caused by the depolarization field or thermal depolarization. The opposite state retention is a consequence of the imprint effect. When a ferroelectric capacitor is stored in a given polarization state, the hysteresis shifts in a way to stabilize the state the capacitor is stored in. As a consequence, the E_c to reach the opposite state becomes larger. After the switching to that state the polarization will be reduced. This has been a critical issue also for perovskite based ferroelectric memories and like for the field cycling endurance, oxygen electrodes helped to strongly reduce this effect. The effect is attributed to charge injection into dead layers at the electrode/ferroelectric interface. Since in hafnium oxide based ferroelectrics the fields are considerable higher, also the fields across tiny dead layers are increased making imprint and opposite state retention a major issue that needs to be resolved.[72, 73]

Another major reliability issue is the limited number of endurable cycles for HfO_2-based ferroelectrics. In the initial stage of FeFETs with HfO_2-based ferroelectrics, the endurable program/erase number was limited below 10^6 cycles.[50, 55] Such low endurance could be attributed to charge trapping and interfacial trap generation.[50, 55] The issues is that the *k* value of the SiO_2 IL is only 1/7–1/8 of that of HfO_2-based ferroelectrics. Thus, when E_c of 1 MV cm^{-1} is applied across a HfO_2 -based ferroelectric, roughly 7–8 MV cm^{-1} of electric field is applied across the SiO_2 IL. This high field causes injection of charge carriers through the SiO_2 IL.[50, 55] Thus, several attempts have been made to resolve this issue. The insertion of high-*k* materials instead of SiO_2 IL is one of the most successful solutions without changing the channel material. Ali et al.[74] reported that inserting a

IL could effectively increase the endurance of FeFETs up to 10^6 cycles. Tan et al.[75] reported that 10^{10} endurance cycles could be achieved by inserting a IL between the ferroelectric HZO film and the Si substrate. Kim et al.[76] reported that the endurance of a Mo/HZO/Si capacitor could be increased beyond 10^9 switching cycles by forming a TiO_2 IL on the

/Si substrate.

The last issue to be discussed in this chapter is the spatial uniformity. In modern ultra large scale integration, it is highly important to decrease the device-to-device-variation. From a viewpoint of material science, it can be achieved by the deposition of films with narrow distribution of material properties. However, it is highly challenging in HfO_2-based ferroelectrics grown by atomic layer deposition. Generally, in the as-deposited state, the amorphous phase is formed, and subsequent annealing (generally by a rapid thermal process) is required to crystallize the material into the ferroelectric orthorhombic phase. Afterward the annealed film is polycrystalline with almost random orientations, and frequently several different crystallographic phases coexist. It has been suggested that the fraction of the nonferroelectric phase could be decreased by an optimized annealing processes and optimized electrode materials.

However, currently there is no clear solution for depositing films with a strong preferred orientation by ALD. Shenk et al.[77, 78] reported that the 10 nm-thick

and

could have a weak (111) and (002) preferred orientation on TiN bottom electrodes, but the magnitude of the preferred orientation was very low. Park et al.[79] deposited (111)-oriented HZO film on Pt bottom electrode, but the P_r was negligible despite the fact that a composition of Hf:Zr of 50:50 was used. This is generally known as the optimum condition. Recently, there have been interesting reports on the preferred orientation in sub 3 nm ferroelectric HfO_2 films.[80] Kim et al.[80] reported that (112) orientation is dominantly formed within their 2 nm-thick HZO films. However, the polycrystalline films with a strong preferred orientation is limited only to sub-3-nm thickness directly grown on a Si substrate. There is no clear solution to induce strong preferred orientation in HfO_2-based films with higher thickness on bottom electrodes other than Si, requiring urgent solutions for practical applications.

4 Ferroelectric Devices and Their Application in Memories

The remnant ferroelectric polarization reversal can be used to store information in a non-volatile manner. Thereby, the write operation which is basically common to all the different ferroelectric device flavors is always performed by applying an electric field that exceeds the E_c of the ferroelectric layer with typical values of 0.8-2.0 MV cm^{-1} in the case of ferroelectric hafnium oxide. Depending on the device sizes and material stack configurations a rich variety of switching dynamics including single domain and accumulative switching, gradual switching with many intermediate states, or just digital switching between two distinct polarization states, can be observed (see **Figure** 4). Only the current flow resulting from the displacement of the dipoles is necessary to switch the polarization. Since the ferroelectric is switched between the positive and negative polarization state, the maximum write energy that is required for complete polarization reversal can be estimated simply from the product of the write voltage and the polarization charge: V_{write}*P_r. Typical values of write voltages and polarization charge for 10 nm thick ferroelectric HfO_2 films are in the range of 1-2V and 20–30 μC cm^{-2}. Thus, the write energy per area is about 50 μJ cm^{-2}. Depending on the device size, write energies in the range of just 1-100 fJ are required and the write operation is very energy efficient. However, the main differentiator between the device concepts is the read operation. In general, the ferroelectric polarization causes the formation of a remnant electric field within layer stacks that might be composed from different materials including semiconductor channels or electrodes, metal electrodes and additional dielectric layers. Moreover, the change in ferroelectric polarization causes an electric switching current. The read operation in the different devices can be performed by directly sensing the difference between the charge flowing during polarization switching and the capacitive displacement charge without switching. This is done in the conventional FeRAM concept using just a ferroelectric capacitor. Alternatively an indirect and non-destructive read operation by sensing the impact of the polarization field on the conductance of either a semiconducting channel as is used in a ferroelectric field effect transistor (FeFET) or the polarization dependent tunneling current through a ferroelectric material stack as is done in the ferroelectric tunneling junction (FTJ) can be applied. Hence, basically three different devices concepts are nowadays under investigation. Obviously, the different sensing schemes cause different boundary conditions for the device design and their application in electronic circuits as is depicted in **Figure** 5. While the FeFET appears to be the most flexible device featuring very rich dynamics and thus is used in pure memory arrays as well as in more unconventional

applications such as synapse or neuron circuits, the FeCAP device seems to be most suitable just for memory application due to its destructive readout operation. The FTJ due to its very low read currents might fit best into beyond-von-Neumann architectures targeting at data-centric massive parallel computations. Thus, in the following subsections we will first discuss the three memory devices in more detail with respect to their suitability for memory applications. Thereafter, in Section 5 we will shed more light on their specific dynamic features which are interesting for neuromorphic applications.

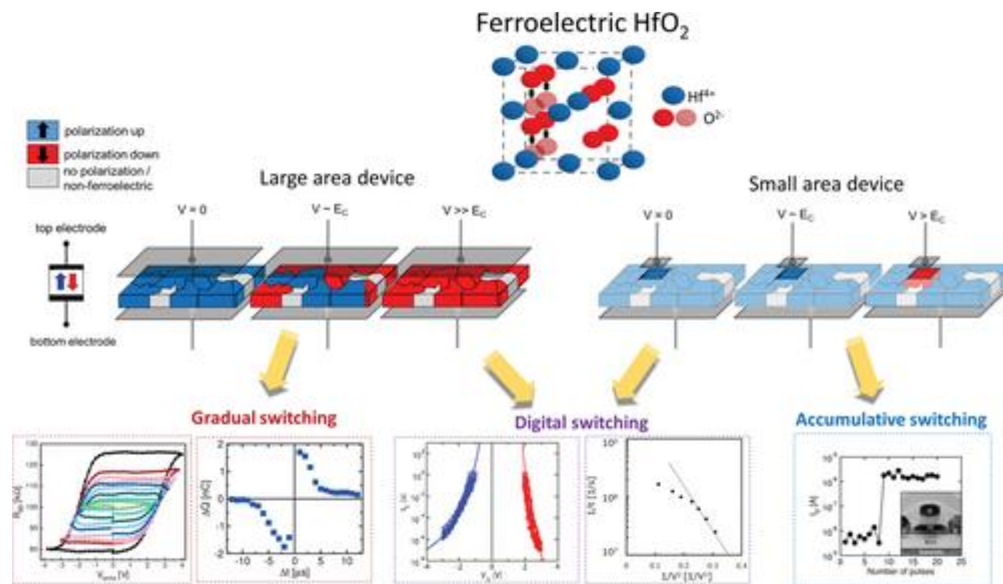

Figure 4

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The switching kinetics of ferroelectric devices are determined by the interplay between the individual ferroelectric domains and their characteristics. Accumulative single domain switching can be observed only in small-scaled devices where a very small number of domains is active. Due to the internal gain of the FeFET and its nondestructive and indirect readout scheme this is the only device where this effect can be observed. For larger devices, the ensemble of multiple domains defines the switching kinetics. The stochastic distribution of coercive fields, spatial location of the domains and their impact on the device characteristics give rise to the emergence of gradual switching between many intermediate states in the ferroelectric *PE*-sub-loops. It can be observed in FeFETs, FTJs as well as FeCAPs. Finally, digital switching is attained by complete polarization of all domains in either polarity, independently on the number of involved ferroelectric domains. The figure is in part reproduced with permission.[81] Copyright 2020, American Chemical Society; reproduced with permission.[82] Copyright 2017, IEEE; reproduced with permission.[70] Copyright 2018, American Chemical Society; reproduced with permission.[83] Copyright 2020, reproduced with permission.[84] Copyright 2020, AIP Publishing.

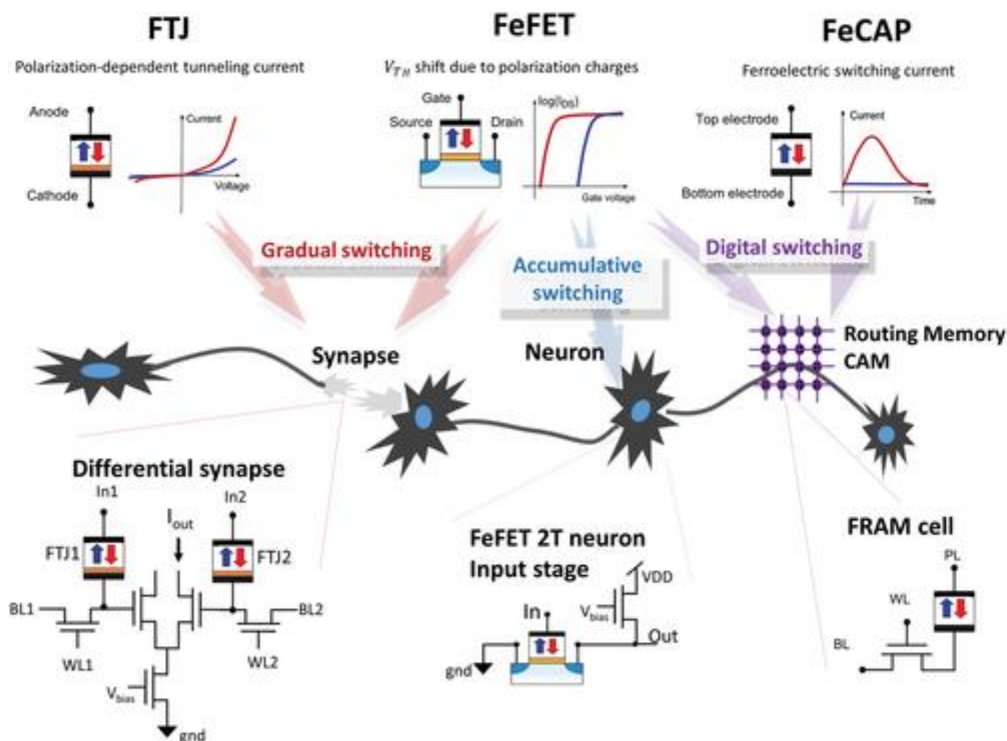

Figure 5

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The spontaneous ferroelectric polarization that occurs in ferroelectric materials such as the perovskite structure PZT or fluorite structure hafnium oxide can be used to store information. The memory effect is used in three different device concepts, FTJ, FeCAP, and FeFET. Moreover, the rich switching dynamics such as gradual analogue switching, accumulative switching or digital switching can be used in different applications. The gradual analogue switching is interesting for the application in synaptic weighting elements especially when using FTJ or FeFET devices. Moreover, the accumulative switching properties in small scaled FeFETs is a very interesting feature for the realization of the integration part of LIF-neurons. Finally, deterministic and digital switching is used to realize pure digital single-level or even multi-level memory or content-addressable-memory cells (CAM). These can be further utilized in neuromorphic systems, for example, as routing tables in address-event-representation (AER) based spiking neural networks,[85] where point-to-point connections between different cells are emulated by sending spikes as identifying addresses via a digital bus system.

Ferroelectric Capacitor and 1T-1C FeRAM

The basic FeRAM concept has been already proposed in the 1950s.[10] Within this memory concept the two terminals of a ferroelectric capacitor (FeCAP) are connected to perpendicularly oriented lines forming the memory array. Besides this simplest cross-bar array arrangement, in the 1T1C concept the first terminal of the FeCAP is connected to a plate line PL, whereas its second terminal is connected to one source/drain terminal of an additional access transistor, whose second source/drain terminal connects to the bit line BL and its gate to the word line WL. The 1T1C concept in general offers better array disturb immunity. Write operation is performed by applying the write voltages in either polarity between the two FeCAP terminals, for example, via PL and BL while switching on the access transistor via the WL in the 1T1C cell. During read operation the access transistor is switched on again and a voltage pulse is applied to the PL. Depending on the previously stored

polarization within the FeCAP, a polarization reversal occurs and the polarization switching charge is transferred to the BL. There a voltage signal develops which depends mainly on the non-switching capacitive load of the ferroelectric capacitor and the BL as well as the switched polarization charge according to: $\delta V_{BL} = 2P_r/(C_{\mathrm{FeCAP}} + C_{\mathrm{BL}})$. Hence, the actual read signal that is detected by a voltage sense amplifier (SA), typically being realized as a cross-coupled inverter SA using a fixed reference voltage or a reference voltage generated by reference cells, depends strongly on the whole array design, and there is a trade-off between BL length, FeCAP area, write energy, etc. The destructive read operation requires a write-back operation after readout. Hence, reading of the FeCAP requires up to twice the energy of the single write operation on cell level, depending on the data to be read. FeRAMs are commercially available since the early 1990s[11] after successful development of mature processing techniques for planar ferroelectric lead zirconium titanate (PZT) films. However, the need for a sufficiently large capacitor together with the limited thin-film manufacturability of the perovskite materials restricted their use to niche applications.[4] Thanks to its CMOS manufacturing compatibility the ferroelectric HfO_2 paved the way for the integration of scalable 3D ferroelectric capacitors[86, 87] and thus revived also the interest in the research on FeRAM scaling. First very encouraging results have been recently demonstrated. Functional FeRAM arrays with a memory size of 16[88] and 64 kBit[89] have been demonstrated which are interesting for embedded applications. The main challenges for commercialization of this technology as standalone product are the decrease of the ferroelectric layer thickness well below 10 nm and scaling of 3D capacitors toward the 10 nm node. First encouraging results of an 8 Gb 3D FeRAM featuring a 5 nm HZO layer have been presented recently.[87] In order to attain sufficient read margin between the two states and in view of a certain device-to device variability and some design constraints the reported capacitor area is in the range of 0.2–0.4 µm. Fast write operation in the range of some ns at write voltages of 2–4 V have been shown. Also, high endurance, reasonable data retention[90] and immunity of the data storage under solder reflow conditions have been demonstrated.[88] The improvement of the so called “wake-up effect” with increasing of P_r for low cycle counts as well as the “fatigue effect” resulting in a reduction of P_r at high cycle counts and the so called imprint effect which causes a shift of the polarization hysteresis along the field axis which are mainly caused from oxygen vacancy redistribution[91] and defect generation have to be tackled by proper engineering of the ferroelectric layer stack as well as the electrode materials when targeting at the realization of larger FeRAM arrays. The scalability of the FeCAP-based memory cell using planar capacitors might be improved by the adoption of a 2T1C concept, where an additional read transistor TR is integrated into each memory cell.[92, 93] In comparison to the 1T1C concept in the 2T1C cell the polarization charge of the ferroelectric capacitor is transferred just to the gate of the read transistor. Hence, a good matching between the size of TR and the ferroelectric capacitor is mandatory and thus the size of both, access and read transistor are mainly responsible for the cell size, implying the integration of the ferroelectric capacitor preferentially in the lower metallization levels and potentially cointegration of a back-end-of-line (BEOL) compatible select transistor.[93] However, so far single memory cells have been demonstrated and the successful array operation in view of the different read and write disturb effects still has to be proven. Other cell concepts such as differential 2T2C cells[94] targeting at larger read-margin might suffer from a too large cell footprint, while on the other hand further variants might enable the implementation of new functionalities such as compute-in-memory algorithms already on cell-level.[95]

Ferroelectric Field Effect Transistor

The read operation of the ferroelectric field effect transistor, which was proposed already back in 1957[96] relies on sensing the channel conductivity depending on the polarization state of the ferroelectric gate insulator. The electrostatic screening in the channel of the polarization charges at the interface with the ferroelectric, induces a depletion or an accumulation of carriers in the channel. For moderate modulation, the carrier density decays exponentially inside the conductor as described in a Thomas–Fermi approach, with a characteristic length inversely proportional to the square root of the carrier density. The channel material is either a semiconductor such as Si,[97] Ge,[98, 99] a semiconducting metal oxide[100] or a conductor with a carrier density typically below $10^{22}cm^{-3}$.[81] The latter concept is also referred to as ferroelectric thin film transistor (FeTFT). The readout can be performed either at a constant gate voltage by sensing the respective source–drain current or channel conductivity, respectively, or by sensing the required gate voltage in order to attain a certain source–drain current, that is, sensing the FeFET's threshold voltage V_{th}. The actual sensing scheme depends on the application and the used sense amplifier. Functional FeFETs based on perovskite ferroelectrics have been demonstrated already in 1975[101] and FeFET memory arrays with up to 64 kBit have been realized.[102] But due to difficulties in the technological implementation, limited scalability, and data retention issues, no commercial devices became available. However, with the discovery of ferroelectricity in the fluorite structure and CMOS compatible HfO_2 also the research in the FeFET concept based on the well-established high-k metal gate CMOS technology was pushed. Since then, very encouraging electrical results of fully front-end-of-line (FEOL) integrated FeFET devices have been reported and memory arrays above 1 Mbit have been realized in 28 and 22 nm technology.[97] Typical memory windows that are defined as the difference between the high-V_{th} and the low-V_{th} states are in the range of 1–2 V[103] and dependent mainly on ferroelectric layer thickness and the coercive field together with some other device design features. The ability of fine-grained cointegration of FeFET memory devices together with CMOS logic transistors paves the way for the realization of novel computing architectures that combine the functionality of logic and memory devices.[104, 105] Another variant of a ferroelectric field effect device was recently introduced by using the 2D ferroelectric

in a ferroelectric semiconductor field effect transistor (FeS-FET).[106] This material behaves as a semiconductor rather than an insulator and in contrast to the traditional FeFET device, in this device the channel itself and not the gate dielectric is ferroelectric. In this configuration, issues related to charge trapping at the channel/ferroelectric interface disappear. Within the channel and at the interfaces with the gate and the substrates, the ferroelectric charges are screened, resulting in a local change in the carrier concentration. The new properties of such devices yet remain to be explored and more research is required to find its application space.

4.2.1 Memory Density and Ferroelectric Domain Size

In FeFET devices that feature multiple ferroelectric domains, a gradual switching behavior can be observed.[107] The common understanding of the gradual switching effect is, that multiple current percolation paths form between the source and the drain terminals.[108] The different polarization dependent local threshold voltages in the channel average out, such that a continuous threshold voltage gradient develops. The number of available memory states is directly linked to the absolute number of ferroelectric domains in the device, the size of the domains being related to the material and to the microstructure of the thin-film. After the breakthrough in 2017 with the demonstration of Hafnia based 5-bit FeFET synapse (Si channel) with symmetric potentiation and depression characteristics,[82, 109] several variations were proposed. Reducing the footprint of the FeFETs to the 28 nm node lead to a transition

from analog to multi-level behavior,[68] as the area of the device became comparable to the ferroelectric grain size. That is, there is a direct trade-off between multi-level switching and device scalability. Similar as in the ferroelectric capacitor, a certain device-to-device variability in terms of switching kinetics and resulting threshold voltage after write operation which is mainly caused by the poly-crystalline nature of the ferroelectric HfO_2 so far limits the scalability of the concept to about 0.2 μm^2 cell size for storing digital values.[97] This variability might be tackled by further material stack optimization targeting at improved film uniformity and texture of the ferroelectric layer, as was observed in Lanthanum doped films.[78] Recent results on ferroelectricity in very thin hafnium oxide films on silicon[110] can be very interesting to optimize the film growth conditions. Additionally, it was also shown, that by controlling the oxygen vacancy concentration in the films the phase composition can be adjusted.[111] Therefore, tailoring the oxygen vacancy profile in the film could also be a path forward. However, here the trade off with cycling related instabilities, namely wake-up and fatigue of the films needs to be carefully considered.[91, 112] Improvement in variability can further be attained by proper selection of the electrical write conditions. For example, V_{th} target programming schemes that imply iterative programming and read operation until a certain target threshold voltage value is reached might be applied.[113] However,the accumulative switching behavior[69] which results in polarization reversal in FeFETs after application of several subcritical switching pulses might bear a certain risk of unintentional data manipulation in inhibited cells during such repeated write operations in FeFET memory arrays. For synaptic memory devices targeting at gradual and analogue switching, for example, in neuromorphic chips maximizing number of intermediate conductance levels is key for attaining high accuracy. Thus, to maximize the number of ferroelectric domains technology processes are being developed to allow for the integration of ferroelectric synapses in the BEOL, that is, above the CMOS levels, thus increasing the available synapse area. The challenging technology step for such integration relates to the crystallization temperature of ferroelectric materials, which should not exceed 450 °C to avoid any damages to the peripheral and neurons circuitry.[81, 114] In addition to fabricating a BEOL compatible FeFET based on a indium–tungsten–oxide channel, Aabrar et al. introduced a dielectric layer between two ferroelectric HZO 5 nm thick films, stabilizing partial polarization states and reaching 7 bits per cell.[114] To maintain a higher number of memory states while seeking for a reduced footprint, an alternative route for scaling the devices is the development of 3D devices and FinFeFETs, enabled by the atomic layer deposition of Hafnia ferroelectrics. For example, FinFeFETs of ref. [115] have 2 bits per cells for a fin width of 18 nm. Analog resistive switching was demonstrated in BEOL compatible FinFeFETs with a metal oxide channel.[116] Finally, attempts have been made to implement FeFETs into 3D-NAND structures.[117, 118] In contrast to the conventional NAND-FLASH, a faster write operation at lower voltages is envisioned. However, due to the limited memory window in the range of 1–2 V and device variability the realization of multi-level operation with more than 2–3 bits per cell might be problematic. Hence, this kind of memory could target at a higher speed but lower density storage class memory (SCM).[119] Another issue in the ferro-3D-NAND concept is the comparably low write voltage of the FeFET devices, which can cause issues especially for reading devices along the NAND string and for the write inhibit schemes. Thus, increasing the ferroelectric layer thickness might be the way to go for 3D-NAND, hence increasing the write-voltages and memory window[103] at comparatively low cost in terms of cell-area.

4.2.2 FeFET Reliability: Charge Trapping, Retention, and Endurance

The limited direct read after write capability of Si-channel based nFeFETs is caused by the strong electron trapping mainly during write operation with positive gate voltages. Unfortunately in these devices, an interfacial SiO_2 layer between the ferroelectric layer Si-channel material is unavoidable, which—if not intentionally implemented—would form during the crystallization anneal that converts the as-deposited amorphous HfO_2 into the orthorhombic $Pca2_1$ phase. Since the ratio between the permittivity of the interfacial SiO_2 layer and the doped and crystallized HfO_2 is in the range of 1/7–1/8, a rather large field of about ten times the coercive field of the ferroelectric applies to the interface. Obviously, high electric fields in the range of 10 $MVcm^{-1}$ can cause a strong electron injection into the layer stack, thus causing the unintentional charge trapping and drift effects as well as a wear out of the interfacial layer. These effects are also limiting the cycling endurance to typical values in the range of 10^5 cycles. Moreover, the dielectric capacitor connected in series to the ferroelectric capacitor causes a depolarization field[72] that made the realization of nonvolatility in FeFET devices almost impossible for decades.[120] Here, the high coercive field together with the comparable low dielectric permittivity of ferroelectric hafnium oxide turns out to be a large advantage.[54] These effects can be further adjusted by material stack engineering, for example by increasing the *k*-value of the interfacial layer by introducing a SiON layer,[74, 75] and by interface and band structure engineering. Recently it has been reported, that similarly manufactured pFeFETs based on a Si-channel exhibit a much lower charge trapping and threshold voltage drift after write operation,[99] offering a direct read after write operation. A second approach is to change the channel material, for example, by using semi-conductive metal oxides bears the opportunity to get rid of the additional interfacial layer, for example using amorphous indium tungsten oxide. Dutta et al. reported an endurance of 10^{11} cycles, a retention higher than 1000 s at 85 °C, and an operating voltage of +/−1.6 V.[121] The first InGaZnO based FeTFT by Kim et al.[122] showed large on/off (40) and high endurance, good linearity in the weight update, and recent work shows even larger on/off ratio of 10^5 and endurance of 10^7 cycles.[123]) Such concepts are especially interesting for the realization of FeFET devices in the BEOL of CMOS technologies.[81] A third approach is the introduction of an internal metal gate (IMG) leading to ferroelectric metal field effect transistor (FeMFET). An IGZO/HfO_2/IMG/HZO/TiN memory device showed threshold voltages of only −0.41 and −0.28 V for an IMG made of TiN,[124] indicating weak defect trapping in the device. In similar MFMIS synapses with a tungsten IMG, 10^8 cycles and 10 years of retention were achieved.[125] Additional interesting electrical features such as a virtual increase or even shift of the whole memory window by applying a back-bias are attained when implementing double-gate transistors as was demonstrated based on a 22 nm FDSOI technology.[126]

Ferroelectric Tunnel Junctions

Under the name “ferroelectric tunnel junctions” exists a broad variety of two-terminals devices comprising a ferroelectric layer that is thin enough to allow a current to flow through it. This basic concept was proposed by L. Esaki et al. already in 1971 as a “polar switch.”[127] But again it took more than three decades until first functional FTJ devices were demonstrated mainly due to difficulties in fabrication of an ultra-thin ferroelectric layer with thicknesses below 4 nm being mandatory to attain reasonable tunneling currents. A first significant milestone was reached in the 2000's when electroresistance (a change in electrical resistance with current) in ferroelectric tunnel junctions was obtained using a 6 nm thick PZT ferroelectric film sandwiched between a metal (Pt) and a n-type semiconductor (strontium ruthenate) electrode[128] or using $BaTiO_3$ ferroelectric layers.[129] Since the discovery of

ferroelectricity in the fluorite structure HfO_2, several FTJ devices have been demonstrated using this CMOS-compatible material.

4.3.1 Tunneling Electroresistance Ratio

According to the model proposed by Zhuralev et al.,[130] the screening of the negative or positive polarization charges in a semiconducting electrode creates a depletion or an accumulation layer, modulating the effective tunneling barrier thickness and thus the tunneling probability. The polarization-dependent current can be measured nondestructively when applying voltages to the electrodes that are smaller than the coercive voltage V_c of the ferroelectric layer stack. In order to attain a reasonable current difference between on- and off-state and thus a large tunneling electroresistance ratio (TER), which is defined by TER = $(G_{LRS} - G_{HRS})/G_{HRS}$ as the ratio between G_{LRS} the conductance in the low- and G_{HRS} the conductance in the high-resistive state, respectively, the FTJ device has to be formed with an asymmetric layer stack. For example, different metal electrodes featuring different screening lengths of electrons result in a different band bending at the ferroelectric-to-electrode interface, thus modulating the effective tunneling barrier. However, the effect of screening length on the electroresistance modulation is limited, thus resulting in a low TER.[131] Improvement can be obtained by replacing one electrode by a semiconductor material featuring a much lower carrier density and thus resulting in a larger band bending and higher TER[132] or by electrode work function engineering.[133] Similarly as in the FeFET device it is complicated to avoid the formation of an additional interfacial layer when depositing the hafnium oxide directly on Si or Ge, giving rise to an even larger asymmetry in the stack, but reducing the on-currents. The use of a metallic oxide interlayer (for example atomic layer deposited tungsten oxide[134] or indium gallium zinc oxide[135]) allows for the fabrication of asymmetric stacks with large currents. In the double-layer FTJ concept, an additional tunneling dielectric layer is intentionally inserted between one of the metal electrodes and the ferroelectric switching-layer[136-138] or in combination with a semiconducting electrode.[139] In this concept, the functionality of ferroelectric switching layer and dielectric tunneling layer are separate and thus these layers might be optimized independently. However, due to the imperfect screening of the polarization charge, the depolarization field and its impact on the data retention becomes more important. Improvement was reported by the adjustment of the work-function of the electrodes.[140] Typical current densities are in the range below 1 pAµm^2. Such low on-currents bear a challenge for the read-out operation. In memory arrays typically currents in the range of some µA are mandatory for reading the memory state in the ns-range. That is, for scaled FTJ devices read times in the range of several 10 µs are mandatory. Thus, increasing the on-current density while keeping the TER high is one of the most important objectives of FTJ optimization. In order to increase the on-current density a lower stack-thickness is preferable. FTJs with just 1.5 nm epitaxially grown ferroelectric HZO on single crystalline $SrTiO_3$ (STO) (001) substrate have been demonstrated that feature high TER ratio and large on-currents.[141] However, for ALD-deposited ferroelectric HfO_2 layers that would be mandatory for CMOS integration it has been reported that the ferroelectric properties degrade with scaling the layer thickness.[142] A potential solution was found by first depositing and crystallizing a thicker ferroelectric layer and in a second step reducing it is thickness by adoption of an atomic layer etching (ALE) step,[143] yielding current densities of several pAµm^2 and a TER of above 10^3. Similarly as in the FeFET case, gradual polarization switching can be attained in FTJ devices. Moreover, since the current flow is perpendicular to the layer stack and no percolation paths form, an even more gradual switching effect can be attained.

4.3.2 Depolarization Fields in Ferroelectric Tunnel Junctions

In the ideal case of a symmetric MFM capacitor, the polarization charges are screened and the various ferroelectric domain configurations are stable. In functional devices the retention of—generally one out of the two extreme—memory states can be affected by the existence of a depolarization field. The later can originate from the reduced ferroelectric film thickness[144] in synaptic weights such as ferroelectric tunnel junctions, or from the use of asymmetric electrodes exhibiting a different work function. In most technologies, the conductance change obtained in the synaptic weight originates from the ferroelectric field-effect, and in at least one of the two configurations the polarization charges are not screened by a metallic layer but by a conducting layer with a limited carrier density,[145] a depleted semiconducting layer (see ref. [146] for a temperature dependent study of the depolarization field) or, as described in the previous paragraph, a dielectric layer. The poor screening eventually leads to the spontaneous backswitching of ferroelectric domains toward the most stable configuration. Nevertheless, energy band diagram engineering allowed for the fabrication of ferroelectric nonvolatile memories exhibiting retention higher than 10 years.[135] In particular, Van der Waals heterostructures based on a

layer and a CIPS ferroelectric film show excellent retention during 10^3 s and the 10 years projection. Although the fabrication methods such as exfoliation and transfer on Si are not compatible yet with production lines, these devices feature promising characteristics: no wake-up, operation voltage below 5 V and on/off higher than 10^4 using an MoS_2 channel[147] or an In_2Se_3 channel.[148] In summary, instead of being the perfect memory device, FTJs are rather interesting candidates as synaptic devices[138] to be used as single or differential elements in synaptic circuits[149] or in arrays in a cross-bar arrangement.[150] These applications will be discussed in more detail in the next section.

5 Ferroelectric Devices for Neuromorphic Computing

The development of ferroelectric devices for usage in neural networks, driven by the demand of weight storage in ANNs, follows decades of research on resistive elements and nonvolatile memories. In 2008, Strukov and coworkers identified the connection between resistive switching memory cells and the memristor concept proposed by Chua back in 1971.[151, 152] Consequently Chua stated: “All 2-terminal nonvolatile memory devices based on resistance switching are memristors,”[153] and the first work on intermediate electroresistance levels in $BiFeO_3$[154] and $BaTiO_3$[155] perovskite ferroelectric tunnel junctions gave birth to ferroelectric memristors. In NVM applications, the programming procedure ensures that a predefined information is stored in the ferroelectric memristors. In this section, we will describe how for neuromorphic application, in addition, both the resistive properties of the synaptic elements (weights and synapses) and the programming dynamics are key. In ref. [156] Shimeng Yu proposed the following desirable performances metrics for synaptic devices: a device dimension below 10 nm, over 100 distinct resistance states, an energy consumption below 10 fJ per programming pulse, a dynamic range above 100, 10 years retention for inference applications and an endurance above 10^9 updates for online training application. In this section, we will detail how the requirements vary depending on the use of the synapse, link the later to the ferroelectric materials properties and provide examples. For the resistive properties, the requirements in term of current–voltage linearity will be specified depending on the number of bits represented by the synaptic element. Then, we will describe why the memory properties requirements differ for weights in ANN inference and ANN online-learning, as well as for synapses in SNN. In the second part on this section the focus will be

on the programming dynamics. Different circuit structures and algorithms lead to different requirements in terms of weight update. We will define weight update "linearity," a key figure for evaluating the learning rate of an ANN, as well as desired nonlinearities in synapses for SNN. We will describe how in both cases these parameters relate to the ferroelectric domains switching dynamics.

Resistive Properties of the Synaptic Elements

In artificial neural networks (Figure 1a), the information propagates from one layer of nodes to the next. Between each layer, a matrix–vector multiplication, or multiply and accumulate operation, is performed. By analogy with the brain, the matrix elements of a static ANN are called "synaptic weights." This operation can be implemented in the analog domain by adding the voltage drops along the bitline in a cross-bar array of programmable memristors. In a crossbar configuration, the "accumulate" operation is physically obtained by Kirchhoff's law: at each bitline, the currents coming from the various wordlines are summed. In Ohmic resistors, the "multiply" operation lies in the linear relationship: $I = G*U$ where I is the current, G the conductance and U the input voltage. In binarized neural networks[157] or ternary neural networks,[158] the weights are constrained to two or three values and the linearity of the current–voltage characteristic is not required. The implementation of the multiply and accumulate operation using a crossbar of analog weights[159] requires such linearity, and experimental demonstration of classification using a crossbar arrangement of resistive memory cells was successfully demonstrated.[160] In two-terminals devices, both during the weight update (**Figure** 6d) and the reading (Figure 6e) the current flows through the ferroelectric layer. In FTJs, the conduction mechanisms are generally non linear: in ferroelectric or dielectric tunnel barriers, either Direct or Fowler–Nordheim tunneling (FNT)[155, 161, 162] is observed. Increasing the thickness of the ferroelectric layer leads to an increase in the relative contribution of the thermionic emission.[163] In hafnia ferroelectrics, the presence of shallow traps is associated to Poole–Frenkel conduction[164] or modified Schottky emission,[165] which are also nonlinear conduction mechanisms, making them poor candidates for the analog implementation of the "multiply" operation. Berdan et al. exploited the fact that the nonlinearity factor was constant for various conductance levels in ferroelectric

tunnel junctions: as represented in Figure 6a, the nonlinearity of the current–voltage relation was circumvented by logarithmic line drivers.[166] Another approach relies in exploiting the limited number of electrons that can be excited to the conduction band of the ferroelectric layer, either from impurity levels or from the valence band, leading to Ohmic conduction at small bias. In HZO films thinner than 3 nm, linear current-voltage characteristics were obtained up to 100 mV, for a current density reaching 0.01 Acm^{-2}.[134] The nonlinearity is easily circumvented in three-terminal synaptic elements or FeFETs, where the current during the reading does not flow through the ferroelectric layer but through a channel material. In three-terminals devices, the weight update (Figure 6f) is performed using the gate (G) and the drain (D), whereas the reading (Figure 6g) is performed by the channel (S–D) read-out. In this configuration, excellent I_{DS}–V_{DS} linearity was obtained using conducting oxides, for example [81] or $BaSnO_3$[167] as channel materials. Indium–tin-oxide (ITO) shows Ohmic conduction and can be combined with HZO in a BEOL compatible process.[168] Combining ferroelectric gates with 2D materials, whose integration remain difficult, can also lead to devices with linear conduction. ReS_2 using Au/Cr contacts exhibited an on/off ratio up to 10^7 using a P(VDF-TrFE) ferroelectric in the gate stack,[169] and

using Ti/Al/Au contacts exhibited an on/off ratio of up to 10^6 using HZO in the gate stack.[170] Finally, other approaches than summing the weights using Kirchhoff's law were suggested. Kamimura et al. proposed to use the threshold voltage of the FeFET instead of the channel conductance to represent the synaptic weight. The product sum operation is not operated using Kirchoff's law but by summing a number of clock pulses in 4-bit MFIS FeFET transistors.[171] A cycling endurance of 10^4 cycles, a dynamic range of 10^4 and lower power consumption per neuron compared to the sequential product-sum operation were obtained. In addition, computing concepts using hybrid precision were proposed with ferroelectric devices. In a 2T-1FeFET synapse, the 6-bit less significant bits (LSB) are represented by the volatile gate voltage of a FeFET and four polarization states serve as 2-bit most significant bits (MSB).[172] Kazemi et al. proposed a 6-bit synapses consisting of a 3T1C cell for the LSBs and of a 1T-1FeMFET cell for the MSBs (four states).[173]

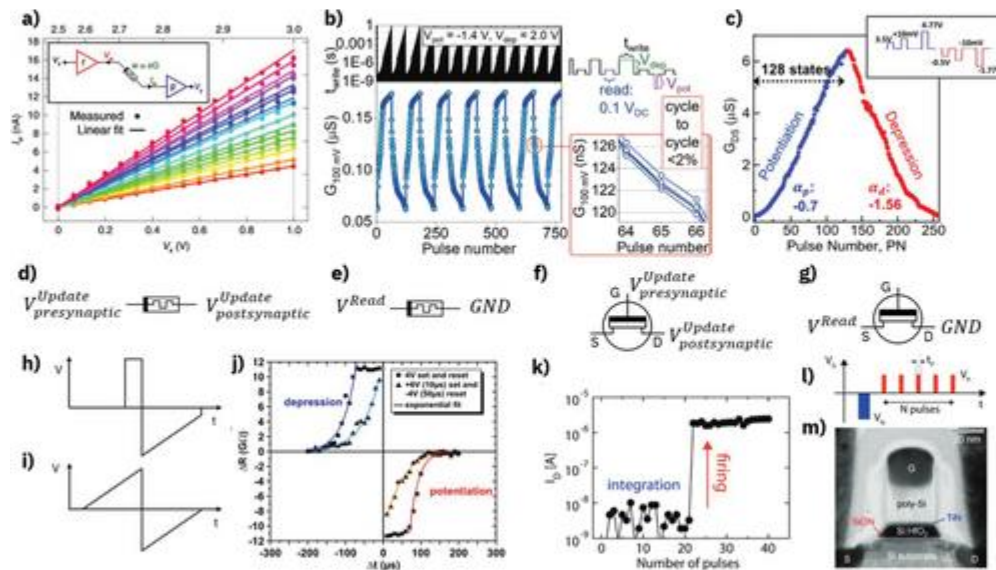

Figure 6

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a) Current measured after programming a HfSiO FTJ device in 16 different states, using the circuit shown in the inset: a logarithmic wordline driver (red), a bitline transimpedance amplifier (blue) and a nonlinear FTJ memristor. Reproduced with permission.[166] Copyright 2020, Springer Nature. b) Conductance measured after programming a FTJ device using pulse of constant amplitude V_{pot} = 1.4V and V_{dep} = 2.0V, and of exponentially increasing duration, as represented in the top right inset. The conductance is measured by a DC bias of 100 mV. The bottom left inset shows the overlap of six consecutive cycles in a narrow range. Reproduced with permission.[165] Copyright 2022, John Wiley and Sons. c) Drain (D)–Source (S) conductance measured after programming a HZO/HfO_2/HZO/IWO FeFET device using pulses of constant duration and linearly increasing amplitude, as represented in the inset. The linearity coefficients αp and αd are defined in ref. [183]. Reproduced with permission.[114] Copyright 2022, IEEE. In two-terminals devices, d) the weight update and e) the reading use the same connections. In three-terminals devices, f) the weight update is performed using the gate (G) and the drain (D), whereas g) the reading is performed by the channel (S–D) read-out. h) Waveform optimized for spike-timing-dependent-plasticity (STDP) according to ref. [192]. i) Alternative waveform used in ref. [138]. j) Resistance change of a HfSiO FTJ device as a function of the timing between two spikes as in (i) of opposite polarities, emulating biological STDP curves. Reproduced with permission.[138] Copyright 2020, American Chemical Society. k–m) Accumulative switching in FeFET. Applying the pulsing scheme (l) on a nanoscale FeFET

whose cross-section is shown in (m), the device switches from Off to On state with pulses of amplitude 2.2 V and duration 1 µs, emulating a neuron. k–m) Reproduced with permission.[70] Copyright 2018, Royal Society of Chemistry.

Memory Properties of Synaptic Weights

For artificial neural networks inference applications, long retention times of 10 years are required. The situation is different for neural networks trained online, where a retention longer than 1 day is sufficient because the weights are continuously updated. Finally, neuromorphic architectures using advanced synaptic functionalities eventually implement the short-term plasticity observed in the brain. “Facilitation” results in an increase of the synaptic strength over a short period of time typically in the 100 ms range, whereas “augmentation,” resp. “depression” result in an increase or decrease of the synaptic strength over a moderate duration of typically 10 s. The “long-term plasticity” lasts at least several tenths of minutes and the memory can be eventually consolidated in response to repetitive exposure to a learning event.[174] In addition to spontaneous backswitching of ferroelectric domains which can lead to an unidirectional drift of the synaptic weight, mechanisms related to charge trapping/detrapping were reported.[175] Triggered by recent advances in neuromorphic vision systems, research on optoelectronic, ferroelectric synapses emerges. Xue et al. proposed to exploit the strong coupling between ferroelectricity and photovoltaic effects in the 2D ferroelectric material

. The synapse shows advanced functionalities such as LTP, STP and paired pulse facilitation.[176] The combination of STP at low bias and LTP at large bias was obtained in $BaTiO_3$ by Li et al.,[177] allowing the supervised training of a network using a backpropagation algorithm.

Synaptic Weight Update

In contrast to non-volatile memory as well as inference in ANNs, for neuromorphic applications the synapse's weight update is strongly linked both to the learning algorithm and to the neuromorphic chip design. Common to all ferroelectric devices is a polarization-voltage hysteresis loop exhibiting positive and negative coercive and saturation voltages. In absolute value, the coercive voltage is the voltage below which the domains oriented anti-parallel to the direction of the field do not switch. As the amplitude increases, ferroelectric domains switch until the saturation polarization is reached at the saturation voltage. This dependence on the electric field translates into the observation of a weight update upon the application of pulses of constant duration, and of an amplitude comprised between the coercive and saturation voltages. It is also possible to obtain a weight update using a constant amplitude, as the domains switching dynamics in ferroelectrics are universally governed by Merz's law, that is, the characteristic switching time varies exponentially with the inverse of the electric field pulse.[178] However, the definition of the characteristic switching times depends on the microstructure of the ferroelectric film (single crystal, textured, polycrystalline,…), the energy of the domain walls and the dynamics of the domain switching. In polycrystalline hafnia, it corresponds to the duration of a single pulse in order to switch the domains.[134, 179] In epitaxial $BaTiO_3$ however, the switching time corresponds to the cumulative duration of sequential pulses.[177, 180, 181]

5.3.1 Weight Update in Static Artificial Neural Networks

In this section, the "static" ANNs (as defined in Figure 1a as opposed to SNN) implemented with ferroelectric resistive memories as synaptic weights, are discussed. The online training of such networks is possible by implementing learning rules such as back-propagation. As seen above, the weight update in ferroelectric devices can be performed by applying pulses of increasing amplitude or duration, as illustrated in Figure 6b,c. For the implementation of gradient descent algorithms, it implies that the pulse applied for the weight update is a function of the actual conductance of the weight. The exponential dependence of the pulse duration on the fraction of switched domains can be exploited in this respect (Figure 6b). Other effects than ferroelectric domain switching are eventually involved at long timescales, such as oxygen migration. See for example the in operando electron microscopy of an epitaxial, hafnium zirconium oxide capacitor in ref. [182]. Similarly, recent works simplify the weight update by utilizing the voltage relation, with a constant weight update upon pulses of linearly increasing amplitude, as represented in Figure 6c. In this figure, the linearity coefficients are defined as proposed by Chen et al.[183] For this scheme, the technical implementation is constrained by the maximal available voltage amplitude on chip. This ideally should not exceed 5 V, a value often below the DC saturation voltage of ferroelectric devices. A first method is to reduce the ferroelectric thickness, with a compromise on the annealing temperature and on the polarization.[184] A second method to reduce the coercive voltage consists in engineering the device layer stack, for example by combining ferroelectric HZO and anti-ferroelectric ZrO_2.[185] In the quest of reducing the operating voltage, MFMIS capacitor were integrated in the gate stack of a FeFET to obtain a FeMFET.[186, 187] By controlling the ratio between the MFM area and the MIS area, the synaptic plasticity of the MFMFIS FeMFETs offered low voltage and high-speed analog weight update. A gradual weight update upon identical pulses, separated in time by a relaxation period is also applied. These dynamics are typically observed in current-driven memristors such as filamentary, valence change or phase change resistive memories. Cumulative switching was observed for example in ferroelectric Schottky barrier field-effect transistors,[188] where the ferroelectric polarization modulates both the Schottky barrier at the source/drain contacts and the potential in the channel,[189] modulating the carrier injection. In the ideal case, the weight update is a linear function of the number of applied pulses. Leveraging the optoelectronic effect can allow for a linear weight update. Xue et al. obtained it by gradually displacing domain walls in a lateral device, combining light spikes for the potentiation and electrical spikes for the depression.[176] Zhou et al. obtained cumulative switching with linearity coefficients[183] as small as 0.6 and −1.2 while achieving an on/off ratio of 30, using a monolayer of WSe_2 gated by a P(VDF-TrFE) polymer ferroelectric.[190] Excellent linearity coefficients of 0.01 and −3.8 for an on/off of 3 were also obtained for the identical pulse scheme in domain wall synapses made from $LiNbO_3$ ferroelectric crystals bonded to SiO_2/Si wafers.[191]

5.3.2 Nonlinear Synapses for Neuromorphic Systems

Ferroelectric synapses are also excellent candidates for the implementation of bio-inspired, unsupervised training for example using Hebbian learning. The plasticity rule is such that correlated activation of pre- and postsynaptic neurons leads to the strengthening of the connection between the two neurons. Reciprocally, the shape of the spike (amplitude, duration) is such that a pre- or a post-synaptic spike alone does not change the ferroelectric domains configuration. Lecerf et al. proposed an optimal spike shape for the implementation of "spike-timing-dependent plasticity" (STDP) using ferroelectric memristors.[192] The waveform of the spikes emitted by the pre- and post-synaptic neurons, represented in Figure 6d, is tailored with respect to the coercive field of the ferroelectric domains. In the optimal situation, the saturation polarization is reached at a saturation voltage that is less than

twice the coercive voltage. The amplitude and the duration of the electric field applied to the synapse depends on the delay between the post- and pre- synaptic pulses and results in an STDP response similar to the biological one. Boyn et al. demonstrated that STDP could be harnessed from switching fractions of ferroelectric domains in tunnel junctions,[180] showing the potential of ferroelectric memristors as solid-state synapses. In these single crystal ferroelectric films, successively applying pulses with the same waveform leads to the gradual reversal of domains. As for biological synapses, cumulative switching is observed. STDP was reproduced later in epitaxial single crystals.[181] Using a different waveform as shown in Figure 6e, Max et al. demonstrated STDP in polycrystalline hafnia.[138] The weight update as function of the spikes time delay is reproduced in Figure 6f. Some Van der Waals semiconducting materials such as

exhibit room temperature ferroelectricity and are promising candidates for neuromorphic computing. The synapses proposed by Wang et al. exhibit LTP with identical pulses (cumulative switching) as well as STDP.[193] On Silicon, Xi et al. demonstrated excitatory/inhibitory post-synaptic current, paired pulse facilitation/depression and STDP in Schottky barrier FeFETs.[188] Liu et al. exploited the combination of STP and LTP in a synapse based on ferroelectric

to build a multilayer reservoir computing system,[194] a type of recurrent neural network performing in temporal information processing. Finally, reward-modulated spike-timing-dependent plasticity was demonstrated in a cell consisting of two FeFETs exhibiting reconfigurable polarity behavior.[190] Here the ferroelectric polarization allows to set the first WSe_2 channel as n-type and the second as p-type.

Accumulative Switching in Ferroelectric Neurons

The hysteretic *IV*-characteristic of FeFET devices has been explored for adoption in relaxation-oscillator based neuron circuits.[195] The switching dynamics of the FeFET device (see Figure 4) thereby plays an important role for the whole dynamic behavior of the neuron circuit.[196] In small-scaled FeFETs with a gate area in the range of the ferroelectric grain size, an interesting effect, namely the abrupt stochastic single domains switching can be observed.[68, 197] Due to its internal gain the FeFET is the only practical device that allows the characterization of the switching of such single domains with an area of just some 10 nm in diameter. A cross-section of such a device is represented in Figure 6i. Switching kinetics measurements are adopted to characterize the threshold voltage evolution by applying switching pulses with increasing width and amplitude in either polarity and monitoring the on-current or threshold voltage. From this data, the relation between the switching voltage and the switching pulse width—for example targeting at changing the memory state by 50%—can be extracted. An accumulative switching behavior has been observed as well, as represented in Figure 6g, where multiple accumulated subcritical switching pulses (Figure 6h) finally lead to a polarization reversal[69, 107] of a single domain. This is a very interesting feature for the potential realization of the accumulative input characteristic in neuron circuits since it results in very abrupt threshold voltage changes. Interestingly, there seems to be a universal time–voltage dependence for both: one-shot switching—that is, applying just single pulses like in synapses—and accumulative switching—that is, applying multiple pulses as would be used for example as input to a neuron circuit, for switching of single domains as well as a collection of multiple domains[107] and for nFeFETs as well as for pFeFETs.[99] It is to be mentioned here that the cumulative switching which is adopted in synaptic devices and the accumulative switching originate from the very same physical

mechanisms and the differentiation is given mainly from the device size and operation modes. Tuning the FeFETs internal depolarization field in an opposite way as would be done for a memory, namely decreasing its retention time can be adopted to generate the leaky-behavior of neurons.[198] Moreover, the dynamics of the neurons input might be electrically adapted further by the adoption of positive as well as negative gate voltages being defined as excitatory or inhibitory inputs.[199] That is, the rich ferroelectric switching dynamics facilitate the development of a large variety of neuron functionalities that might allow the creation of all-FeFET-based neural networks.[200] Even though till now there is only little work on adoption of FTJ or even FeCAP devices as input device for artificial neurons, this topic might be explored in near future as well, since many of the specific switching dynamics features are very similar in all of these device concepts.

6 Summary and Conclusion

In summary we have explained the basics of ferroelectricity with a special focus on ferroelectricity in hafnium oxide based material systems. This new class of ferroelectric materials is only known for little more than a decade now. The main properties for building memory cells and devices for in-memory and neuromorphic computing as well as the current knowledge on the influencing factors to engineer these properties toward different applications have been discussed. Going further the three different ways of reading out the ferroelectric polarization leading to the three memory concepts of capacitor based ferroelectric random access memories, ferroelectric field effect transistor, and ferroelectric tunnel junctions have been introduced and their status was briefly discussed. This sets the stage for the extensive discussion on using ferroelectrics in both artificial neural networks and spiking neural networks. Here important results from material systems other than hafnium oxide have been included to give a broad picture of the current status and theoretical understanding of such approaches. When comparing the status of ferroelectric devices with competing concepts like magnetoresitive devices phase change devices or ion based resistive switching devices, we need to consider, that due to the limited CMOS compatibility the interest in ferroelectrics moved toward the other three material classes. It was only after the first reports on ferroelectricity in hafnium oxide, that the interest has revived and it took about 5 years until the community was convinced that the presented results indeed reflect a ferroelectric effect. So it was only about 5–7 years ago since broad activities had been revived. In the meantime, the research and development activities have reached a similar level as in the other devices mentioned above. When comparing them from a performance point of view, then the main advantages of hafnium oxide based ferroelectric devices lie in the fact that it is a well behaved switching mechanism that has a low power writing operation in combination with nonvolatility and allows to realize three different basic devices including transistor based nonvolatile memories, that are not straight forward using any of the other mechanisms. However, they also have some shortcomings. In comparison with MRAM, the lower write energy and the simpler stack as well as the flexible device concepts are advantages, while the lower write voltage and the even better understanding of the physics are pluses for magnetoresistive devices. With respect to the ability to store more than 1 bit, there is a small plus on the ferroelectric side while there is a small plus with respect to endurance potential on the magnetoresistive side since there is no inherent degradation during switching of magnetic materials. In comparison to phase change devices, the more efficient write mechanism and the flexible device concepts speak for the ferroelectric devices while phase change devices are more mature at least compared to hafnium oxide based ferroelectric devices and can more easily allow multiple bit storage. For comparison with restive switching devices, we restrict ourselves here to valence change[201] and electrochemical metallization

devices.[202] Again the flexible device concepts and the low power write is in favor of the ferroelectric devices while the resistive switches are even a bit easier to integrate. Moreover in resistive switches the realization of storing many levels in a single cell is easier to achieve. However, ferroelectric switching is a more defined and well understood physical process compared to the complex switching of valence change and electrical metallization cells especially since the latter two include the formation of a filament, that makes a forming process necessary and adds to fluctuations in the switching process. In **Table** 2 we have compared the most important properties of different devices currently considered to realize basic functions in neuromorphic systems. In addition to the devices already briefly discussed above, we have also added analogue resistive switching devices,[203, 204] that are more frequently explored recently but not have reached the maturity of the devices mentioned above as well as charge trapping[205] and floating gate[206] devices as used in Flash memories, since the latter are the most mature options. In conclusion there is no clear winner among the discussed concepts and we can expect to see all of them coexisting and optimized for different applications. When looking at the current research activities in the field of neuromorphic computation as the main field discussed in this paper, we see that ferroelectric devices have seen a strong growth in the last 3–4 years and the activities have almost reached the level of those of using resistive switching devices for neuromorphic computing underlining the huge potential the scientific and engineering communities see in such approaches.

Table 2. Comparison of the main parameters and features of FeFET and FTJ devices with other device types currently considered to realize the basic functions of neuromorphic systems.

HfO_2 based FeFET	**HfO_2 based FTJ**	**Magnetoresistive (spin torque t)**	**Phase change**	**Filamentary resistive switching**	**Analogue resistive switching**	**Charge based nonvolatile transistors as used in Flash**	
Data storage	On/off 10 to 1000. Tradeoff: footprint versus number of states (3 to >128)	Tradeoff: min current density versus on/off (2 to 20). Continuous switching.	On/off 3. <10 levels.	On/off > 100. Binary PCM, 8 levels for projected-PCM.	On/off 10 to 1000. Continuous switching	On/off 10 to 100. Continous switching	On/off 1E6 to 1E9. Continuous switching
Density	Limited by variability due to poly-crystalline material,	Scaling limited mainly by low on-current density 0.2 µm	20 F^2 cell size, mainly driven by select device	High scalability in $4F^2$ cross-point arrays	20 F^2 cell size, mainly driven by select device (on-currents	Scaling limited mainly by low on-currents	4 F^2 cell size planar, best scalability in 3D NAND integration

HfO_2 based FeFET	HfO_2 based FTJ	Magnetoresistive (spin torque t)	Phase change	Filamentary resistive switching	Analogue resistive switching	Charge based nonvolatile transistors as used in Flash	
	currently 0.2 µm				during erase)		
Weight update	Field or current driven, limited cumulative effect, cycle-to-cycle variation <2%		Stable binary switching, stochastic, current driven intermediate switching.	Cumulative switching, but stochastic and non-linear in non-projected PCM.	Cumulative switching. Stochastic intermediate switching due to Joule heating.	Cumulative switching, non-linearity.	Cumulative switching typically program verify and increasing programming voltage are applied
Symmetry	Fair; tuneable by stack engineering and operation mode	Fair; tuneable by stack engineering and operation mode	NA	Low symmetry due to different operation mode for program and erase	Low, but tuneable by operation mode	Fair	Low symmetry due to different operation mode for program and erase
Retention	>10 years	>10 years	>10 years for binary	Drift from LRS to HRS	>10 years	Months to years	>10 years
Endurance	1E6–1E11 1E6–1E11	1.00E+11	1.00E+09	1E6–1E8	1E3–1E6	1E3–1E6	
Writing	<5 V, 50 ns. High gate impedance: fJ	1–5 V, 20 ns. tradeoff: Energy versus Ioffmin	0.2 V, 10 ns.	1–3 V, 10 ns	1–3 V, 100 ns	1–5 V, 10 ns–10 ms	CHE: 5 V, 1 µs FN: 20 V, 100 µs–1 ms
Read speed	< 10 ns	Low; 10 µs - range due to low on-currents and	< 10 ns	< 10 ns	< 10 ns	µs - range due to low on-currents and self-capacitance	NOR < 10 ns NAND: 50 µs–1 ms

HfO_2 based FeFET	**HfO_2 based FTJ**	**Magnetoresistive (spin torque t)**	**Phase change**	**Filamentary resistive switching**	**Analogue resistive switching**	**Charge based nonvolatile transistors as used in Flash**	
		self-capacitance					(depending on the number of levels stored)
Ease of integration	Trade-off: device-to-device variability and footprint. Wake-up effect.		Noisy intermediate levels. Possible connectivity using magnetic waves.	Broad LRS distribution	Noisy intermediate levels. Require forming (5 V). Device-to-device variability after forming. Large (µA) Off currents. Read disturb.	Often unusal materials many different approaches but all are on a basic research level	High voltage support devices required
High impedance/parallel operation	Impedance tuneable, sub-threshold operation possible	Very high impedance, parallel read operation preferable	Tradeoff between on-current and read speed, large write current impede parallel write	Good in 1S1R crossbar arrays	Tradeoff between on-current and read speed, large write current impede parallel write	Very high impedance, parallel read operation preferable	Limited in NAND array architecture
Comment		Tradeoff between retention and endurance can be tuned by magentic anistropy of		Options are: Valence Change and Electrochemical Metalization cells	Physical mechanisms: Charge storage or area dependent oxygen	Two flavors: floating gate (FG) and charge trapping (CT) CHE: channel hot electron programmin	

HfO_2 based FeFET	HfO_2 based FTJ	Magnetoresistive (spin torque t)	Phase change	Filamentary resistive switching	Analogue resistive switching	Charge based nonvolatile transistors as used in Flash
		the free layer			vacancy migration	g FN: Fowler_Nordheim programming

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Conflict of Interest

The authors declare no conflict of interest.

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