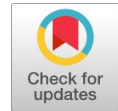


Performance Analysis of an Efficient Router using X Y Algorithm

Geethanjali N, Rekha K R



Abstract: As more and more functions are expected to be performed by a single electronic device (such as a smartphone, smart television, etc.), the need to have more and more components on SoC is increasing, posing new difficulties for NoC. The majority of NoC designs utilise mesh, torus, or other topologies to ensure a robust router. Most solutions, however, fall short when it comes to addressing key issues like throughput, area overhead, and latency, as well as QoS and congestion. The current paper proposes a concept for a reconfigurable router that can be used in NoC settings. For the suggested router's design, we use Verilog, formal language for describing hardware (Verilog HDL). The four-channel router presented here has an east-west-north-south orientation and a crossbar switch connecting the two pairs of channels. Each channel consists of a multiplexer and a FIFO buffer. The input and output are handled by multiplexers, and the data is stored in FIFO buffers. The FIFO and multiplexer architectures for the south channel are developed initially. Afterwards the remaining three channels and the crossbar switch are made. Routers use channels, FIFO buffers, multiplexers, and crossbar switches in their overall design. Simulating the proposed design in Modelsim and obtaining the RTL view in Xilinx ISE 14.0 are the two primary methods of approaching this problem. The suggested reconfigurable router's power consumption is greatly reduced by employing the Power gating technique.. The XPower Analyzer application is used to determine the total power. As demonstrated by the findings obtained, the proposed design uses less energy than conventional reconfigurable routers

Keywords: IP core, NOC, On Chip Network, Router, X Y algorithm.

I. INTRODUCTION

THERE ARE now more processors than ever packed into a single Chip. [1]. To perform computations, these parts may comprise central processing units, specialised IP cores, memory modules, and input/output controllers. MPSoCs, short for "multiprocessor system on a chip," are the collective term for these integrated devices (CMPs) [2]. When the number of IP cores expands, the capacity of conventional methods for delivering efficient connections is quickly overwhelmed. There needs to be a high-performance interface for moving data between the many IP cores on a

single device. Connectivity can be established in a variety of ways, including point-to-point, bus, carbon nanotube, fibre optic, and network-on-a-chip (NoC). As a solution to these problems, a new paradigm has emerged: Networks on Chip (NoCs) are gradually replacing more conventional means of interconnecting components on a single chip. [3]. NoCs allow for the integration of wide-area networks into on-chip embedded devices (SoCs). Due to the large density of IP cores in modern NoC designs, inter-core communication is often the most pressing issue.. The interaction between these IP cores should be smooth and easy to use. A well-defined system is required to carry out such a communication. The literature has introduced numerous topology kinds. The first step is to decide on a topology. Routers, links, and wrappers are the NoC's three primary building blocks. An essential part of most NoCs is a router or switch. Basic requirements for the router design are the enhancement of performance, small footprint, and low power consumption. The purpose of this research is to develop a router architecture suitable for use in NoCs that can be easily reconfigured. Because of the many moving parts in a router (FIFOs, Arbiters, etc.), it's important to design each part with efficiency in mind. Communication Interfaces, Chip cost, Quality of Service, and Network Flexibility are all addressed by the dynamic reconfiguration architecture for on-chip networks. The suggested architecture adapts to real-time changes in communication conditions and packet size by dynamically configuring individual Hardware Modules like routers, packet-based switches, and data packets. Its architecture allows for both low latency and high data throughput.

II. LITERATURE REVIEW

It's possible to change the network's topology thanks to Network-on-a-Chip (NoC) design. The architecture enables a generic System-on-Chip (SoC) platform with topology adapted to the operating application by supporting both long-interface and direct-interface between IP-cores. In order to work with preexisting NoC routers, the interface is simply installed as a layer between the routers and the wires, making the architecture extremely versatile. By allowing for dynamically reconfigurable routing in a network's topology, networks built with a network-on-a-chip architecture may easily adjust to new conditions and overcome previously insurmountable problems. The performance of a Multi-Processor System on Chip increases with the number of processors it contains and the bandwidth of the medium used to communicate between them.

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This paper proposes a dynamically reconfigurable Network-on-Chip architecture for multiprocessor system reconfiguration. Increased communication requirements, QoS requirements, low power consumption, and network scalability are all factors on chip. As a result of their modular design, networks on chips have the potential to serve as a reliable communication backbone for future developments in the field of heterogeneous dynamic reconfigurable systems.[1]

This paper [2] provides a NoC architecture for networking that permits changes to the topology of the underlying network. The lengthy linkages and direct links between IP-blocks made possible by the architecture make it possible to create a generic System-on-Chip (SoC) platform that adapts its topology to the needs of the application currently running on the chip. Adding a layer of configurability between routers and links makes this design flexible enough to be used with any existing NoC routers. Topology that conserves electricity Topology is established using switches based on physical circuit-switching, such as those found in FPGAs. In order for massive on-chip systems to be organised on-chip and provide the required proportional performance to applications, they provide an effective guiding calculation. There are many benefits to executing systems on-chip utilising table-based switches, such as the ability to adjust steering computations and account for internal failure. Nonetheless, table-based switches have been deemed unattractive for system-on-chip s due to their seemingly excessive area and power utilisation. This research details the area-based steering system, which organises goals into clusters at various system locations to improve the efficiency of execution via rational squares.. You can also look at district-based steering as a way to cut down on the text in your tables of directions. Space-based guiding is universal and can be applied to any adaptable guiding formula. They have evaluated the proposed strategy in relation to a general directing calculation, in particular section-based steering and an application-explicit directing calculation with regular and ad hoc work topologies. We find that for large systems, the number of table rows is drastically reduced. Analysis shows that only four areas are needed for area-based directing to aid in a few steering computations in a 2-dimensional task without reducing the quality of the execution. Our results show that in an 8x8 work setting, district-based leading combined with SR can withstand up to 7 connect failures. In the same way that localization-based steering reduces the area and power distribution of a proportional table-based usage by 8 and 10, respectively, it also reduces the overall consumption of the table. On top of that, when an application-specific directing computation is used in conjunction with a location-based steering mechanism, any corruption in system execution is negligible.[3].

Many-center processors may support a large number of processing threads thanks to a network on-chip (NoC) that grants access to shared resources including main memory and on-chip storage. Locally reasonable mediation in multi-stage NoC, however, can lead to internationally unreasonable access to shared resources and impact framework-level execution depending on the actual locations of the individual jobs. The proposed work is an intervention towards a given administrative equilibrium (EoS) in an arrangement and aid for a task position that is uninformed of its geographic context. To accomplish EOS without stymieing cooperative

authority, we propose combining probabilistic assertion with a distance of a based loads. Yet, due to its complexity, probabilistic mediation frequently causes high-zone and long-idle times, both of which have a deleterious effect on productivity. We suggest a mixture mediator that can switch between a simple referee at a light burden and a complex judge at a heavy burden, reducing the complexity of the requisite equipment. Cross-breed mediators are given more power by the belief that international fairness and public opinion are heavily impacted by intervention. The GPGPU benchmarks and fabricated traffic examples used to evaluate our judgement. Our research demonstrates that a combined cooperative judge and probabilistic distance-based mediator, or "half and half referee," reduces execution variation when assignment situations vary and enhances standard IPC.[4].

SOC's growing reliance on intelligent properties has exposed it to a variety of security holes and continues to create a wide range of new and pressing concerns. In the meantime, the current plans for a billion semiconductor chips present an additional difficulty in amassing a lack-free device due to the aggressive extension on chip thickness and considerable scale of feature size. The proposed unified runtime solution for security and variation to internal disappointment of field-programmable entryway displays (FPGA)-based SoCs makes use of automated imprints, live checking, flexible coordinating, and mid-configuration maintained by an in-house made organisation on a chip called X-Network. X-Network lessens the number of switches needed by managing individual components more efficiently, and more fundamentally, it provides more leeway for change in the face of failure and security threats than conventional networks. We have finished the design and testing of a Xilinx Virtex-6 FPGA development board. Initial tests reveal that this reconfigurable plan with estimation sorts out how to course distributes such faults and passes them near their complaints in a reasonably low latency, even if 20% of the associations in the association are broken. Our setup doesn't attain huge area or a speed corruption in contrast to regular issue receptive techniques, which typically require resource overabundance. As much as 10% of additional question tables' budgets go into the resource overhead of a both security with inadequacy indulgent type. In order to speed up the Rivest algorithm, a multiplexed Montgomery disconnected enlargement design is implemented. Estimation by Shamir Adleman.[5]

There is a proposed NOC embedding for FPGAs that uses a system of level correspondence. One of its many advantages is that it can shorten the time it takes to connect an FPGA's surface to its fast memory ports and I/O. The proposed approach is a hybrid of hard-introduced NOC components that would take up less than one percent of a large FPGA's available space while yet being careful of memory interface and I/O latency. Power consumption is reduced by 14 percent when switches are operated in a firm manner as opposed to a delicate one, and whether a switch is stiff or fragile, most of its power is consumed by its data modules for buffering.

Hard NOCs consume less than six percent of an FPGA's dynamic power budget while supporting 100 GB/s of communication bandwidth. We calculate that, for a hard NOC, the average energy usage per GB of data transported is between 4.5 and 10.4 mJ. This is astonishingly close to the 4.7 mJ/GB needed by the least troublesome standard interconnect for linking points in an FPGA. When compared to cars that are used to being connected, we find that conventional architecture is 4 times less disruptive and uses 23% less energy when deployed via a hard NOC, even though it is only 43% utilised..[6].

Current multiprocessor framework on-chips have a growing problem with power supply noise (MPSystem-on-Chip s). When new models have emerged, such as the system on-chip (, the standard for on-chip correspondence in MPSystem-on-Chip s), it has become easier to maintain constant and energy-productive activities in the present. Due to increasing Network-on-Chip control impact, increasing transistor current, and the fast changing of rational devices, power supply noise in Network-on-Chip control delivery systems is at an all-time high (PDN). This makes it all the more important to safeguard the PDN's power supply against interruptions. IcoNetwork on chiplast, a hybrid of an original stream control convention (PAF) and a versatile steering calculation, is proposed in this research to help bring peace to the Power supply chaos in Network-on-Chip s. (PSN-mindful directing).[7]

Constant testing of the system with Built-in Self-Tests (BIST) is essential for achieving high consistent quality in aon-chip systems, since this allows for faults to be found quickly and the number of affected parcels to be kept to a minimum. Nonetheless, Built-in Self-Tests results in significant performance loss due to data constraints. We suggestEsyTest, a comprehensive testing approach that has low overhead on framework operation. The information way and the control way are subjected to separate testing in EsyTest. The information highway test initiates at random intervals, however the actual test runs during the spare time in the timetable to prevent switch deactivation. To ensure the access to the training facility during testing of the as System-on-Chip switch, a reconfigurable switch design and a flexible flaw tolerant directed computation are presented. All training facilities are operational throughout the system test procedure to ensure consistent performance. As compared to other available test systems, EsyTest's improved equipment comparability and exhaustive test inclusion for the Network-on-chip make it the clear choice. Under the PARSEC benchmark and with varying test frequencies, executing without a coupled test method results in an increase of less than 5% in execution time, 9.9% in space requirements, and 4.6% in power consumption..[8]

While planning out communication structures for a SoC, the NoC Architecture plays a crucial role. The standard vehicle, shared vehicle plan, and cross bar connectivity plan for on-chip associations need to be considered when developing a NoC. Cross-area, torus, and other topologies are used extensively in the design of NoC switches. Despite this, a sizable proportion of designs are unsuccessful in their attempts to address QoS, congestion, cost, chip, and even fundamental concerns like throughput, zone overhead, and slowness. This study aims to make progress towards the

forementioned objectives by developing a hexagonal centre point layout for pack turned Network on Chip (PS-NoC). Using a network design based on a hexagonal central node provides improved correspondence between nodes, eliminates obstruction problems, and allows for traffic-free transmission of packets across on-chip connections. The vast majority of on-chip connections can be dynamically rearranged with our setup. We are employing a need encoder and a Deterministic XY coordinating computation to create a hexagonal focal point. Our proposed architecture expands the level of complexity in on-chip networks. [9]

For an on-chip cor-respondence of a processor with a multi-cognizance display, the most popular network on chip geology is a 2-Dimensional cross segment because of its low arrangement difficulties and great 9 In form to a square processor plan. Yet, it still suffers from some of the chip industry's most pressing issues, such as nearby congestion, which can also arise from va-rious levels of visitors with diverse neighbour groups and is a major issue because it results in both high latency and high power consumption. We identified a novel design of 6-neighbor hexagonal move segment topology to execute on an FPGA to address the aforementioned issues. The connection is expressed in the verilog hdl language, and an attempt was made to use modelsim to ensure realism. Designing has also been done to try and solve some of the major frameworks' agency concerns, such as gridlock and livelock. As well as being finished, it has been tested on contemporary Xilinx FPGAs such the Atrix 7 and Vertex 6 for practical use. A 6-neighbor hexagonal grid topology has been completed, which has less district on chip in comparison to a 4-neighbor 2nd move section, and it is also more productive in its interconnect with the between processor, which could result in a 21% reduction in location, a 17% reduction in average strength, and a 19% reduction in correspondence area between cover centres. By breaking away from the norm of 2D design, this can make a layout more compelling. [10]

Using quad-rail data encoding, this work proposes a low-region-overhead and power-effective unique reasoning semi-deferral heartless sense-speaker half-support strategy. For atypical association on-chip switch designs requiring more space and less power, the proposed quad-rail SAHB technique is put to use. There are three main parts to the quad-rail SAHB plan that has been proposed. In any case, the quad-rail SAHB plans to use just four wires to pick four of the ANoC switch's directions, cutting down on the necessary number of semiconductors and the amount of space they'll need. In addition, the quad-rail SAHB only modifies one of the four wires when multiplying by two bits of data, hence the number of semiconductor switchings and the quantity of dynamic power dissipation are both decreased. Finally, the QDI-compliant quad-rail SAHB allows for a high degree of operational tolerance for fluctuations in PV and T in the intended ANoC switch. We demonstrate a complete 18-switch ANoC design using the suggested quad-rail SAHB while keeping in mind the 65-nm CMOS standard..

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The suggested quad-rail SAHB ANoC switch occupies 32% less space than the two-rail companion and disperses 50% less energy under comparable stunning operational force towards PVT distributions. Compared to the other ANoC switches that have been discovered, the proposed quad-rail SAHB ANoC switch stands out as having exceptional operational strength, the smallest footprint, and the highest efficiency.[11]

Heterogeneous manycore architectures, with their greater computing capabilities, allow for the simultaneous execution of a wide variety of applications. In order to operate numerous applications concurrently, it is necessary to have a communication fabric that is adaptable, fast, and low on energy consumption. The design of modern Network-on-Chip systems (NoCs) is being severely tested by such tight criteria. For effective communication support during concurrent application execution, this study proposes Adapt-NoC, a flexible NoC architecture with a control strategy based on reinforcement learning (RL). Adapt-NoC has the flexibility to dynamically assign a number of sub-NoCs of varying sizes and placements to the many processes that are operating in the NoC all at once. To better suit the performance and energy consumption needs of a certain application, each of the dynamically assigned subNoCs can switch to a different topology, such as a mesh, cmesh, torus, or tree. We also explore the possibility of using RL to develop a command strategy for selecting an appropriate subNoC architecture for a given application. Therefore, Adapt-NoC might not only provide a variety of topologies for simultaneously running applications, but it might also optimise the selection of the optimum topology for a given application in an effort to increase performance and decrease energy consumption. We use both graphical processing unit (GPU) and central processing unit (CPU) benchmarks to evaluate Adapt-NoC. Comparing the simulation findings with those of previous work reveals that the proposed Adapt-NoC can increase NoC energy efficiency by 53%, reduce latency by 34%, and shorten execution times

by 10%[12].

III. METHOD

The suggested router design is based on a four-channel (north, south, east, and west) network with a cross-bar switch. Several sub modules make up the bulk of a reconfigurable network-on-chip module refer Fig 1. The components include a FIFO multiplexer, a crossbar switch, a memory chip, and some on-board circuitry. Digital circuits were employed in earlier designs, however sampling problems and data loss occurred because the source clock was faster than the destination clock. Our solution to this issue is to offer a FIFO with independent write and read clock signals, as well as dedicated input and output ports, implemented as a high-performance parallel interface between clock-domains.

In order to design the whole router, we've made a few of its constituent parts. Find out more about these add-on pieces of software in the next paragraphs. All of the modules' HDL code is written in Verilog, and simulation is performed with MODELSIM. Synthesis is performed using Xilinx ISE Design Suite 13.4. Includes the RTL viewpoint, a detailed description of the circuit's architecture, and an analysis of the circuit's overall power consumption

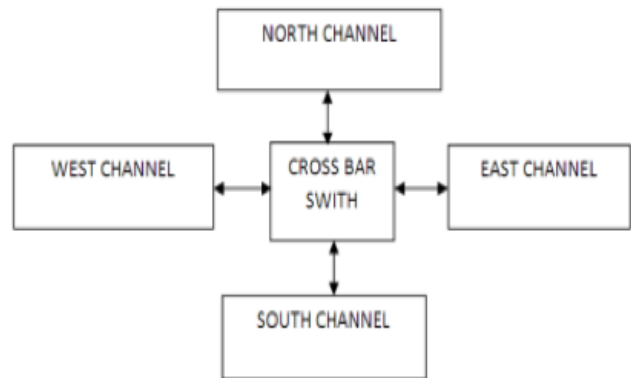


Fig. 1 Router Design which contains four channel and a crossbar switch connects four channel

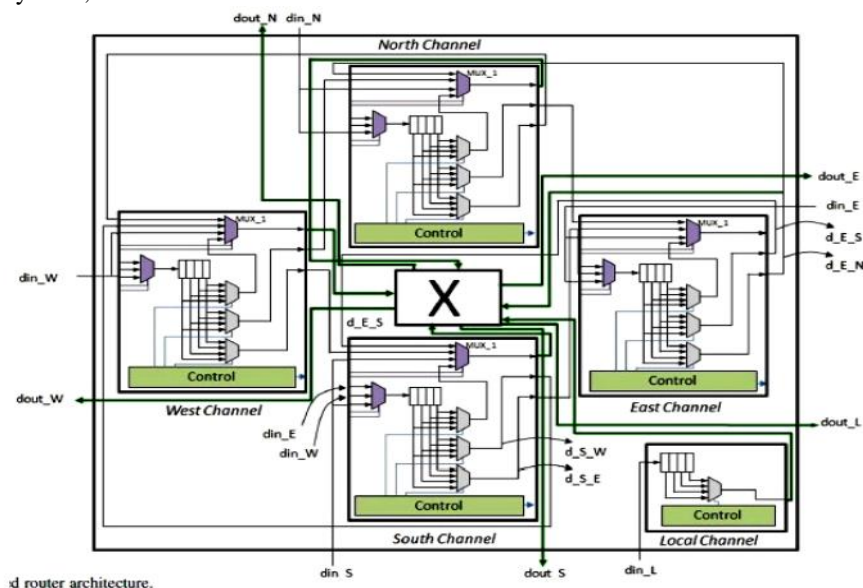


Fig. 2 Router architecture proposed by Matos. Reference [14].

The computerised circuits' source clock was faster than the target clock, resulting in a FIFO operation. An inability to test at source speed, leading to a black hole of missing data needed to solve the problem, was revealed when the team behind the objective and the source clocks failed to sync up. To manage data and maximise its output, each diversion uses first-in, first-out (FIFO) storage and a flexible, modular design. The independent clock and the read/write signal communicate in tandem, making this conceivable. The stacking order of the FIFO cradle is thought of as a multiple of three. means each of its four locations can hold three bits of data Refer Fig 2. Block of Control for Logic Memory Arrays: There are two different justifications for exercising authority in this situation. The FIRST IN FIRST OUT (FIFO) internal memory makes use of a compose control rationale for its composing activities, while the read operations are limited by a read control rationale Refer Fig 3. The synchronisation functions of gears are achieved via the FIFO pad. It's usually finished off as an indirect line, with two indicators.:

I. Read Address Register /Read Pointer

II Write Address Register /Write Pointer

All of the addresses in a FIFO line and the primary memory area are empty at the outset of any check with create. When the size of the memory display is less than or equal to the difference between the read address and the make address from the FIFO pad, the FIFO line is full.

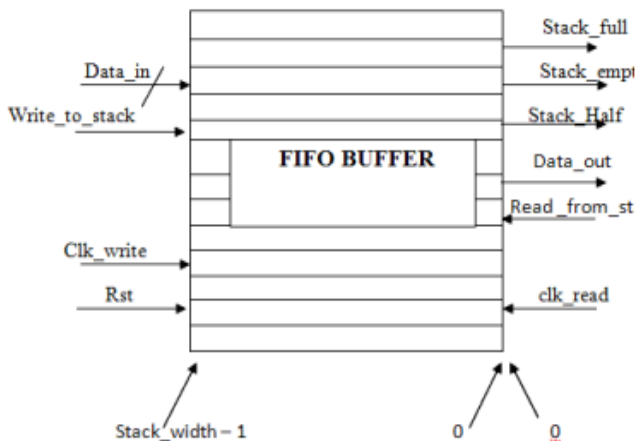


Fig. 3 FIFO buffer unit and Input Output ports. Reference [13]

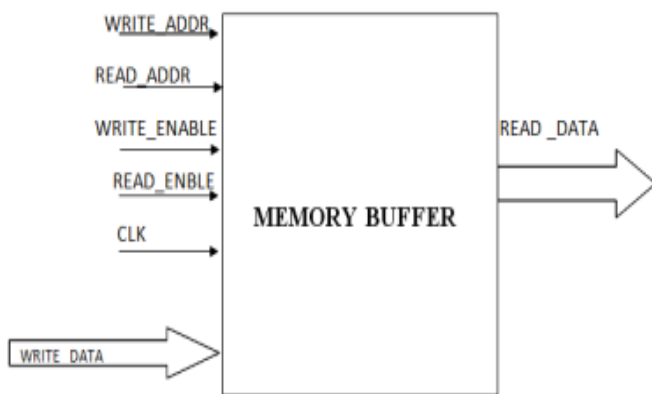


Fig. 4 FIFO buffer unit and Input Output ports. Reference [13]

The memory array control logic block is depicted on top. The FIFO's internal memory write operation is managed by write Control Logic.

A binary pointer to where you can write is created. The memory address pointed to by this pointer is where the incoming data will be stored. The write pointer is advanced by one after every successful write. Moreover, a FIFO full flag and a FIFO almost full flag are generated. Including these signals into your data structure will help prevent any accidental data loss. Like the Write control logic, the Read control logic manages the FIFO's internal memory during read operations Refer Fig 4. A binary-coded read pointer is created to specify the location in memory from which the data is to be retrieved. After each successful read operation, the Read pointer is incremented by one Write and read logic control blocks are shown in figure .5

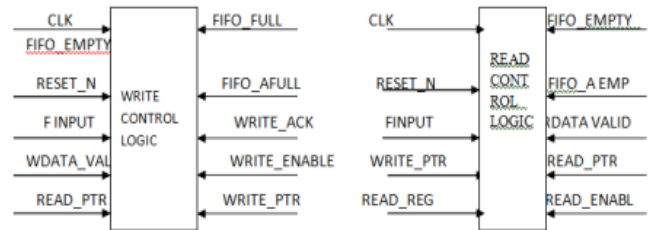


Fig. 5 .Write and read logic control blocks Reference [13]

Plan of Multiplexer: The primary function of a multiplexer is to select one of several possible data bits for output. Two are used to regulate information flow out and in, while the other three manage the FIFO operations of writing and reading. The primary function of a multiplexer design is to multiplex a signal so that it can be routed from a single input to a number of different outputs. The primary function of a selector is to select a signal from a data input and route it to a multiplexed output Refer Fig 5. A four-by-one multiplexer is constructed with a and or invert gate. Cross Bar Switch: power measurements may be taken with the help of the xilinx control analyzer setup device and the switch has the ability to link several inputs to many different outputs. To control the spread of intensity, the power reduction approach is employed. Simple crossbar switching routing is the foundation of the current scheme. To reduce delays and data loss, the suggested work proposes to use the Extended XY Algorithm to replace the standard routing. Verilog Language will be the primary coding language used. The Modelsim software will be used for reproducible functional verification. Cross point switch is another name for the control switch. This mostly does the connecting between various outputs and inputs. For the purposes of this study, a crossbar with five outputs and five inputs is employed to route data between the various ports on the bar. Planned Activities After being implemented in Xilinx ISE, the Xilinx power analyser is utilised to calculate power consumption in the current work. Powergating is also useful for minimising power loss.

Power Analysis using Xilinx Power Analyzer tool (XPA) Xilinx Power Analyzer (XPA) is a design tool used to analyze real design data. After a design has been built in Xilinx ISE, this tool is used to calculate power consumption. The NCD file generated by the Place & Route (PAR) procedure is utilised. Efficiency Enhancement Method with VLSI circuits, power is primarily lost due to leakage currents and dynamic currents. Power gating, an efficient method for reducing leakage power, is employed here.

This method is commonly employed in the design of microprocessors. With packet-switched No Cs, power gating has some subtleties. Full connectivity is needed to ensure that there are paths for every packet when all the nodes are regularly sending messages. This connectivity can be provided by configuring always-on links, while other links may be switched on and off dynamically.

IV. RESULT AND DISCUSSION

Our proposed router design is based on a four-channel (north, south, east, and west) network with a cross-bar switch. As the sub modules make up the bulk of a reconfigurable network-on-chip module.

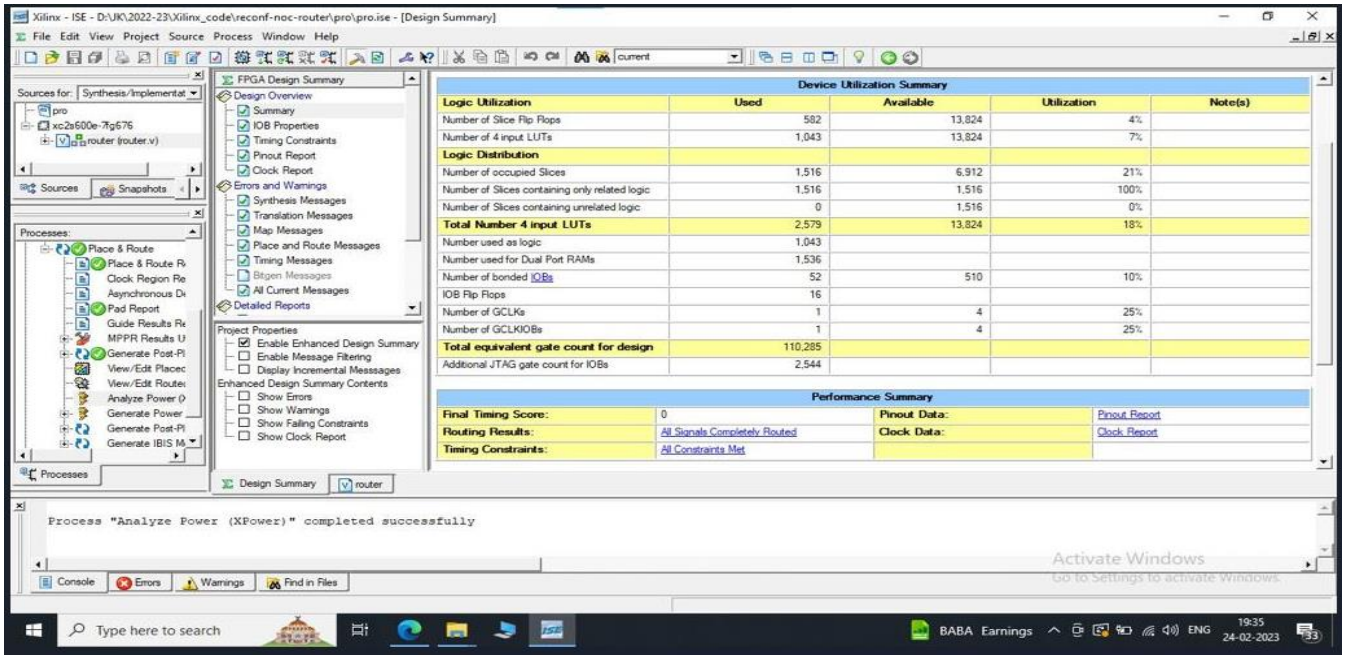


Fig. 6 No of LUTs used by a proposed Router

The components include a FIFO multiplexer, a crossbar switch, a memory chip, and some on-board circuitry and all these components are designed using Verilog code and we use a X Y routing algorithms to design a router architecture all these design are written in Verilog code as the Verilog language is easy to write and debug the errors. This routing algorithm will avoid deadlock and data-loss in the present network. Functional/synthesis verification will be done using Xilinx software, simulation/functional verification is done using Modelsim Refer Fig 6. . All of the modules' HDL code is written in Verilog, and simulation is performed with MODELSIM. Synthesis is performed using Xilinx ISE Design Suite 13.4. Refer Fig 7 Above is the screenshot of the proposed router which consumes the four input LUTs of 1,043 which shows the efficiency of the router in terms of consumption of LUTs

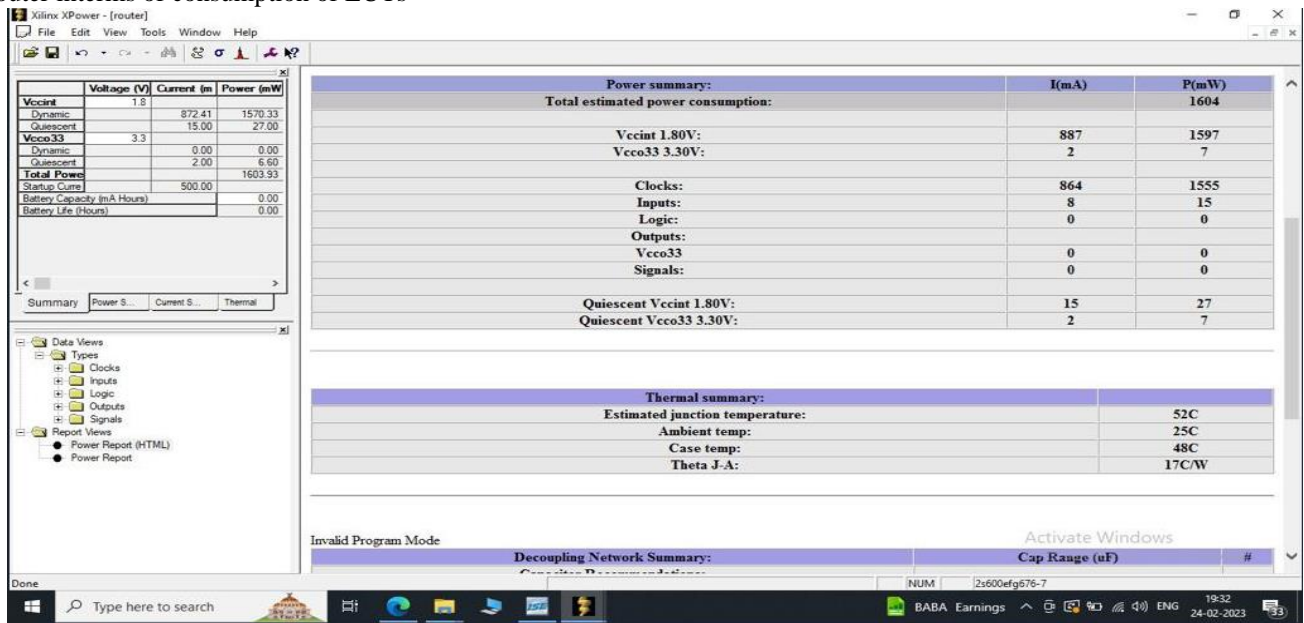


Fig. 7 Power consumed by a proposed Router

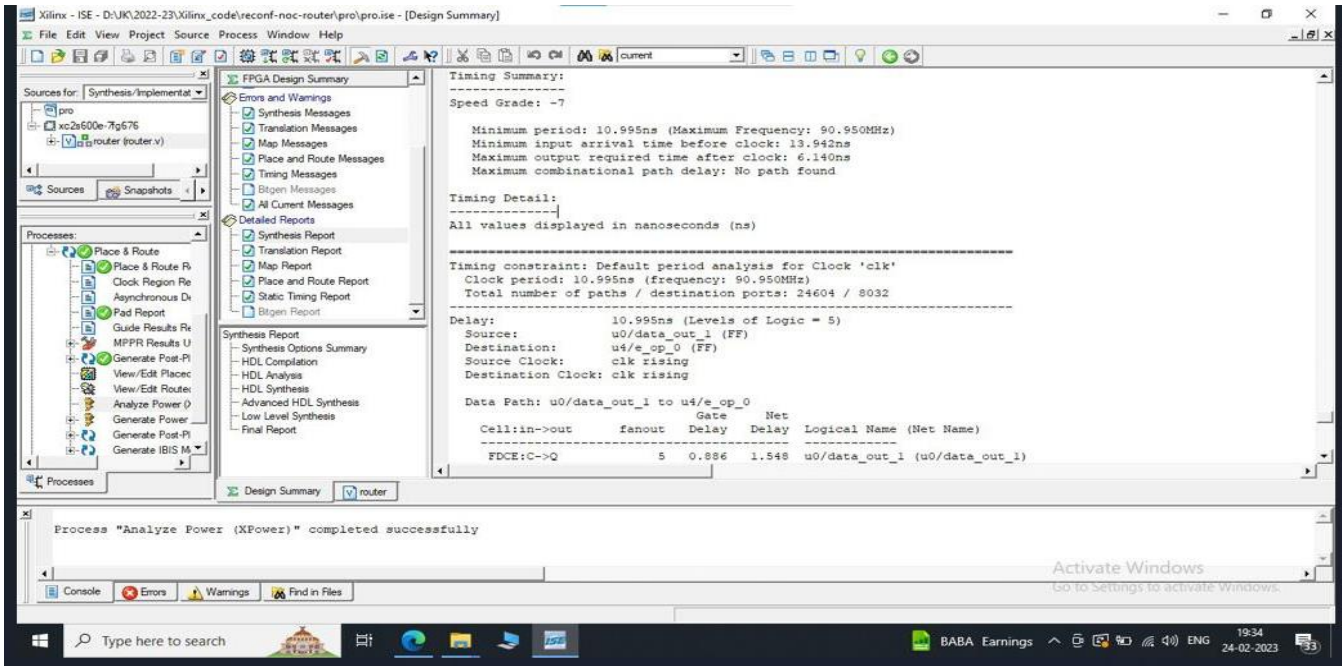


Fig. 8 Speed and Time consumed by a proposed Router

By the above diagram we can say that Power, speed consumed by a proposed Router which is designed using XY algorithm is less when compared to the existing method hence by this we can conclude that proposed router has better efficiency compared to the previous router Refer Fig 8.

Table -I: Comparison Results of Previous Router and Proposed Router

PARAMETERS	PREVIOUS ROUTER	PROPOSED RECONFIGURABLE ROUTER
SLICES	1,865	1,516
LUT'S	3,567	2,579
GATE COUNT	1,44,444	1,10,285
DELAY (ns)	14,136	10,995
POWER(Mw)	1918	1604

V. CONCLUSION

A In this study, we analyse the existing methods for reconfigurable routers on chips, and we design a modified X Y algorithm to achieve low power and high performance, fast communication, low power consumption, and minimal deadlock and data loss along the network's path.

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Conflicts of Interest/ Competing Interests	No conflicts of interest to the best of our knowledge.
Ethical Approval and Consent to Participate	No, the article does not require ethical approval and consent to participate with evidence.
Availability of Data and Material/ Data Access Statement	Not relevant.
Authors Contributions	All authors have equal participation in this article.

REFERENCES

- B. Ahmad, "Dynamically Reconfigurable Network on chip for Reconfigurable MPSoC", IEEE CUSTOM INTEGRATED CIRCUITS CONFERENCE, 2005. [CrossRef]
- Mikkel B. Stensgaard and Jens Sparso, "ReNoC: A Network-on-Chip Architecture with Reconfigurable Topology", Second ACM/IEEE International Symposium on Networks-on-Chip, 2008. [CrossRef]
- Andresmejia, Amurziopalesi, Jos E Fich, Shashikumar"Region-Based Routing: A Mechanism to Support Efficient Routing Algorithms in NETWORK ON CHIPS" IEEE Transactions on Very Large Scale Integration (VLSI) Systems , Volume: 17, Issue: 3, March 2009. [CrossRef]
- Gwangsun Kim, Lee, M.M.-J. , Kim, J., Lee, J.W., Abts, D., Marty, M." Low-Overhead Network-on-Chip Support for Location-Oblivious Task Placement" Computers, IEEE Transactions on Volume: 63 , Issue: 6, 2014 [CrossRef]
- TaimourWehbe; Xiaofang Wang Secure and Dependable NOC-Connected Systems on an FPGA Chip IEEE Transactions on Reliability Year: 2016, Volume: 65, Issue: 4 Pages: 1852 - 1863, IEEE Journals & Magazines [CrossRef]
- Mohamed S. Abdelfattah; Vaughn Betz"Power Analysis of Embedded NOCs on FPGAs and Comparison With Custom Buses"IEEE Transactions on Very Large Scale Integration (VLSI) SystemsYear: 2016, Volume: 24, Issue: 1Pages: 165 - 177, IEEE Journals & Magazines [CrossRef]
- PrabalBasu; Rajesh JayashankaraShridevi; KoushikChakraborty; Sanghamitra Roy "IcoNetwork on chip: Tackling Voltage Noise in the Network on chip Power Supply Through Flow-Control and Routing Algorithms"IEEE Transactions on Very Large Scale Integration (VLSI) Systems,Year: 2017, Volume: 25, [CrossRef]
- JunshiWang ,MasoumehEbrahimi, Letian Huang , XuanXie, Qiang Li , Guangjun Li, and Axel Jantsch "Efficient Design-for-Test Approach for Networks-on-Chip"IEEE Transactions On Computers, Vol. 68, No. 2, February 2019
- Shilpa K Gowda and Dr. Rekha K.R." Performance Analysis of Hexagonal Node Design For Packet-Switched NoC on FPGA"International Journal of Applied Engineering Research 12(13):4004-4008 January 2017
- Shilpa K Gowda, Rekha K R and Nataraj K R. "Design And Implementation of Novel NOC Architecture On FPGA."International Journal of Advanced Research (IJAR)2018



11. Weng-Geng Ho;Kwen-Siong Chong;Kyaw Zwa Lwin Ne;Bah-Hwee Gwee;Joseph S. Chang "Asynchronous-Logic QDI Quad-Rail Sense-Amplifier Half-Buffer Approach for NoC Router Design" IEEE Transactions on Very Large Scale Integration (VLSI) Systems Year: 2018 | Volume: 26, Issue: 1 | Journal Article | Publisher: IEEE Cited by: Papers (1) [[CrossRef](#)]
12. Hao Zheng; Ke Wang; Ahmed Louri "Adapt-NoC: A Flexible Network-on-Chip Design for Heterogeneous Manycore Architectures" IEEE International Symposium on High-Performance Computer Architecture (HPCA) IEEE Xplore: 22 April 2021 [[CrossRef](#)]
13. AmitBhanwala,Mayank Kumar ,YogenderaKumar "FPGA based Design of Low Power Reconfigurable Router for Network on Chip (NoC)"International Conference on Computing, Communication and Automation (ICCCA2015) ISBN:978-1-4799-8890-7/15/\$31.00 ©2015 IEEE 1320
14. D. Matos, C. Concatto, M. Kreutz, F. Kastensmidt, L. Carro and A. Susin, "Reconfigurable routers for low power and high performance," IEEE Transaction on Very Large Scale Integration (VLSI) System, vol. 19, no. 11, pp. 2045-2057, Nov. 2011. [[CrossRef](#)]

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