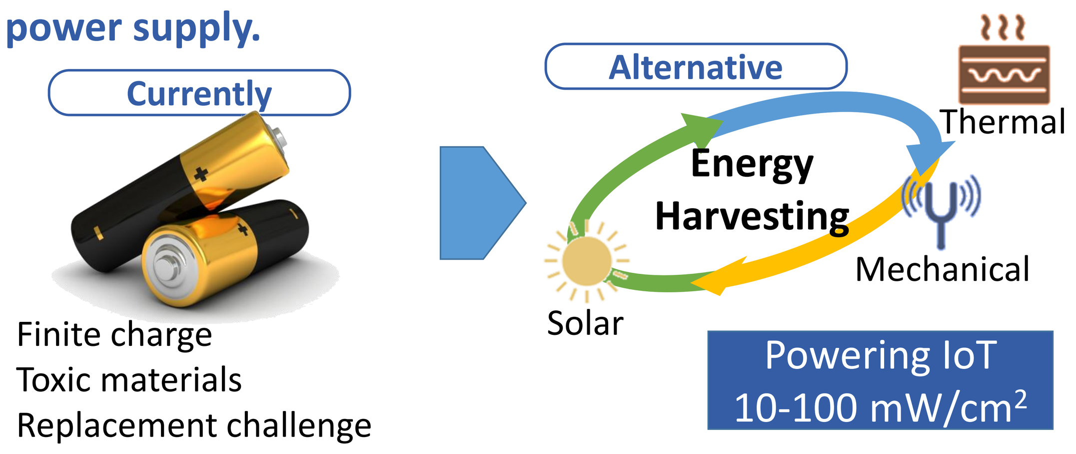
# INTEGRATION OF THIN FILM THERMOELECTRIC OXIDE MATERIAL INTO MICRO THERMOELECTRIC GENERATORS


I. Martin-Fernandez[1], M. Salleras[1], A. Chatterjee[2], A. Rodriguez-Iglesias[1], M. Fernandez-Regulez[1], F. Bauitti[3], A. Morata[3], A. Tarancon[3], N. Pryds[2], L. Abad[1], J. Santander[1], L. Fonseca[1]

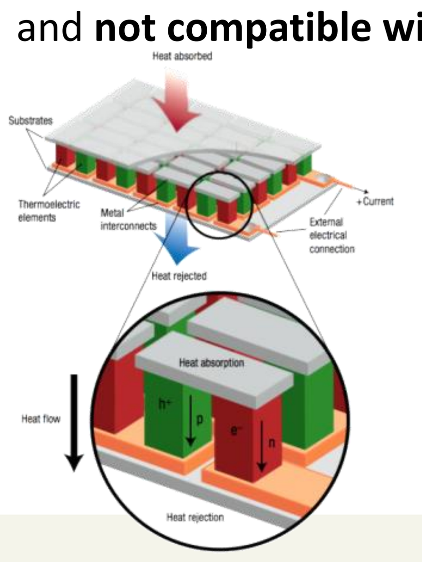
1 Institute of Microelectronics of Barcelona (IMB-CNM-CSIC), Barcelona, Spain.
2 Department of Energy Conversion and Storage, Technical University of Denmark, 2800 Kgs Lyngby, Denmark
3 Catalonia Institute for Energy Research (IREC), Barcelona, Spain
email: inigo.martin@imb-cnm.csic.es


## The challenge

For electronics to become ubiquitous and to fully deploy trillions of autonomous sensors **one of the challenges is the sustainability and the long-term autonomy of their power supply.**



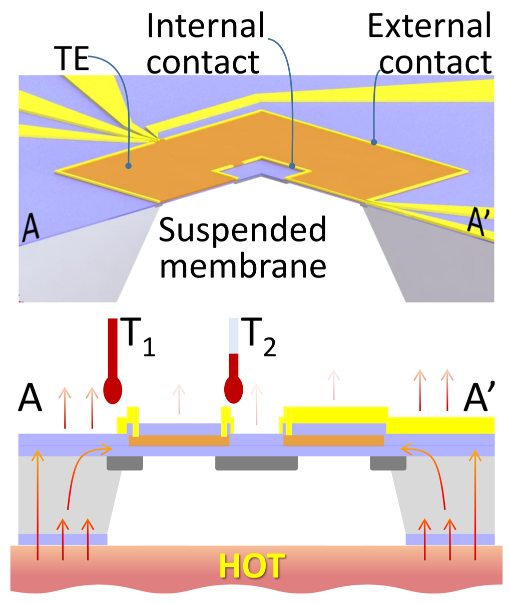

**Thermal harvesting** is attractive but currently **based on scarce and toxic materials** (e.g. $Bi_2Te_3$) and **not compatible with miniaturization**



$$ZT = \frac{S^2 \cdot \sigma}{\kappa} \cdot T$$

σ, electrical conductivity
K, thermal conductivity
S, Seebeck coefficient
T, temperature

## Our approach

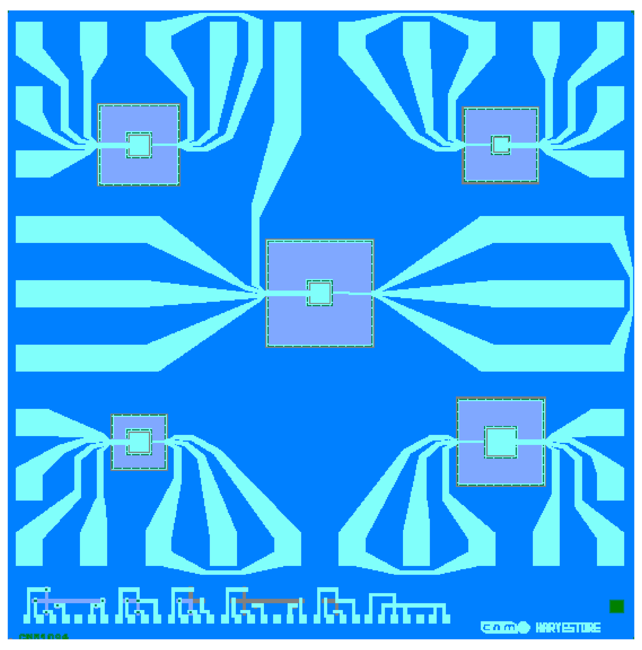


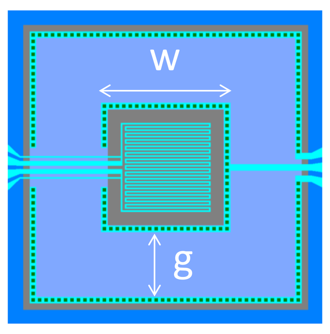

**Planar microthermoelectric generators** (μTEG) based on Si-compatible TE oxide thin films

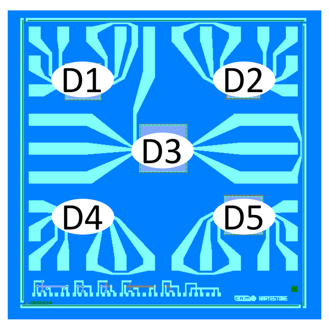
→ TE oxide materials (environmental friendliness)
→ Thin film technology (less critical raw materials)
→ Si (MEMS) technology (scalability, large production)

ΔT develops laterally between the bulk Si and the inner of the membrane

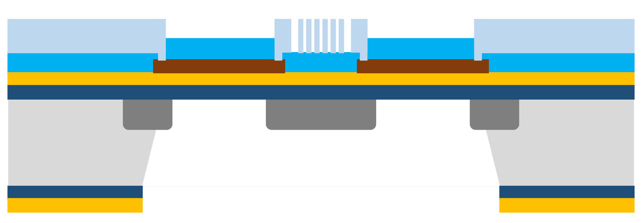
## Device Technology



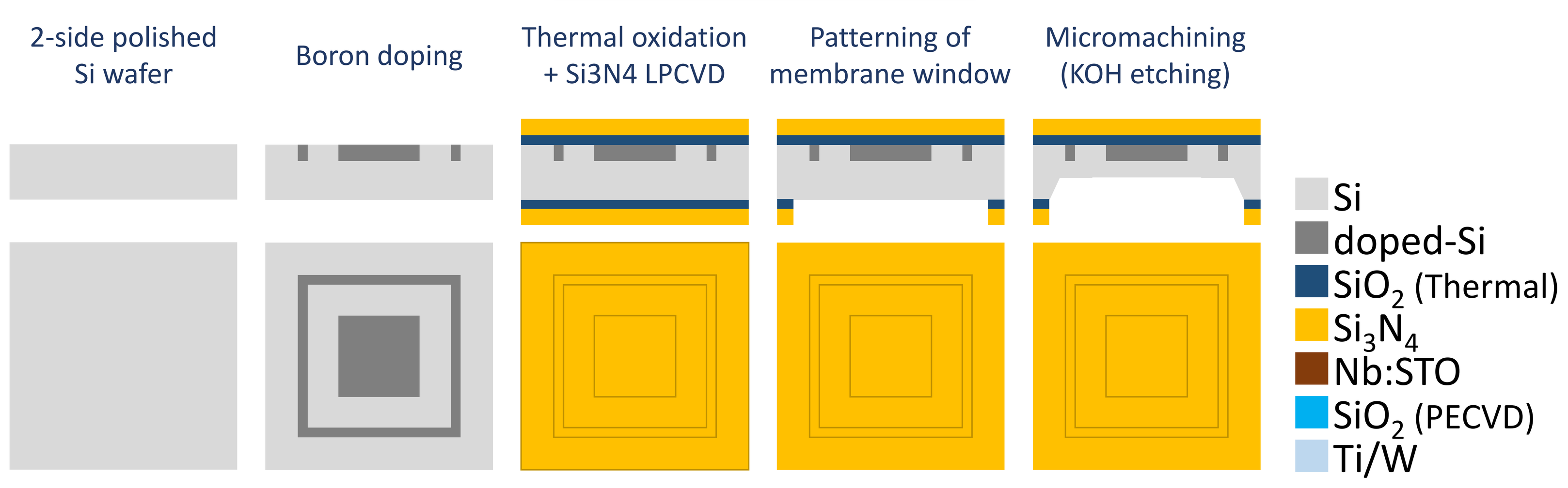


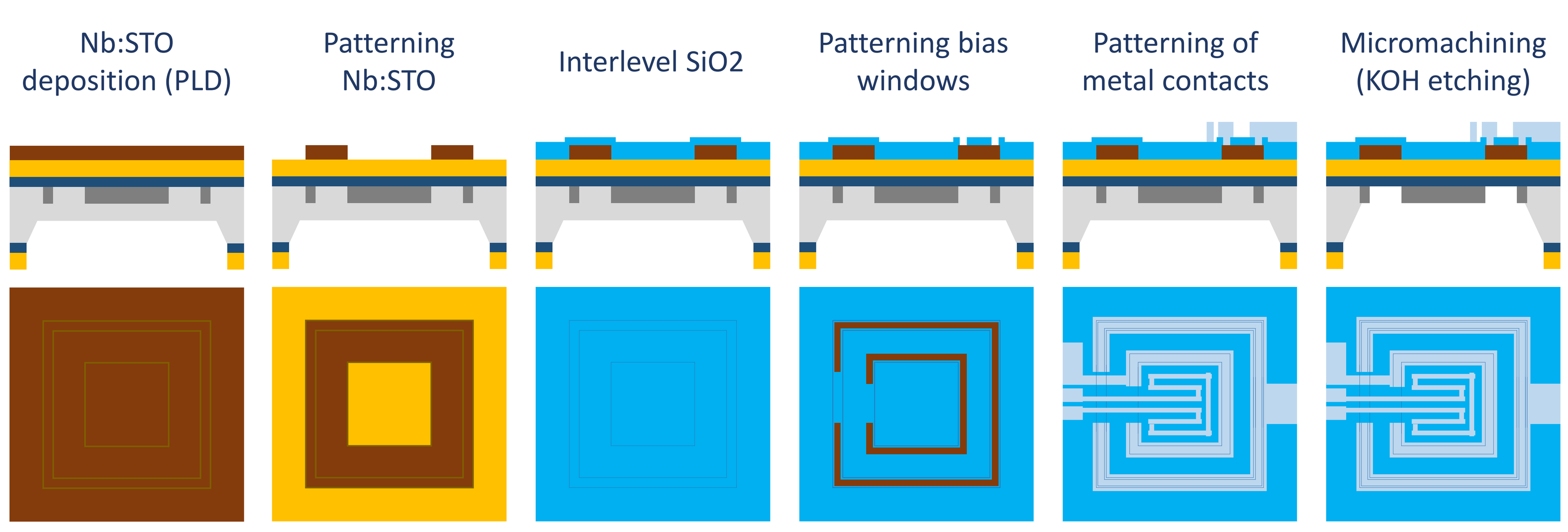




| | D1 | D2 | D3 | D4 | D5 |
|---|---|---|---|---|---|
| w (μm) | 400 | 300 | 400 | 400 | 500 |
| g (μm) | 400 | 400 | 600 | 200 | 400 |
| A (cm²) | $1.44\cdot10^{-2}$ | $1.21\cdot10^{-2}$ | $2.56\cdot10^{-2}$ | $6.4\cdot10^{-3}$ | $1.69\cdot10^{-2}$ |



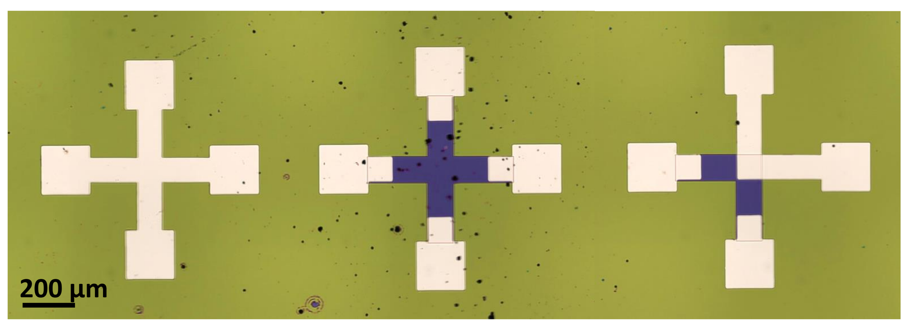
The fabrication of the chips is completed in two 2 phases




## Results

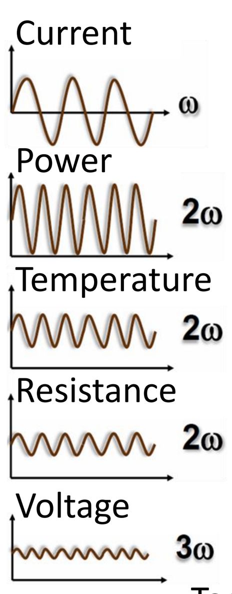
### Electrical tests:



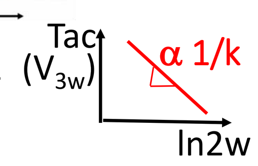

IV characterization of metal layers and Nb:STO with van der Pauw and Kelvin test structures

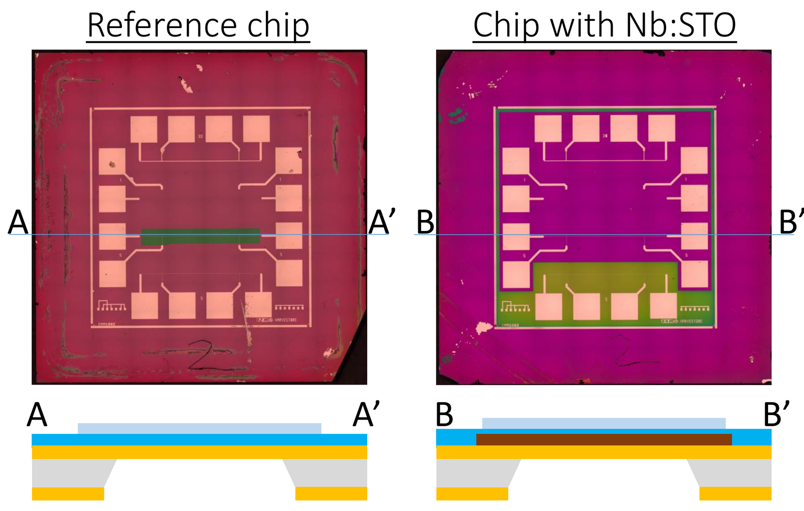
| | |
|---|---|
| $R_s$ metal | 1.3 Ω/□ |
| $R_s$ Nb:STO | 52 +/-3 kΩ/□ |
| $R_c$ metal-STO | 1,9 +/- 0,2 kΩ |

### Thermal characterization - 3ω-Völklein measurement

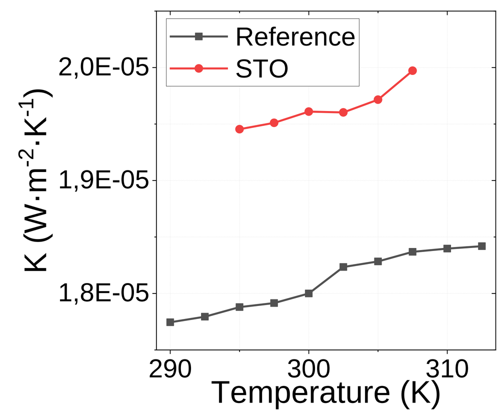



$$G = \frac{P}{\Delta T_{2\omega}}$$




| | Reference chip | Chip with STO |
|---|---|---|
| STO thickness | n/a | 25,5 nm |
| Membrane width | 757 μm | 689 μm |
| Contact distance | 3500 μm | 3500 μm |

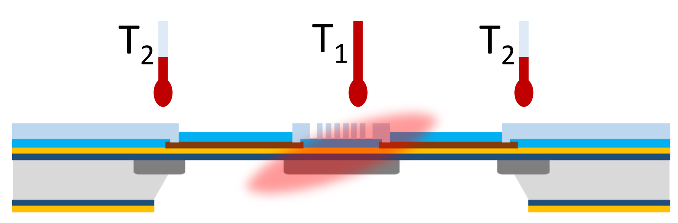


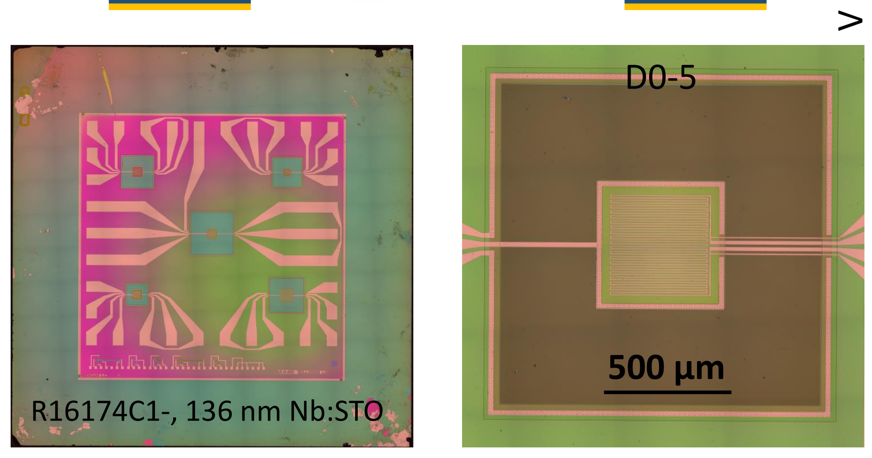

@300K

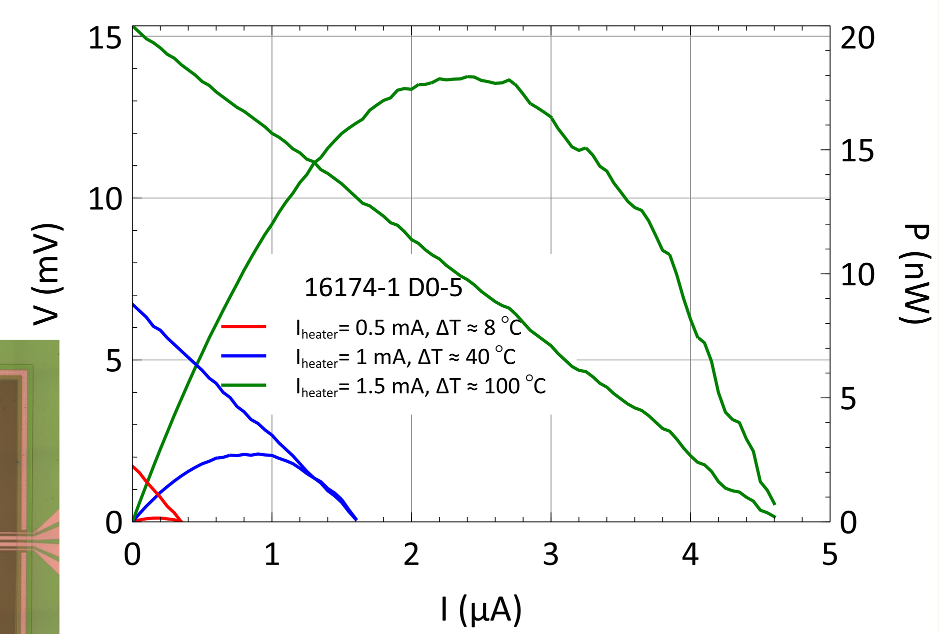
$k_{(mem)}$= **1,378** $W\cdot m^{-1}\cdot K^{-1}$
$k_{(STO(25nm))}$= **3,118** $W\cdot m^{-1}\cdot K^{-1}$

### Output and Seebeck coefficient (S)

Devices tested in "test mode"




@ ΔT ~ 100°C

$P_{MAX}$ = 18 nW (1.1 nW/cm²)
Seebeck ~ 155 μV/K

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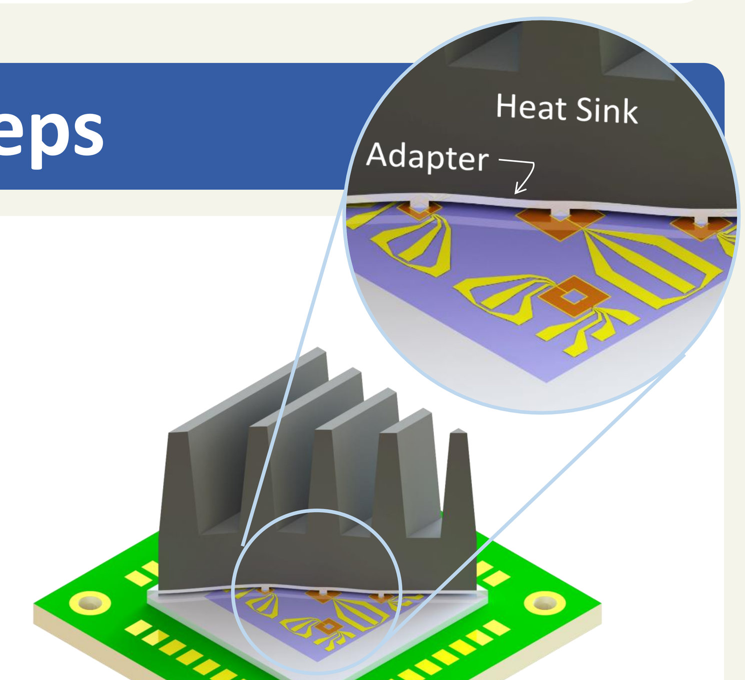
## Conclusions and next steps

- **The deposition and patterning Nb:STO thin films has been made compatible with Si (MEMS) technologies.**
- Different chips have been designed and fabricated to test the characteristics of the **Nb:STO thin films for thermal harvesting.**

- **Full characterization of optimised Nb:STO thin films are ongoing.**




## Acknowledgements


**HARVESTORE project** (grant agreement No 824072) funded by the European Union's Horizon 2020 research and innovation programme

Generalitat de Catalunya
AGAUR
(2021 SGR 00497)