

Fabrication of local areas of high aspect ratio silicon structures using metal-assisted chemical etching - MACE

A technology platform for the creation of 3D templates

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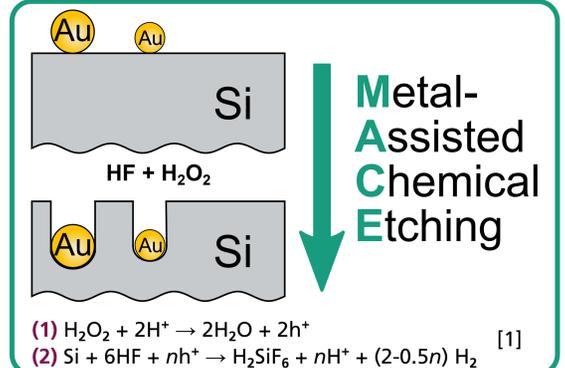


Background

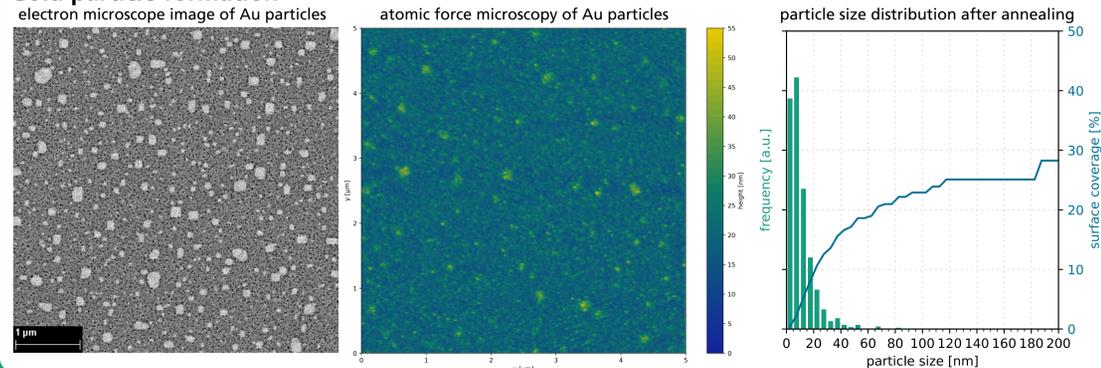
The ongoing miniaturisation of integrated devices comes along with the demand of smaller feature scales in combination with an increasing aspect ratio. 3D structures can be fabricated by a bottom-up approach to omit cost intensive high precision lithography processes. Here, we present a technology to fabricate integrated 3D silicon structures with high aspect ratios using metal-assisted chemical etching (MACE).^[1]

MACE is a wet etching process which uses a noble metal - like gold - to selectively etch silicon at the metal-silicon interface. Silicon is etched in a solution of aqueous hydrofluoric acid (HF) and hydrogen peroxide (H₂O₂) in the presence of gold.

H₂O₂ is reduced at the noble metal interface within the acidic solution generating electron vacancies h⁺ (1). The parameter *n* depicts the number of involved electrons. Two mechanisms may occur (2): *n*=2, the pore formation with direct silicon etching, *n*=4, the electropolishing: Si will be oxidised to SiO₂, which is etched by HF.^[1]



Gold particle formation

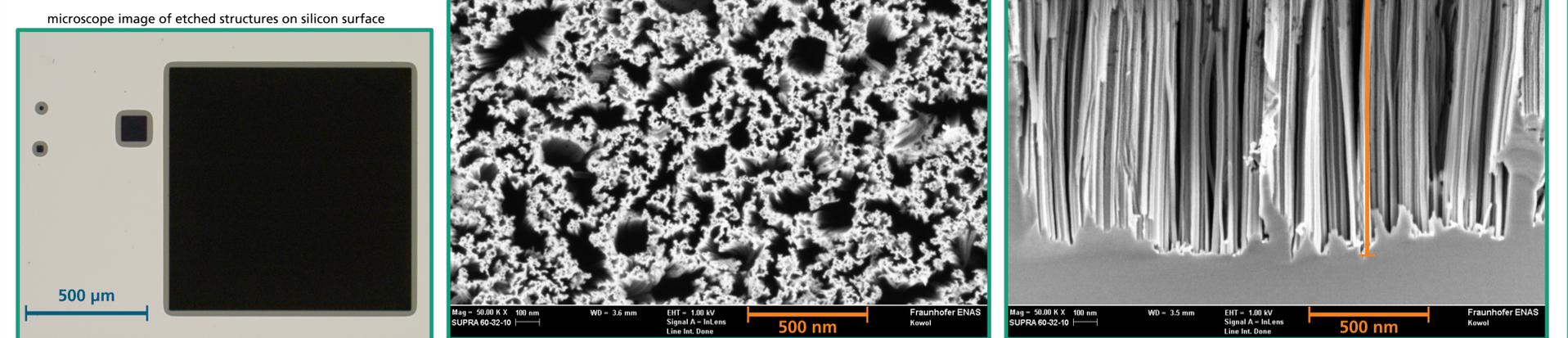


Experimental

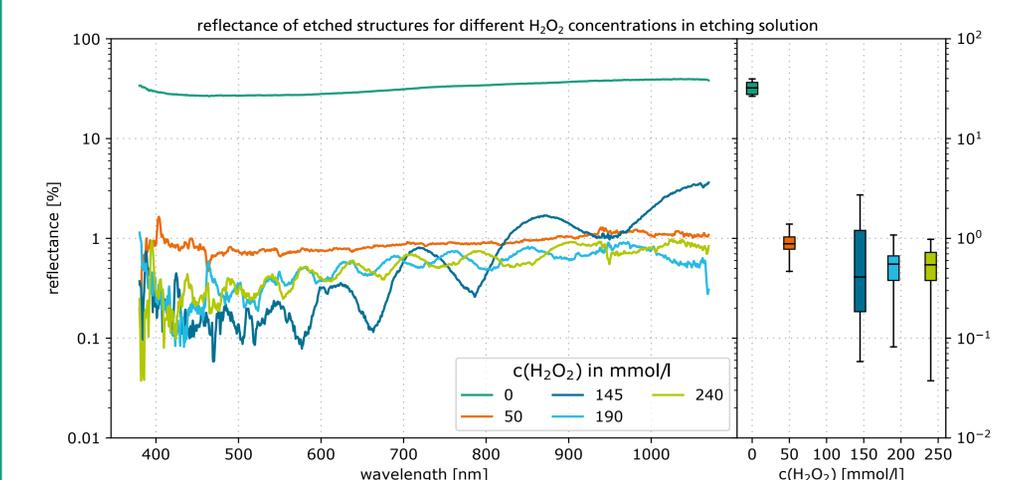
- p-doped 150 mm Si wafers coated with 5 nm Au
- annealing at 300 °C for 30 min for particle formation
- parylene C pattern as masking layer - rectangular testing fields
- wet etching in HF:H₂O₂:H₂O
 - HF concentration: 1.7 mol/L
 - H₂O₂ concentration: 0, 50, 145, 190, 240 mmol/L
 - etching time: 10 min
- analysis with scanning electron microscopy, atomic force microscopy, optical microscopy, and spectral reflectometry

Etched silicon

- 3D structures created in defined areas
- Au particles remain at bottom of trenches
- surface of etched area dark: black silicon.



black silicon - reflectance



Conclusion

Here, we successfully demonstrated a low-cost bottom-up approach for the fabrication of 3D silicon structures with high aspect ratios on wafer-level.

The wet etching process using self-assembled Au nano-particles resulted in local areas with black silicon structures. The 10 min wet etching process resulted in an etching depth of 1.2 to 1.7 µm. The resulting structures are mainly vertical pillars and ribbons with typical wall sizes of ≈ 20 nm. The special geometry creates a high absorbance for visible light. This results in a reflectance of below 1% for a wide wavelength range.

This gives a technology platform for a local integration of 3D structures on chip level. These templates can be further functionalised for capacitors, gas sensors, radiation sensors and so on.

Acknowledgements

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[1] M. Franz, R. Junghans, P. Schmitt, A. Szeghalmi, and S. E. Schulz, "Wafer-level integration of self-aligned high aspect ratio silicon 3D structures using the MACE method with Au, Pd, Pt, Cu, and Ir," Beilstein J. Nanotechnol., vol. 11, pp. 1439–1449, Sep. 2020, doi: 10.3762/bjnano.11.128.