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Turbo encoder and decoder chip design and FPGA device analysis for communication system

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ABSTRACT

Turbo codes are error-correcting codes with performance that is close to the Shannon theoretical limit (SHA). The motivation for using turbo codes is that the codes are an appealing mix of a random appearance on the channel and a physically realizable decoding structure. The communication systems have the problem of latency, fast switching, and reliable data transfer. The objective of the research paper is to design and turbo encoder and decoder hardware chip and analyze its performance. Two convolutional codes are concatenated concurrently and detached by an interleaver or permuter in the turbo encoder. The expected data from the channel is interpreted iteratively using the two related decoders. The soft (probabilistic) data about an individual bit of the decoded structure is passed in each cycle from one elementary decoder to the next, and this information is updated regularly. The performance of the chip is also verified using the maximum a posteriori (MAP) method in the decoder chip. The performance of field-programmable gate array (FPGA) hardware is evaluated using hardware and timing parameters extracted from Xilinx ISE 14.7. The parallel concatenation offers a better global rate for the same component code performance, and reduced delay, low hardware complexity, and higher frequency support.

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1. INTRODUCTION

In the present telecommunication systems, the transmission of data at high speed, voice quality, and expansion of broadband services are the most challenging areas for improvement. Thus, the evolution of technology from the first generation to the third, third to fourth, and now the fifth generation has experienced a dynamic change in data transmission rate [1]. Another important aspect of any wireless communication system [2] is its reliable data transmission means data transmission and reception should be of the same quality. During transmission, the data is subjected to noise or distortion when transmitted via the channel. The noise corrupts the data [3] due to which failure in data transmission occurs. Therefore, error detection and error correction [4] play an important role in data communication. For this purpose, different channel coding techniques are used. Some of these coding methods are low density parity check (LDPC), convolution, polar, and turbo codes [5]. The performance of these codes can be analyzed by their performance in expressions of bit error rate, complexity, functionality, and hardware device utilization. In the late 1940s, a researcher named Shannon gave a concept describing the theoretical limit [6] of maximum capacity for data transmission in any communication channel. This channel capacity limit has now become

the goal for any communication system. To better understand the need for this theoretical limit, the modern mobile industry can be considered. As the number of users is emergent enormously day by day the need and the complexity of the application are also increasing? For example, earlier mobile phones were only used for making calls or text messages but now we can access multiple features like sending pictures, and videos, and using the internet. This technological advancement demands a higher data rate.

As the number of consumers are emergent to access the existing channel different multiplexing techniques are used such as frequency division multiple access (FDMA), time division multiple access (TDMA), and code division multiple access (CDMA). However, these techniques do not increase the rate of data transmission. To increase the data rate one way is to increase the bandwidth of the passage but this reduces the number of available channels thus, this method does not solve the problem. Another way to increase the data rate is by improving the coding scheme so that the existing channel can be utilized to its full strength. This allows more channels to accommodate a particular range of bandwidth. As shown by Berrou [2] in his research work where a new category of code was introduced that performs close to Shannon's limit [6]. The proposed work stated turbo codes based on an iterative decoding scheme. Turbo encoder consists of two convolution encoders connected in equivalent and detached by an interleaver. Moreover, the receiver consists of the serial concatenation of convolution decoders. These decoders use the data from the previous decoder for the error-controlling process. The whole iteration process can be repeatedly run for one received codeword until further improvement. For the iterative decoding mechanism, two algorithms are present: the soft output viterbi algorithm (SOVA) and the maximum a posteriori probability (MAP) algorithm [7]. Earlier application-specific integrated circuits (ASICs) were considered the standard structure for implementing wireless transmitters and receivers. For multiple wireless standards, devices require separate ASICs for each wireless standard which makes the circuit more complex, costly, and power-consuming. The wireless standards have limited use of fixed ASIC and demand a new flexible architecture. The flexible architectures share hardware for common wireless standard features. Therefore, constraints like reduced chip area, complexity, and low power consumption can be optimized while using flexible architecture.

Various reconfigurable architectures, such as field-programmable gate array (FPGA) [8] are now available with user-programmable logic blocks that may be altered based on the requirements or applications. These architectures are attractive solutions to get the desired functionality with relatively high flexibility. The error correction method [9] is incorporated into a wireless communication system for reliable data transmission in channels subjective to noise. The encoding of the input data structure is done by the transmitter based on a particular encoding scheme. This encoding adds some redundant bits/data in the data sequence and at the receiver end, these encoded bits are separated for reliable detection of the data sequence. In any wireless channel whenever data bits are transmitted, they are subjective to the noise that causes the error. Forward error correction codes can be used to detect and rectify this problem. This work is accomplished by encoders such as convolution or block codes, which add redundant bits to the data sequence. If an error occurs during transmission, the decoder detects it and corrects it at the receiver.

Turbo codes were presented in 1993 as a new type of error correction code. These codes are made up of two or more recursive systematic convolutional encoders [10] coupled in equivalent and detached by an interleaver. Turbo codes perform better in relation to bit error rate (BER) than convolution codes because of their concatenation structure and iterative decoding method. Turbo codes are used in existing wireless protocols such as long term evolution (LTE), universal mobile telecommunication system (UMTS), and high-speed downlink packet access (HSDPA). A binary turbo encoder with two recursive convolution encoders is shown in Figure 1. Two parity bits are generated for each message bit given to the turbo encoder. The production of the turbo encoder is the interleaved version of input bits. An interleaver is employed because consecutively transmitted bits can be influenced by faulty bits. The production of the turbo encoder is comprised of parity bits produced by recursive convolution encoder-1 (RSE-1) and recursive convolution encoder-2 (RSE-2). A systematic frame and a parity frame are generated by two convolution encoders. The feedforward polynomial ($1+m+m^3$) is generated by RSE-1 and feedback generator polynomial ($1+m^2+m^3$) is generated by RSE-2. The value of the code rate for each encoder is R=1/3, and the length of the sequence is 3N bits. A state diagram with (n=8) is considered for the turbo encoder as revealed in Figure 2. Initially the state of the turbo encoder is (S_0='0') and S(n) ϵ {0, 1… 7} are the subsequent states for S(n) ϵ {0, 1} message bit. The states are S_0(000), S_1(001), S_2(010), S_3(011), S_4(100), S_5(101), S_6(110), and S_7(111) corresponding to binary message inputs (d_i=0, d_i=1).

The interleaver is the main block in the turbo encoding and decoding process. Due to the interleaving process burst errors in consecutive bits are spread over the transmitted sequence. Thus, bit error rate performance is improved as the bits are reordered in some pseudo-random manner. Another process is puncturing, which increases the code rate by removing the coded parity bits of the sequence thus, making the channel utilization efficient. The interleaver in the turbo encoder structure generates a long data block by reshuffling the data and the interleaver in the decoder structure corrects the errors by bypassing the data to the first decoder. After this process, the interleaver further reshuffles the firstly decoded data and once

shuffling is done passes the data to the second decoder for remaining error corrections. The same way process is repeated.

The organization of the manuscript is as follows. Section 2 offerings the related work with the identification of the gaps, problem statement, and originality. Section 3 offerings the proposed method. Section 4 details the methodology and implementation strategy followed by parallel decoding and interleaving design architecture. Section 5 offerings the results and deliberations part with the possible simulation test inputs and analysis for the FPGA parameters followed by conclusions in section 6.

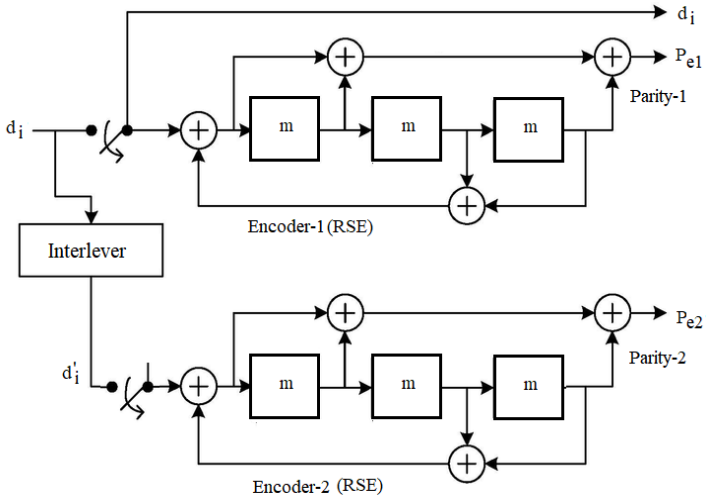

Figure 1. Turbo encoder [11]

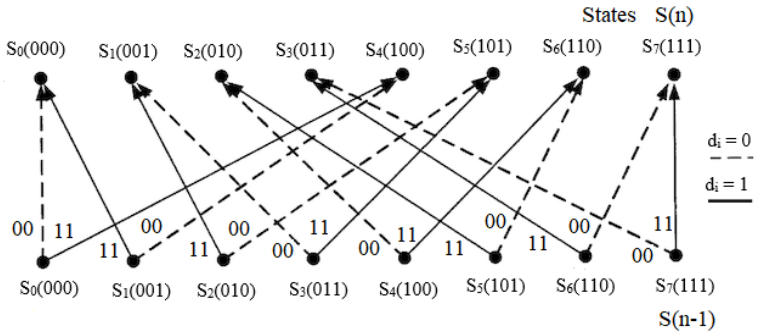

Figure 2. Trellis diagram configuration [11]

2. RELATED WORK

Turbo codes are used in 4G mobile infrastructures as well as in deep-space satellite communications and other applications where inventors want to achieve dependable data transmission over bandwidth-or latency-inhibited transmission links in the existence of data-corrupting noise. The hardware application of a serial turbo decoder architecture [12] was done on FPGA for LTE and worldwide interoperability for microwave access (Wi-MAX) communication system. An interleaver memory (ILM) was used for LTE systems that utilized comparators and subtractors instead of multipliers and dividers. This unique interleaver overcomes the need for memory utilization as compared to the parallel architecture approach. The algorithm was proposed for the scheme of the interleaver [13] for turbo decoder architecture. The error correction performance, as well as latency, was improved in comparison to the sequential decoder by the integration of the algorithm. The algorithm involves the parallel architecture structure which is highly efficient in relations of area, and BER thus, improving the throughput respectively.

Very high-speed integrated circuit hardware description language (VHDL) was used for the application of different error control coding [14] encoders and decoders on FPGA. The error control codes is

an important area of discussion in telecommunication scenario since it provides efficient ways of error correction and error detection. The analysis of different channel coding schemes [15] was proposed for the fifth-generation (5G) mobile system based on binary phase-shift keying (BPSK) modulation over Additive white Gaussian noise (AWGN) channels such as polar, turbo, and low-density parity-check (LDPC). In terms of computational complexity, polar codes proved to be the best of all. A turbo decoder architecture was presented based on the log MAP algorithm [16] using a parallel processor to meet the requirements of long-term evolution communication standards. It is observed that this structure gives better performance in relation to BER. The synthesis results show the device utilization such as the count values of slices and 4 input lookup tables (LUTs) is less using this algorithm, making the design cost-effective. Based on the study and discussion on the forward error correction schemes [17] such as turbo codes and conventional coding, it is observed that turbo codes depict the best theoretical bound in terms of efficiency and channel capacity. In recent times these codes are preferred in several applications such as CDMA-2000 and 3G cellular networks such as UMTS.

The log-MAP algorithm was used for turbo decoding [18] in the Wi-Max communication system. The lookup table (LUT) based log-MAP algorithm was proposed for turbo decoder structure in LTE wireless communication system [19] that reduces the logic resource utilization by 15% in comparison to the conventional design approach. The implementation of a concurrent turbo decoder [20] with an inverse address originator scheme was proposed for future broadcasting communication systems. This address-generation scheme reduces the iteration processing time which further reduces latency. Xilinx integrated logic analyzer (ILA) tool is used to check the validity of the turbo decoder, block error rate (BLER), and latency. A new design approach for the realization of a turbo decoder on [21] FPGA with a reverse address generator to reduce the complexity and latency.

To reduce memory issues a contention-free interleaver is designed and a clock gating technique is used to improve power dissipation. The turbo decoder base was proposed to get high throughput. This was achieved using a processor in which the algorithm has accelerator units and highly controlled software. As the need for configurable memory interfacing is required memory interfacing with a switch fuse unit is used instead of fixed memory interfacing. The parallel decoder [22] based on configurable interleaved networking was used for a long-term evolution standard. A multi-parallelism interleaver approach [23] was designed to reduce computational complexity. The performance loss due to parallel structure is compensated using path metrics [24]. The proposed design is a competitive solution to recent work in terms of high reliability and efficiency.

The related work presents the turbo decoder design and FPGA implementation with different aspects. They have implemented the LTE turbo decoder with the Max log-MAP technique on Virtex-6 XC6VLX75T with a clock frequency of 270 MHz, the number of slices 4108, and LUTs 6310. The work is also done on the VHDL-based design to implement a turbo decoder with a log-MAP technique that follows the decoding iterations but not analyzed FPGA resource utilization. The performance of the turbo codec is also estimated with the log-MAP algorithm on central processing unit (CPU) and FPGA and further utilization of the FPGA for LTE. The work is not done on the latest FPGA that provides fast switching, minimum FPGA hardware parameters utilization, memory, and delay. The problem declaration of the study is to analyze the performance of the hardware chip design of the turbo encoder and decoder based on simple architecture by the integration of the log-MAP algorithm in the same chip, perform the Xilinx simulation for the data verification, and compare the chip design performance on latest supporting FPGA with hardware and timing parameters. The originality of the work is that the encoder and decoder design supports greater frequency with optimal timing and hardware FPGA resources.

3. PROPOSED ALGORITHM

The decoder structure is a parallel concatenated arrangement of convolution codes that takes the independent set of parity bits. After a systematic bit sequence is formed this process is known as the iterative decoding method [25]. The iterative decoding mechanism and the configuration of the turbo decoder are shown with the help of Figure 3 and Figure 4. The information or the message bits are processed between soft input and soft-output (SISO)-1 to SISO-2. Extrinsic information generated by SISO-1 is de-interleaved and fed as input to the next SISO-2. This building block calculates the forward matrix value (α), backward matrix value (β), and the output SISO matrix [5]. To calculate α and β values the Bahl, Cocke, Jelinek, and Raviv (BCJR) algorithm is applied. The SISO decoders perform the turbo decoding process and are referred to as a log-likelihood ratio (LLR) [26]. For the encoded sequence, $d_i = [d_1, d_2 \ldots d_N]$, and generated codeword against each sequence $d_i = [d_1, d_2 \ldots d_N]$, the LLR is articulated as (1).

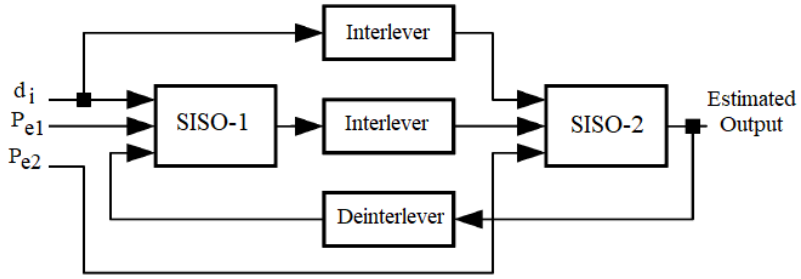

Figure 3. Turbo decoding [5]

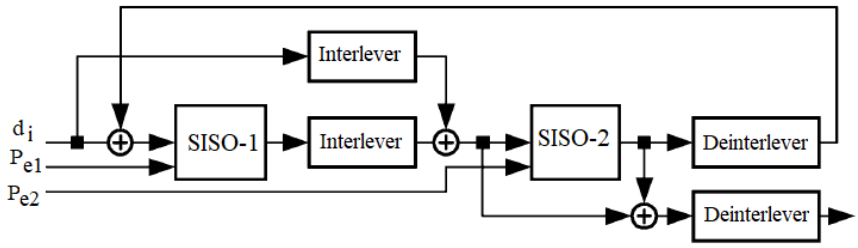

Figure 4. Iterative turbo decoding [26]

$$L(d_i) = \ln \frac{P(d_i=1)}{P(d_i=0)} \quad (1)$$

For the decoded sequence h=[h_1, h_2…h_N],

$$L(d_i|h) = \ln \frac{P(d_i=1|h)}{P(d_i=0|h)} \quad (2)$$

Bahl *et al*. [1] discussed the MAP algorithm in 1974, which was applied to breed the probabilities of individual bits and descend the extrinsic information. The LLR of the k[th] symbol is given as (3).

$$L(d_k|h) = ln \frac{\sum_{d_k=1} \alpha'_{k-1}(s_{k-1}) \gamma'_k(s_{k-1},s_k) \beta'_k(s_k)}{\sum_{d_k=0} \alpha'_{k-1}(s_{k-1}) \gamma'_k(s_{k-1},s_k) \beta'_k(s_k)} \quad (3)$$

In the (3):
α'_k =Forward state matric
β'_k=Backward state matric
γ'_k=Branch matric
s_k=Trellis diagram states at the time 'k'

The MAP algorithm [26] comprises addition processes and multiplication processes. For a large classification, the logarithm and estimate are applied, and the (3) for Max log-MAP is specified as (4).

$$\ln(\sum e^{g_i}) \approx maximum\ (g_i) \quad (4)$$

Then the algorithm is streamlined to the (5).

$$L(d_k|h) = max_{d_k=1}(\alpha_{k-1}\ \gamma_k(s_{k-1},s_k)\ \beta_k\ (s_k)) - max_{d_k=0}(\alpha_{k-1}\ \gamma_k(s_{k-1},s_k)\ \beta_k\ (s_k)) \quad (5)$$

The expression has addition operations and association operations. The state matrix is similarly condensed and written as (6) and (7).

$$\alpha_k\ (s_k) = \ln(\alpha'_k\ (s_k)) = maximum\ \left(\alpha_{k-1}(s_{k-1}) + \gamma_{k-1}(s_{k-1})\right) \quad (6)$$

$$\beta_k\,(s_k) = \ln(\beta'_k\,(s_k)) = maximum\ \left(\beta_{k-1}(s_{k-1}) + \gamma_{k-1}(s_{k-1})\right) \quad (7)$$

The branch matrix is expressed as (8).

$$\gamma_k(s_{k-1}, s_k) = \begin{Bmatrix} \gamma_{k00} = 0.5\,(L_a(d_k) + L(d_{in}) + L(P_{k1}) \\ \gamma_{k01} = 0.5\,(L_a(d_k) + L(d_{in}) - L(P_{k1}) \\ \gamma_{k10} = 0.5\,(-L_a(d_k) - L(d_{in}) + L(P_{k1}) \\ \gamma_{k11} = 0.5\,(-L_a(d_k) - L(d_{in}) - L(P_{k1}) \end{Bmatrix} \quad (8)$$

Here,
L_a=Priori LLR
d_{in}=Methodical bit to the realization of extrinsic information
P_{k1}=Bit for parity check

Subsequently, after processing the calculations of the LLR, the resultant extrinsic information is presented as (9).

$$L_e(d_k) = \mu.\left(L(d_k|h) - L(d_{in}) - L_a(d_k)\right) \quad (9)$$

Where μ denotes the scaling factor, and for accessing the extrinsic information in the MAP procedure to recompense for the losses, μ<1.

4. METHOD

To meet the decoding requirements in the turbo coding scheme, interleaver and de-interleaver blocks are placed in parallel. The most challenging factor in the interleaving process is the contention of memory. Figure 5 shows the interleaving and parallel processing of the turbo decoder. To extract extrinsic information in terms of forwarding and backward variables, successive interleaving is used. Depending on the block size of data-parallel execution is used. An address generator unit (AGU) and a control unit (CU) are used to map the interleaver and de-interleaved with random access memory (RAM).

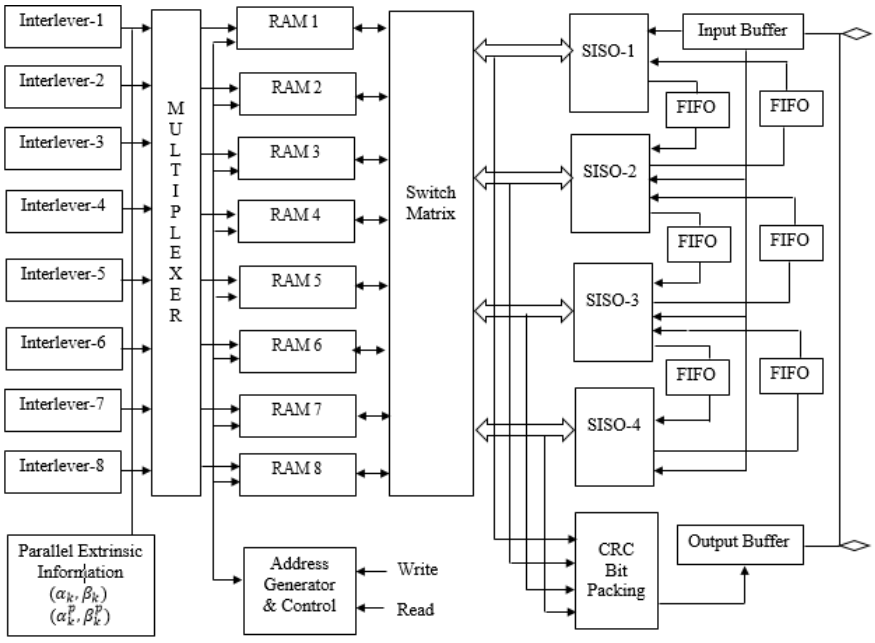

Figure 5. The execution and parallel realization of the interleaving concept in the turbo hardware decoder

The real-time log-likelihood ratio and the parallel extrinsic information are selected with the help of multiplexers to perform the interleaving process. To perform the sequential read and write operations control signals are linked with RAM. To improve latency and reduce processing time during each iteration the AGU

is used. For the selection of SISO and first input first output (FIFO) modules switch matrices are used. Depending upon the priority, each FIFO module is attached to its current SISO module for input-output buffer synchronization. Since, the LLR, branch matrices, forward matrices, and backward matrices parameters are sequential. The throughput of the turbo decoder can be maximized using input and output buffers [27].

The design methodology of the work is as follows. The chip functionality follows the steps of the chip design, and simulation modeling. The VHDL programming is used to design the turbo encoder and decoder chip that accepts the 32-bit input stream. The waveform simulation is carried out for both the integrated decoder module in which the test cases are verified. The real-time verification is done on the Virtex-5 FPGA board to check the feasibility of the design. The method for the same is given in Figure 6.

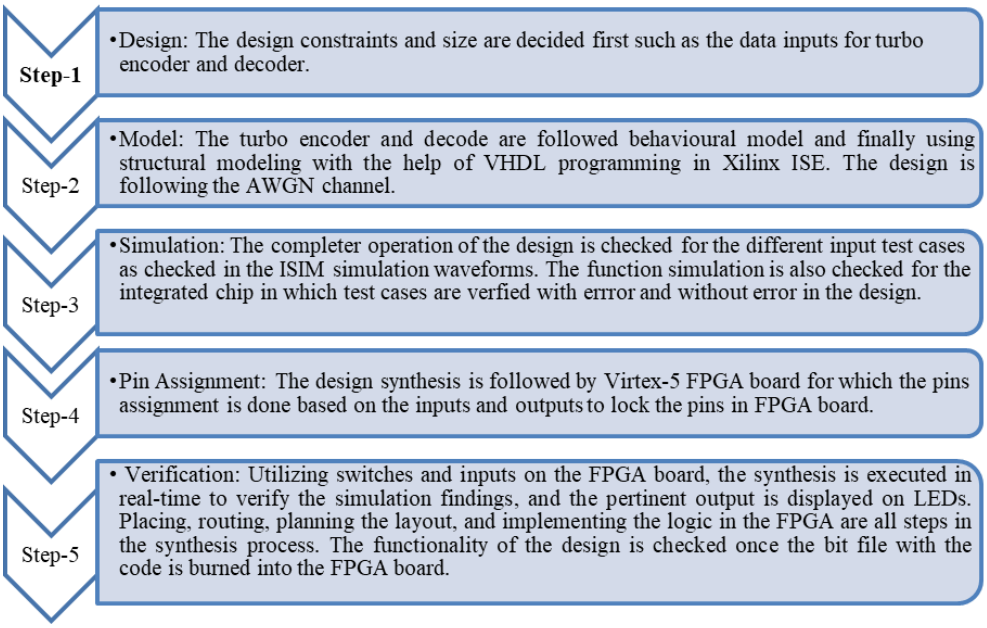

Figure 6. Method

5. RESULTS AND DISCUSSIONS

In Xilinx ISE 14.7, the behavioral modeling-based model is used to develop the turbo encoder and decoder. The encoder and decoder integrated chip register transfer level (RTL) view are shown in Figure 7. Table 1 lists the specifics of RTL pins. Figure 8 depicts the waveform in Xilinx ISIM for the decoder for test-1 and test-2 in binary without error in reception. Figure 9 depicts the waveform in Xilinx ISIM for the decoder for test-1 and test-2 in hexadecimal without error in reception. Figure 10 depicts the waveform in Xilinx ISIM for the decoder for test-3 and test-4 in binary with an error in reception. Figure 11 depicts the waveform in Xilinx ISIM for the decoder for test-3 and test-4 in hexadecimal with an error in reception. The major inputs and outputs of the decoder's main stimuli are displayed on the simulation test bench.

Table 1. Pin description of encoder module and decoder module RTL chip

Pins	Direction	Description
Clk	Input	The clock signal has a 50% duty cycle and is an input clock signal that can provide a rising edge-based clock signal.
Reset	Input	To maintain the contents 0 for the encoder and decoder, reset is the chip design's default input.
Turbo_tx_data_in_encoder [31:0]	Input	It gives the turbo encoder provided at the transmitter section of the design the 32-bit input message.
Turbo_rx_data_out_decoder [31:0]	Output	The 32-bit turbo-encoded output can be treated as an AWGN channel's input.
Turbo_enc_data_inout [31:0]	Inout	It is the 32-bit output of the AWGN communication channel and feedback to the turbo decoder.
Error	Output	It is the indicator output that a correct or incorrect message is received in the decoder section.

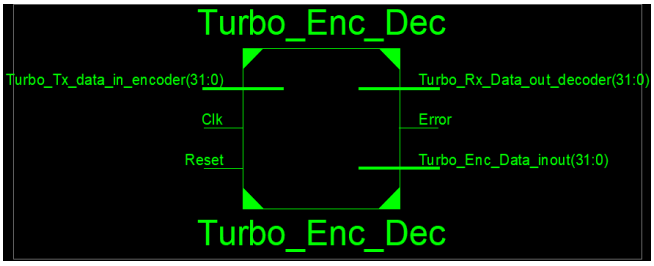

Figure 7. RTL view of the integrated turbo encoder and decoder

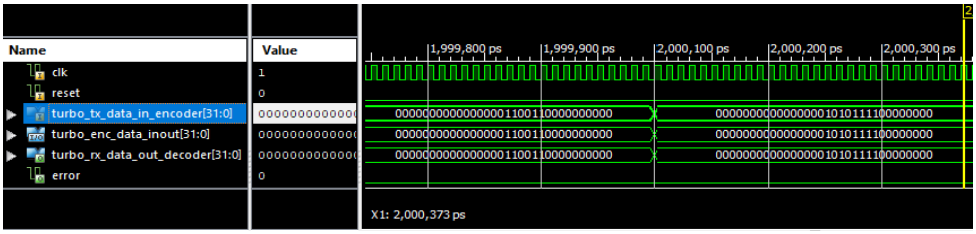

Figure 8. Waveform in Xilinx ISIM for decoder for test-1 and test-2 in binary

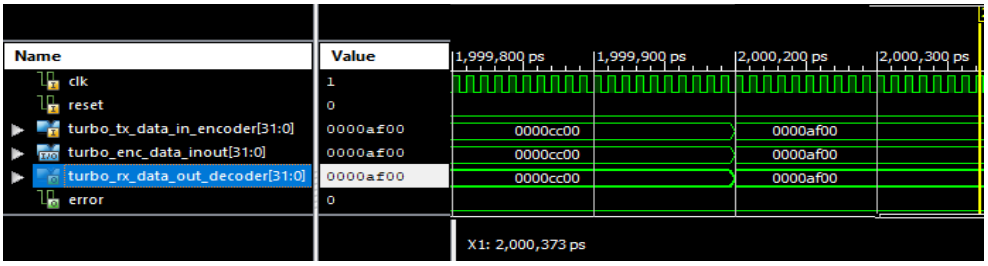

Figure 9. Waveform in Xilinx ISIM for decoder for test-1 and test-2 in hexadecimal

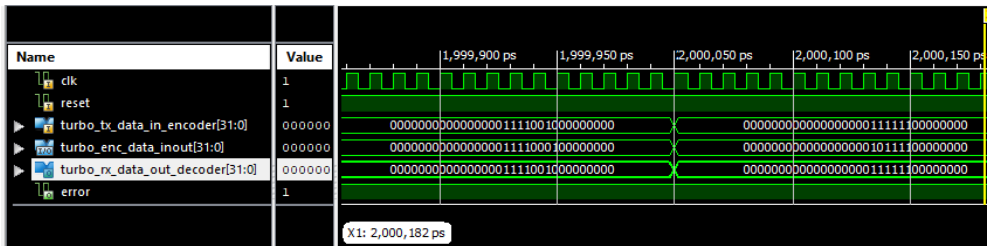

Figure 10. Waveform in Xilinx ISIM for decoder for test-3 and test-4 in binary

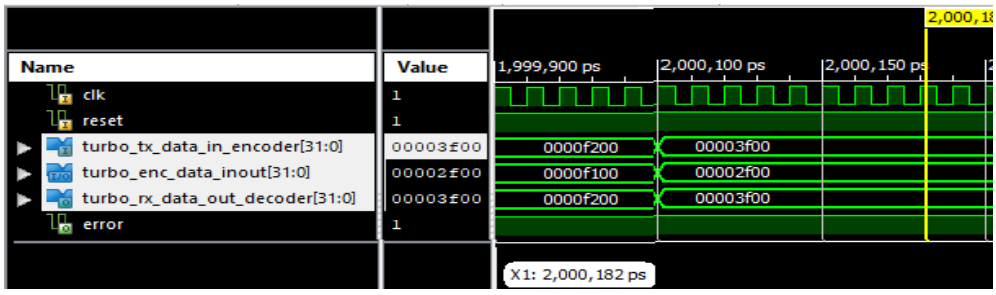

Figure 11. Waveform in Xilinx ISIM for decoder for test-3 and test-4 in hexadecimal

Test case (turbo encoder/ decoder):

- Apply Clk=rising edge clock signal, reset='0', turbo_tx_data_in_encoder [31:0]="0000 0000 0000 0000 1100 1100 0000 0000" (binary)=0000CC00 (hexadecimal), then turbo_enc_data_inout [31:0]="0000 0000 0000 0000 1100 1100 0000 0000" (binary)=0000CC00 (hexadecimal), and turbo_rx_data_out_decoder [31:0]="0000 0000 0000 0000 1100 1100 0000 0000" (binary)=0000CC00 (hexadecimal), with error='0'
- Apply Clk=rising edge clock signal, reset='0', turbo_tx_data_in_encoder [31:0]="0000 0000 0000 0000 1010 1111 0000 0000" (binary)=0000AF00 (hexadecimal), then turbo_enc_data_inout [31:0]="0000 0000 0000 0000 1010 1111 0000 0000" (binary)=0000AF00 (hexadecimal), and turbo_rx_data_out_decoder [31:0]="0000 0000 0000 0000 1010 1111 0000 0000" (binary)=0000AF00 (hexadecimal) with error = '0'
- Apply Clk=rising edge clock signal, reset='0', turbo_tx_data_in_encoder [31:0]="0000 0000 0000 0000 1111 0010 0000 0000" (binary)=0000F200 (hexadecimal), then turbo_enc_data_inout [31:0]="0000 0000 0000 0000 1111 0001 0000 0000" (binary)=0000F100 (hexadecimal), and turbo_rx_data_out_decoder [31:0]="0000 0000 0000 0000 1111 0010 0000 0000" (binary)=0000F200 (hexadecimal) with error='1'
- Apply Clk=rising edge clock signal, reset='0', turbo_tx_data_in_encoder [31:0]="0000 0000 0000 0000 0011 1111 0000 0000" (binary)=00003F00 (hexadecimal), then turbo_enc_data_inout [31:0]="0000 0000 0000 0000 0010 1111 0000 0000" (binary)=00002F00 (hexadecimal), and turbo_rx_data_out_decoder [31:0]="0000 0000 0000 0000 0011 1111 0000 0000" (binary)=00003F00 (hexadecimal) with error='1'.

Table 2 summarizes the hardware parameters of the turbo encoder and decoder hardware with MAP algorithm in Xilinx ISE 14.7 software for various parameters targeting the Virtex-5 FPGA. Slices, flip-flops, LUTs, and input/output block (IOBs) are the hardware parameters [28]. Table 3 shows the results of timing simulations for the turbo encoder and decoder chip hardware for time-concerned parameters such as minimum period (ns), minimum and maximum duration before and after the clock signal (ns), and maximum supporting frequency [29].

Table 2. Summary of FPGA hardware usage

Hardware	Turbo codes		Turbo codes with Max log-MAP	
	Encoder	Decoder	Encoder	Decoder
Slices	75	150	67	140
Flip-flops	87	103	77	80
LUTs	120	125	103	107
IOBs	64	96	64	96
Global Clocks (GCLKs)	1	1	1	1

Table 3. Parameters connected to timing information

Timing parameter	Turbo codes		Turbo codes with Max log-MAP	
	Encoder	Decoder	Encoder	Decoder
Frequency (MHz)	314.0	320.0	332.00	355.0
Minimum period (ns)	1.710	1.420	1.6120	1.390
Time (minimum) before clock (ns)	2.109	2.917	1.964	2.851
Time (maximum) after clock (ns)	4.320	5.325	4.124	4.109
Combinational path delay (ns)	8.139	9.662	7.700	8.350
Speed grade	-5	-5	-5	-5

Figure 12 presents the FPGA hardware utilization graph for the turbo encoder and decoder with a simple and integrated Max log-MAP algorithm chip. Figure 13 presents the time-related parameters of FPGA hardware. The combinational path delay and related time parameters are reduced by the integration of the Max log-MAP algorithm in the turbo encoder and decoder hardware due to parallel execution.

The major motivation for parallel implementation is to efficiently execute code, as it saves time and allows programmers to be executed in a shorter clock time. There is significantly less disruption for workers and equipment because multiple processes can run simultaneously. The encoder and decoder both utilize less hardware resources in comparison to the turbo encoder and decoder due to the parallel execution of the block. The designed hardware chip reduces the hardware utilization in the FPGA synthesis.

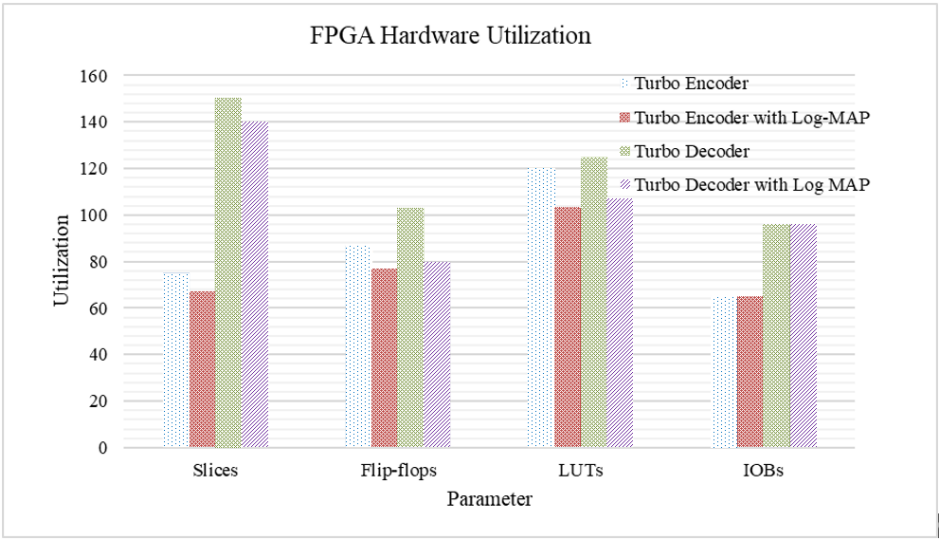

Figure 12. FPGA hardware usage

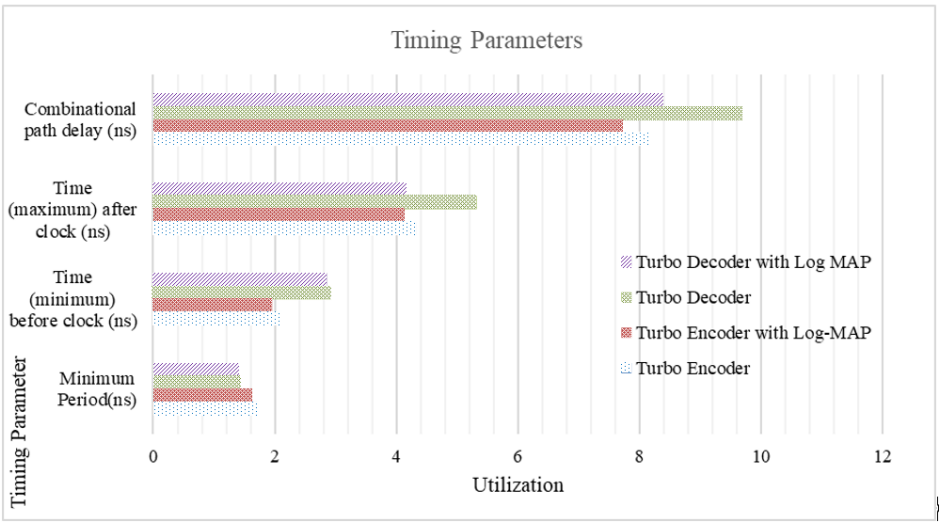

Figure 13. FPGA timing parameters

6. CONCLUSION

The hardware chip design of the turbo encoder and decoder is done successfully in Xilinx ISE 14.7. The Max log-MAP algorithm is integrated with the chip. The comparative performance of the chip is studied based on hardware and timing parameters on Virtex-5 FPGA synthesis. The ISIM simulation waveform shows the successful decoding of the data using the turbo decoder. The turbo encoder with Max log-MAP utilizes less number of slices (67), flip-flops (71), and LUTs (103) in comparison to the turbo encoder. In the same way, the turbo decoder with Max log-MAP utilizes less number of slices (140), flip-flops (80), and LUTs (107) in comparison to the turbo decoder. The frequency of the turbo encoder and decoder is 314 MHz and 320 MHz respectively. The frequency of the turbo encoder and decoder with the Max log-MAP algorithm is 332 MHz and 350 MHz respectively. The higher frequency support indicates that the turbo encoder and decoder with the Max log-MAP algorithm provide the faster response in comparison to the turbo encoder and decoder. The combination path delay of the turbo encoder and decoder with the Max log-MAP algorithm is 7.700 ns and 8.350 ns respectively, which is less in comparison to the combinational path delay of the turbo encoder and decoder. The designed encoder and decoder hardware chip with the Max log-MAP algorithm provides less hardware utilization, higher frequency support, and less delay in comparison to the turbo encoder and decoder.

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