Indian Journal of VLSI Design (IJVLSID)
ISSN: 2582-8843 (Online), Volume-3 Issue-1, March 2023

A Comparative Study of CMOS Transimpedance Amplifier (TIA)

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Abstract: ***In this paper a comparative study of different CMOS transimpedance amplifier has been presented. Standard device parameters of transimpedance amplifier such as gain, input refereed noise, power dissipation and group delay are studied and compared. Here the transimpedance amplifier is divided on the basis of its topology and device technology used and performance is summarized to get the overview. Most of the analysis taken are performed on 0.18 µm technology and some are implemented using 45nm, 0.13µm, 65nm, and 90nm.***

Keywords: ***CMOS, Transimpedance, Amplifier (TIA), Technology***

I. INTRODUCTION

In today's intelligence technology various sensors are used to convey the information signal. Most of the sensors convert this information containing signal to current signal but these signals cannot be further processed since most of the subsequent blocks in a system work in voltage mode. Therefore, it is mandatory to convert this current signal to amplified voltage signal. This conversion can be carried out using transimpedance amplifier (TIA). Transimpedance amplifier can be designed using active and passive circuit elements. Passive circuit elements have many limitations in VLSI designing such as larger chip area, higher power dissipation and so on thus active elements are used more often such as BJT, MOSFET or an operational amplifier. While designing a Practical Transimpedance Amplifier Main Characteristics of concern are low input impedance, low output impedance, high transimpedance gain, high bandwidth and low noise. In this paper main concern is on CMOS transimpedance amplifier. Further section II presents different topologies of CMOS transimpedance amplifier and section III includes comparative study analysis of CMOS existing transimpedance amplifier on the basis of topology and device technology used.

Manuscript received on 12 January 2023 | Revised Manuscript received on 25 February 2023 | Manuscript Accepted on 15 March 2023 | Manuscript published on 30 March 2023.

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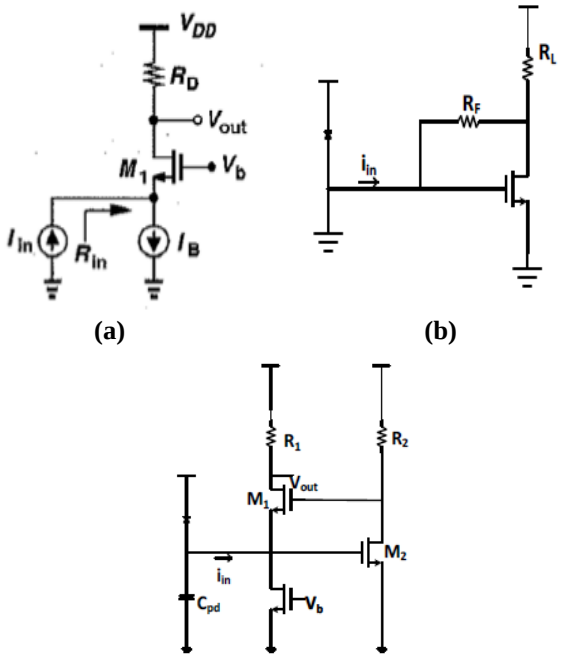
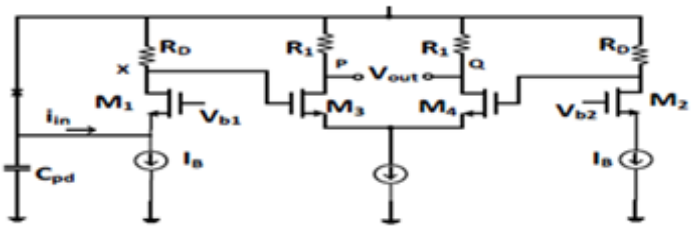
II. TOPOLOGIES OF CMOS TRANSIMPEDANCE AMPLIFIER

A number of research papers published related to CMOS transimpedance amplifier were studied. [1-40] Based on the literature review most of the reported CMOS transimpedance amplifier can be broadly classified in to four types- common gate topology, common source topology, regulated cascode topology and differential topology. Most of the transimpedance amplifier used these basic topologies or hybridized form are used for further improvement. In common gate topology input impedance is low as compared to other topology due to proper bias current. Due to this high bandwidth can be achieved. Noise is the major issue of common gate topology when used in low supply voltage. Common source topology have high driving capability but as the device size minimize transistors breakdown voltage also reduces. Due to this tradeoff amid transimpedance gain and voltage headroom is very crucial for common source topology. Effect of parasitic capacitance on bandwidth can be reduced by cascode structure in regulated cascode topology but due to severe trade off in all characteristics more improvement in circuit is required. Differential structure results in less offset noise and cannot be used alone due to deferential input a converter is always needed that makes circuit more complex.



(a) (b)

(c)



(d)

Figure 1. (a) Common gate TIA topology [36] (b) Common source TIA topology [13] (c) Regulated Cascode TIA topology [33] (d) Differential TIA topology [36]

III. COMPARATIVE STUDY OF CMOS TIA

Comparison of some of the transimpedance amplifier designed with best characteristic achieved so far is refereed in table 1 in ascending order of publication year. Best result obtained among them for each characteristics are highlighted. In table 2 the latest transimpedance amplifier based on device technology used are compared. CMOS technology was always in lime light due to its low cost, low power dissipation and integrity property, but due to its parasitic properties and degraded noise performance design of TIA becomes challenging. Various research gaps had been identified based on this study. Common gate topology of CMOS TIA cannot work at low supply voltage efficiently because of degraded noise performance. Nano scale application cannot use common source TIA due to less voltage headroom thus high bit error rate. Regulated cascode topology provides best isolation from parasitic capacitance but severe tradeoff between gain and bandwidth reduces the efficiency.

Table 1. Comparison of Various TIA Designed

Ref. No.	Year	Topology /technique	Power supply (volts)	Gain D Bohms	BW	Input Referred Noise (pA/√Hz)	Power dissipation M W
[8]	1991	GaAs FET	-	-	100 MHz	-	-
[12]	1999	C peaking technique	-	0.95	2.3 GHz	-	-
[14]	2002	hybrid topology	-	20	1 Ghz	-	27
[9]	2004	Regulated cascade	5	58	950 MHz	6.3	85
[21]	2004	Interstage matching network technique	2.5	54	9.2 GHz	-	-
[10]	2006	Regulated cascade	2	52	7.6GHz		34
[27]	2007	Regulated cascade	1.8	53	8GHz	18	13.5
[5]	2007	Common base-BiCMOS		65.2	7.2GHz	17.7	56.6
[29]	2010	Common gate with active feedback	1.8	54.6	7GHz	17.5	18.6
[32]	2012	Regulated Cascode		52	**35GHz**	14	-
[34]	2012	SOI technology	-	55	33GHz	20.47	-
[39]	2014	Common gate	-	**104.2**	19MHz	-	-
[19]	2015	Differential		87.8	1.4GHz	-	8.1
[3]	2015	Regulated Cascode	3.3	61	15GHz	-	32
[24]	2015	Regulated cascade	-	-	9GHZ	-	-
[18]	2015	Regulated cascade	1.5	50	7GHz	31	-
[17]	2016	Differential with Regulated Cascode input stage	1.8	18	870 MHz	**6**	27
[15]	2017	Common gate using FGMOS	**1**	37.7	13.5GHz	-	**1.1**
[40]	2018	BiCMOS tech.	-	67	28GHz	10	95

Table 2. Performance Comparison of Latest Existing TIA Using Different Device Technology

Technology And devices	Paper no.	Bandwidth (GHz)	Input referred noise (pA/√Hz)	Gain (Z_T) dBΩ	Power Dissipation mw
Bi CMOS 130 nm	IEICE transaction 2018[40]	28	**10**	**67**	95
FGMOS 0.18µm	Integration: the VLSI journal: ELSEVIER 2018[15]	13.5	-	37.7	**1.1**
CMOS 65nm	ISCAS 2012[35]	**35**	14	52	168
SOI CMOS 45nm	JSSC 2012[34]	33	20.47	55	9

IV. CONCLUSION

Apart from topology device technology is playing major issue in improving the characteristics especially when low voltage and low power is concerned. FGMOS as active feedback provides best result in terms of low power supply and power dissipation. BiCMOS gives most consistent result in terms of all characteristics. All topologies are improvised and further improvement can be done to attain the best characteristics by introducing several techniques of bandwidth enhancement and hybridizing these topologies to take the advantage of each. These improved TIA can enhance the performance of intelligent system and application in receiving and transmission of various information carrying signal.

FUTURE WORK

Design of transimpedance amplifier necessitates efficient tradeoff and improvisation of each characteristic. Low voltage circuit techniques such as FGMOS, QFGMOS, bulk driven, DTMOS etc can be used for low voltage application and reducing the power consumption. Various noise reduction techniques could be used in the TIA circuit to optimize the noise performance. Further cascading of different stages will improve the gain as well as improve the parasitic capacitance effect to improve the bandwidth requirement.

DECLARATION

Funding/ Grants/ Financial Support	No, I did not receive.
Conflicts of Interest/ Competing Interests	No conflicts of interest to the best of our knowledge.
Ethical Approval and Consent to Participate	No, the article does not require ethical approval and consent to participate with evidence.
Availability of Data and Material/ Data Access Statement	Not relevant.
Authors Contributions	All authors have contributed equally.

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