Verification of UART and I2C Protocols Using System Verilog

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ABSTRACT- Design Verification in VLSI is the most important step in the product development process. It aims toconfirm that the system designed meets with the standards andrequirements of the system. Verification is the process ofchecking whether the designed system performs all the required functionality specified in the design by writing the test bench or verification environment that contains group ofclasses and modules which generates input stimulus to the system and the output from that design is compared with the expected output.

A communication system has set of roles those are called protocols. UART is a serial communication protocol that is used when only two devices are needed to communicate and it uses peer to peer topology. I2C stands for Inter Integrated Circuit used for communication between master and slave in which more thanone slave devices or memory can be connected to a master device. System Verilog has been primarily used for the verification purposes in VLSI because it has the features of Hardware Description Languages such as Verilog and VHDL, C and C++ and functional coverage, assertion coverage, constrained randomization and supports OOPs concepts.

KEYWORDS- Verification, Protocols, UART, I2C, System Verilog.

I. INTRODUCTION

A. *Verification in VLSI is Done in Two Stages*

Verification is the Predictive analysis that is done to make sure the design will carry out the specified input output function when manufactured [1].

Test: A production phase that verifies there are no manufacturing defects in the actual product that was created from the synthesized design.

System Verilog has special features like randomization, functional coverage, assertions and use OOP features in test bench construction.

Test bench is a group of classes or components where each component is responsible for performing a specific operation.

i.e. generating stimulus, driving to the DUT, monitoring, comparing and scheduling different events like reset, main tasks etc. and those classes will be named based on the operation[9,10].
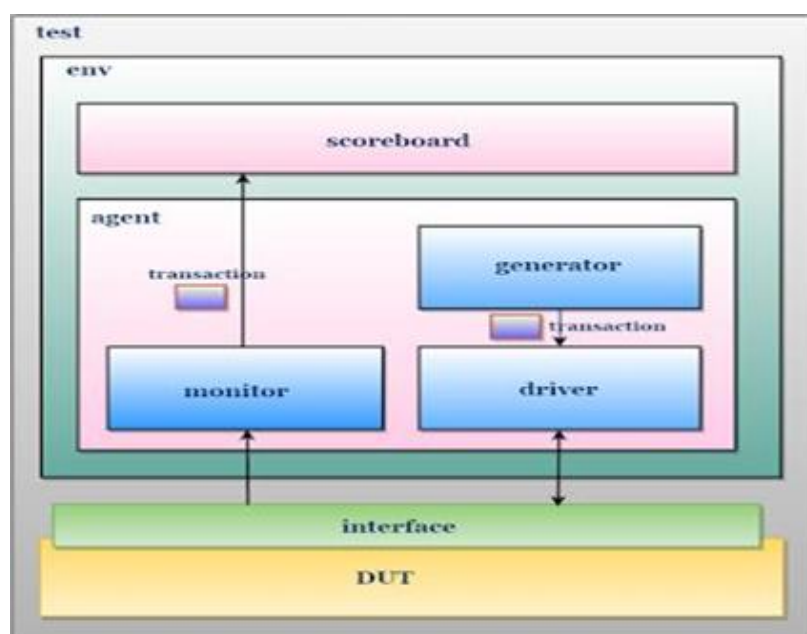

Figure 1: Block Diagram of System Verilog Test Bench

II. UART PROTOCOL

Generally, there are two types of UARTS one is transmitting UART and other is entering UART and the commerce between these two can be done directly [4, 5, 6]. For this, simply two lines are needed to communicate between two UARTs. The inflow of data will be from both the transmitting(Tx) & receiving(Rx) legs of the UARTs. In this protocol the Communication from Tx UART to Rx UART can be done without timepiece. In UART the data transmission can be done like a microcontroller, memory, CPU[7]. The entered UART data packet contains three bits like launch, stop and equality in addition to entered data. It reads the data packet bit by bit and converts the entered data into the resemblant form to exclude the three bits of the data packet. The data packet entered by the UART transfers in resemblant to the entering end by data machine.
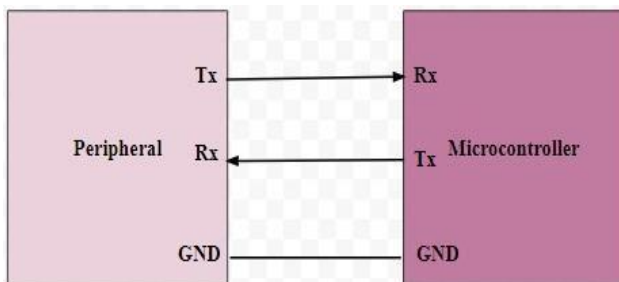

Figure 2: UART communication

UART has 10-bit data frame including start and stop bits, when the parity is added then data becomes 11 bits.
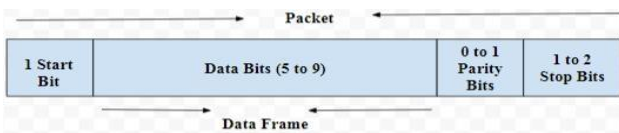

Figure 3: UART data frame

Initially the transmitting and receiving lines are high which

indicates that there is no data transmission. When the device wants to start the communication, it pulls the transmitting line to low in order to notify that the transmitting transmitter wants to send the data there is a stop bit which is an active high signal which acknowledges the receiver about the end of transmission. The rate of transmission of data is dependent on the baud rate between the UART transmitter and receiver.

A. Results

The parameters that are displayed in the output are:

- Type of operation being done.
- The data which is being transmitted.
- The data present at the transmitter and receiver outputs.
- Acknowledgment signals which notify whether the particular operation is done or not.

B. Output

- KERNEL: [DRV] : RESET DONE
- KERNEL: [GEN] : oper : write send : 0 TX_DATA : 01011000 RX_IN : 0 TX_OUT : 0 RX_OUT : 00000000 DONE_TX : 0 DONE_RX : 0
- KERNEL: [DRV]: Data Sent : 88
- KERNEL: [MON] : DATA SEND on UART TX 88 # KERNEL: [SCO] : DRV : 88 MON : 88
- KERNEL: DATA MATCHED
- KERNEL: [GEN] : oper : read send : 0 TX_DATA : 00001010 RX_IN : 0 TX_OUT : 0 RX_OUT : 00000000 DONE_TX : 0 DONE_RX : 0
- KERNEL: [DRV]: Data RCVD : 98
- KERNEL: [MON] : DATA RCVD RX 98 # KERNEL: [SCO] : DRV : 98 MON : 98
- KERNEL: DATA MATCHED
- # KERNEL: [GEN] : oper : write send : 0 TX_DATA : 11001110 RX_IN : 0 TX_OUT : 0 RX_OUT : 00000000 DONE_TX : 0 DONE_RX : 0
- KERNEL: [DRV]: Data Sent : 206
- KERNEL: [MON] : DATA SEND on UART TX 206
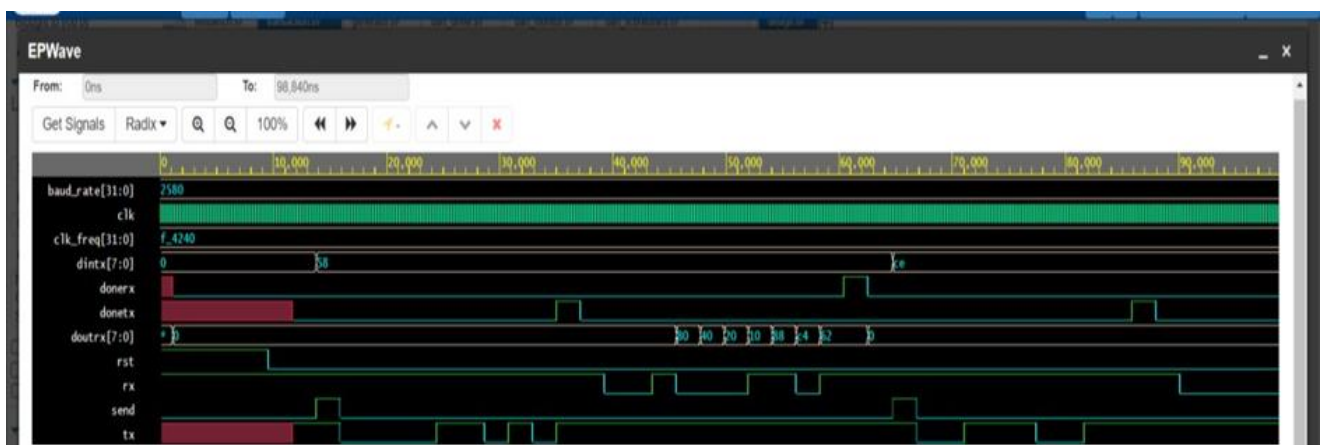- KERNEL: [SCO] : DRV : 206 MON : 206 # KERNEL: DATA MATCHED

Figure 4: Output of UART protocol

III. I2C PROTOCOL

I2C is a multi-master and multi-slave periodical

communication protocol means that we can attach multiple IC at a time with the same machine[2]. In the I2C protocol, the master has control on motorcars and in the case of

multi-master, only one master will control I2C machine. The data transfer and synchronization between the master and slave is done by timepiece signal. In communication master and slave partake the same timepiece, for coetaneous periodical communication. The timepiece machine is handled by the master but in some conditions the slave is also suitable to control the timepiece[3].
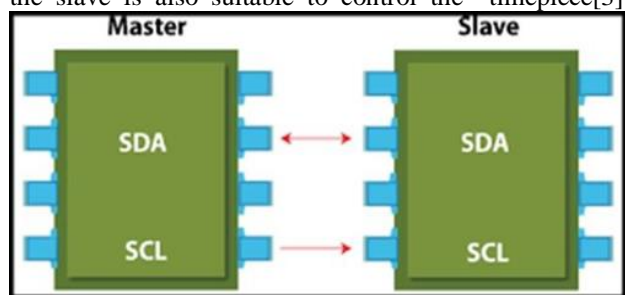

Figure 5: I2C communication

A. I2C Data Frame

I2C is an eight- bit communication protocol and an ACK or NACK bit associated with each byte. In I2C data is transferred in dispatches. Each communication begins with a launch bit, and the trade ends with a stop bit. Master may shoot another launch condition to retain control of the machine. dispatches contain frames of data. Each communication has an address frame (slave address), and one or farther data frames that contain the data being transmitted. The communication signal consists of rd/ wr bits, 1 bit ACK/ NACK signal between each data frame. See the below Image[8].
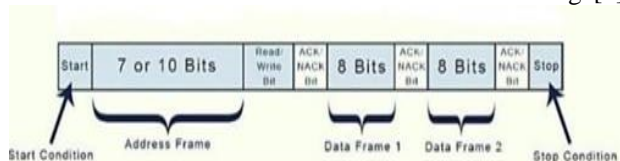

Figure 5: I2C data frame

B. Process of Data Transmission

Slave devices get acknowledged by master with the help of start condition. The data transmission is done by SCL and SDL lines. If address matches the target device gets selected and other slaves get disconnected. The slave device with a matched address received from the master, responds with a confirmation to the master after which the communication is established between both master and slave devices on the data bus.

Then, the master can transmit 8-bit of data to the receiver which replies with a 1-bit confirmation.

C. Result

The following parameters are displayed in the Output:

- The type of operation being done.
- The data sent by the master
- The address at which the data is stored
- Read operation is completed or not.
- Acknowledgement signal to know whether a particular operation is completed or not.

D. Output

- KERNEL: [DRV] : RESET DONE
- KERNEL: [GEN] : WR : 1 WDATA : 76 ADDR : 1 RDATA : 0 DONE : 0
- KERNEL : [DRV] : wr:1 wdata :76 waddr : 1 rdata : x# KERNEL : [MON] : DATA WRITE -> wdata :76 waddr : 1
- KERNEL: [SCO] : WR : 1 WDATA : 76 ADDR : 1 RDATA : 0 DONE : 0
- KERNEL: [SCO]: DATA STORED -> ADDR : 1DATA : 76
- KERNEL: [GEN] : WR : 0 WDATA : 23 ADDR : 4 RDATA : 0 DONE : 0
- KERNEL : [DRV] : wr:0 wdata :23 waddr : 4 rdata :145
- KERNEL: [MON] : DATA READ -> waddr : 4 rdata : 145
- KERNEL: [SCO] : WR : 0 WDATA : 23 ADDR : 4 RDATA : 145 DONE : 0
- KERNEL: [SCO] :DATA READ -> Data Matched # KERNEL: [GEN] : WR : 0 WDATA : 49 ADDR : 1 RDATA : 0 DONE : 0
- KERNEL : [DRV] : wr:0 wdata :49 waddr : 1 rdata :76
- KERNEL: [MON] : DATA READ -> waddr : 1 rdata : 76
- KERNEL: [SCO] : WR : 0 WDATA : 49 ADDR : 1 RDATA : 76 DONE : 0
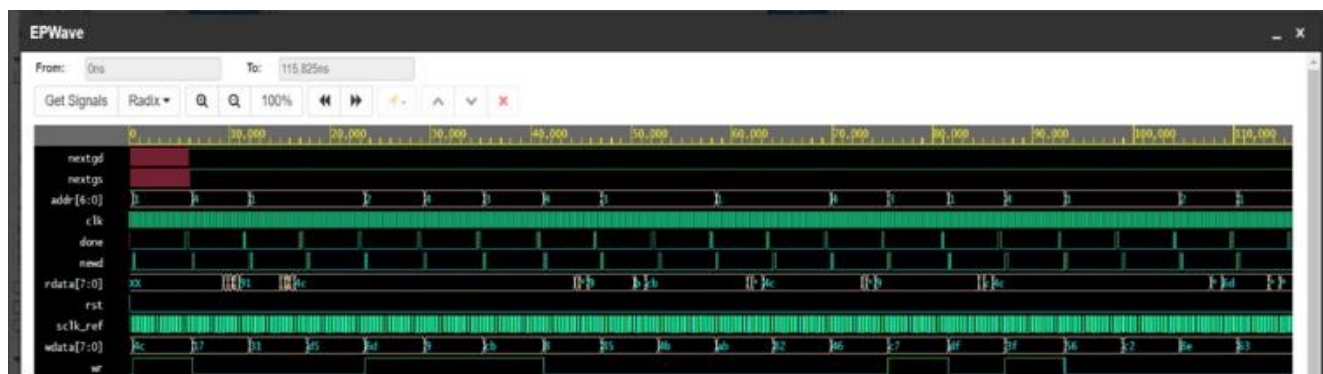- KERNEL: [SCO] :DATA READ -> Data Matched

Figure 6: I2C waveforms

IV. COMPARISION BETWEEN UART AND I2C

UART	I2C
peer to peer topology is used	Master-slave method is used
only a single device canbe connected	Multiple devices can be connected to a single master
The amount of data to be transferred is dependent on baud rate.	The amount of data that canbe transferred by the master is 400kbps.
it is used for high speed devices	it is used for low speed devices
the address allocation and write operation takes place simultaneously	the write operation is doneonly after the acknowledgement of address allocation

V. CONCLUSION

The UART and I2C protocols are designed using System Verilog. The reset, write and read operations of the two protocols are verified and both the protocols are compared with each other based on the parameters such as the topology used, design specifications and data processing.

VI. ABBREVIATIONS

VLSI: Very Large-Scale Integration UART: Universal Asynchronous Receiver and Transmitter I2C: Inter Integrated Circuit.

CONFLICTS OF INTEREST

The authors declare that they have no conflicts of interest.

REFERENCES

[1] Yamini R, Ramya M V, Design and Verification of UART using System Verilog, International Journal of Engineering and Advanced Technology (IJEAT)ISSN: 2249 – 8958 (Online), Volume-9 Issue-5, June 2020

[2] Lakshmi Manasa Kappaganthu, Durga Prakash M, Avinash Yadlapati, I2C Protocol and its Clock Stretching Verification using System Verilog and UVM,International Conference on Inventive Communication and Computational Technologies, (ICICCT 2017)

[3] R. K. Megalingam, J. M. Varghese and S. A. Anil, "Distance estimation and direction finding using I2Cprotocol for an auto-navigation platform," 2016 International Conference on VLSI Systems, Architectures, Technology and Applications (VLSI- SATA), Bengaluru, India, 2016, pp. 1-4, doi: 10.1109/VLSI-SATA.2016.7593061.

[4] U. Nanda and S. K. Patnaik, "Universal Asynchronous Receiver and Transmitter (UART)," 2016 3rd International Conference on Advanced Computing and Communication Systems (ICACCS), Coimbatore, India,2016, pp. 1-5, doi: 10.1109/ICACCS.2016.7586376.

[5] Vibhu Chinmay, Shubham Sachdeva, "A Review Paperon Design and Simulation of UART for Serial Communication,"2014 IJIRT, Volume 1 Issue 6, SSN : 2349-6002.

[6] Bidisha Kashyap and V Ravi, "Universal Verification Methodology Based Verification of UART Protocol", Published under licence by IOP Publishing Ltd. Journal of Physics: Conference Series, Volume 1716, National Science, Engineering and Technology Conference (NCSET)2020,11-12 May 2020, Vellore Institute of Technology, Chennai, India. Citation Bidisha Kashyap and V Ravi 2020 J. Phys.: Conf. Ser. 1716 012040, DOI 10.1088/1742-6596/1716/1/012040

[7] M. R. L. P. M. M. "Design and Implementation of UART". International Journal on Recent and Innovation Trends in Computing and Communication, vol. 3, no. 6,June 2015, pp. 4289-91, doi:10.17762/ijritcc.v3i6.4638.

[8] Frederic Leens, An Introduction to I2C and SPI Protocols, IEEE Instrumentation and Measurement magazine February 2009."Implementing I2C Communication Protocol in LABVIEW FPGA", http:/ /www.ni.com. Samir Palnitkar, Verilog HDL - A guide.

[9] Comparison of VHDL, Verilog and System Verilog, by Stephen Bailey, www.model.com C. H. Roth, "Digital System Design Using VHDL", PWS

[10] Publishing Company, 2008.

[11] System Verilog Verification guide (https://verificationguide.com/systemverilog/systemveril og-tutorial/)

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