A Wideband High-Gain Power Amplifier Operating in the D Band

Vasileios Manouras
School of Electrical and Computer Engineering
National Technical University of Athens
Athens, Greece
vasileiosmanouras@mail.ntua.gr

Ioannis Papananos
School of Electrical and Computer Engineering
National Technical University of Athens
Athens, Greece
papan@elab.ntua.gr

***Abstract*—In this paper the design, analysis and implementation of a 3-stage, broadband power amplifier (BPA), is presented. The device is suitable for medium-distance wireless and wireline gigabit communication in the D-band ($110-170\ GHz$). A pseudo-differential cascode topology is adopted for each stage leading to optimized broadband performance. The PA is integrated in a $0.13\ \mu m$ SiGe BiCMOS technology with $f_T/f_{max} = 250/370\ GHz$, achieving a saturation output power $P_{sat} > 9\ dBm$ and a maximum large-signal power gain $G_P > 29.5\ dB$, over the entire D-band. The chip size is $1.150 \times 0.467\ mm^2$ including all pads.**

***Keywords*—D-band power amplifier, broadband amplifier, differential cascode PA, 6G, 145 GHz, SiGe PA.**

I. INTRODUCTION

The ever increasing demand for higher data-rate communications, supporting applications beyond current mobile use scenarios, such as short-range gigabit communication over dielectric waveguides [1], medical imaging, and biosensing [2], impelled research community to a further investigation of the sub-THz region [3].Currently, referring to the high mm-wave band of 5G auctions, the developed systems use 28 GHz, while some additional bands up to 100 GHz, are planned [4]. However, higher frequency bands up to 300 GHz attract unique attention for the further data-rate extension, arising the potential of beyond 5G and 6G systems [5].

One of the most critical parts of the mm-wave and sub-THz transmitter chain in terms of maximum output power, linearity and broadband behavior, is the PA [6]. Highly linear silicon PAs operating in D-Band, able to provide reasonable output power back-off (OPBO) for wide frequency range in order to support modulated signals with bandwidth up to tens of GHz, is challenging because of the limited power performance of the transistors.

In this paper a 3-stage, pseudo-differential, broadband, cascode PA is presented. Based on the EM simulations of the designed passive structures, the PA achieves an almost flat and broadband response over the entire D-band. The paper is organized as follows: In Section II, key characteristics concerning the used SiGe process are presented with emphasis on the HBTs' performance. In Section III, the proposed D-band PA architecture is introduced, while the simulation results are denoted in Section IV.

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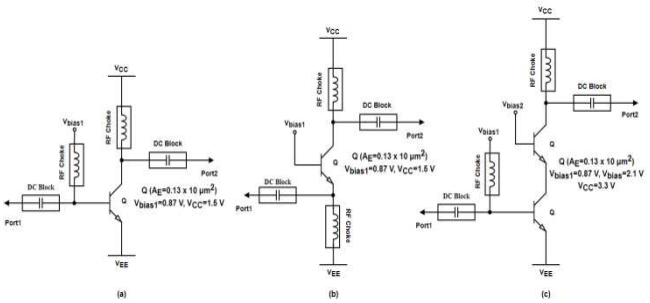
II. HBT PERFORMANCE CAPABILITIES

The proposed D-Band PA was designed and fabricated in Infineon's 130 nm SiGe BiCMOS process. The layer stackup profile includes 6 copper metal layers and 1.0 μm aluminum layer as top metal. Moreover, the technology offers heterojunction bipolar transistors (HBTs) with breakdown-voltages $BV_{CEO} = 1.8\ V$, $BV_{CBO} = 5.3\ V$ and a maximum unity gain frequency f_T as well as a maximum frequency of oscillation f_{max} of 250 GHz and 370 GHz, respectively, making the designing of mm-wave integrated circuits (ICs) for 5G-and-beyond applications, feasible. However, aiming to D-Band applications, a careful selection of the size and configuration of the active modules (HBTs) is required not only due to inherent trade-off between break-down voltages and maximum speed [7] but also because of the reliability of the provided HBT models from the foundry at such high frequencies.

The maximum available/stable gain (MAG/MSG) for the common emitter (CE) (Fig. 1a), common base (CB) (Fig. 1b) and cascode topology (CT) (Fig. 1c) are shown in Figure 1d. For comparison reasons, all the aforementioned topologies are consisted of the same HBT in multi-base configuration with an emitter mask size of $A_{eff} = 0.22 \times 10\ \mu m^2$.

The MAG/MSG simulation results of the various amplifying topologies demonstrate that the CT shows superior power gain in D-band ($110 - 170\ GHz$) at the expense of higher supply voltage and thus power consumption. Since, the proposed PA is intended for the RF front-end of a high-data rate wireline link in which the preceding Mixer block drives the PA with limited power, the highest possible power gain of the latter is necessary, leading us to the CT selection for our main active module. Furthermore, CT offers an inherent reduction of Miller's effect, enforcing the stability of our amplifying core [8].



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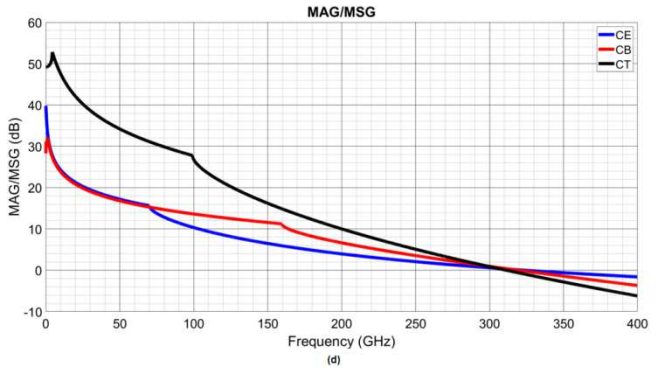

Fig 1. Schematic of (a) common-emitter (CE), (b) common base (CB), (c) cascode topology (CT). (d) Maximum Available/Stable gain (MAG/MSG).

III. D-BAND PA ARCHITECTURE

The proposed D-Band PA is shown in Figure 2. It is consisted of 3 pseudo-differential, cascode stages aiming to a broadband behavior of a 3-dB bandwidth up to 50 GHz, able to support high-data rate modulated signals with high peak-to-average power ratios (PAPR). Inductive g_m boosting technique is used in order to enhance the maximum available power gain. The single-to-differential conversion in both input and output is performed via Marchand Baluns (MBL), described in subsection III-B.

A. Broadband PA Design Consideration

Aiming to the highest possible saturated power as well 1dB compression point, the double base (BEBC) HBTs of each cascode stage have the same emitter size of $A_{eff} = 0.22 \times 10\ \mu m^2$, while each one of the CE HBTs is biased via 200 Ω TaN resistors (R_b) at the optimum current density of $J_{Copt} = 11.5\ mA/\mu m^2$ for maximum f_T, leading the cascode topology to a Class A operating point. Such a bias condition offers maximum linearity and output power for the desired 1st harmonic at the expense of power consumption. Since the transmission of broadband modulated signals with data rates up to tens or hundreds of Gbps requires the highest possible linearity both in terms of frequency and power, the conventional Class A operation offers a safe yet effective choice [8].

The 3 stages of the designed PA are based on a peudo-differential topology that provides excellent stability through the exploitation of the AC virtual grounds. Furthermore, it offers higher power gain compared to a conventional differential stage, since it takes advantage of the larger output voltage swings, via the elimination of the tail current source. It should be noted that much higher voltage swings compared to BV_{CEO} can be applied on the CB HBT, if its base node provides a low impedance path to ground, accomplished by decoupling capacitors.

Several techniques can be used to further increase the power gain of the cascode topology, based on the compensation of the voltage and frequency-depended collector-base capacitance C_{CB} . The majority of these techniques use positive or negative feedback on the CB stage of the cascode topology [6]. However, feedback should be used with caution, since the base node of the CB active module is sensitive to stability issues. In this work, a kind of inductive positive feedback is used (g_m boosting technique) through the insertion of a $5pH$ inductor L_b on the base of each CB HBT of the differential cascode stages, as Figure 2 shows.

A D-band design pushes the HBTs operating close to $f_{max}/2$, where the via contacts and intrinsic interconnects of the HBTs can be proven crucial not only to efficiency but also, to the optimal selection of the load of the various stages. Thus, the via interconnects were EM simulated and their effects were taken into consideration for an accurate modelling of the HBTs. Additionally, the optimum load of the output stage R_{opt} was determined via Load-Pull simulations at the middle frequencies of the D-Band. The impedance transformation to the 100 Ω differential termination was performed though the output matching network (OMN), consisted of 50 Ω transmission lines ($TL_{2,3,4}$) and MIM capacitors (C_1).

The broadband behavior of the proposed PA is based on the stagger tuned amplifier theory, described in [9] and it is realized via the inter-stage matching networks (ISMN) which comprises the 50 Ω $TL_{5,6,7}$ and C_2. It is worth mentioning that the accurate modelling of the passive matching networks is necessary in order to achieve the desired gain behavior over frequency. Therefore, the ISMNs were EM simulated over the whole band of interest and all the existing cross-talk and coupling effects were taken into consideration.

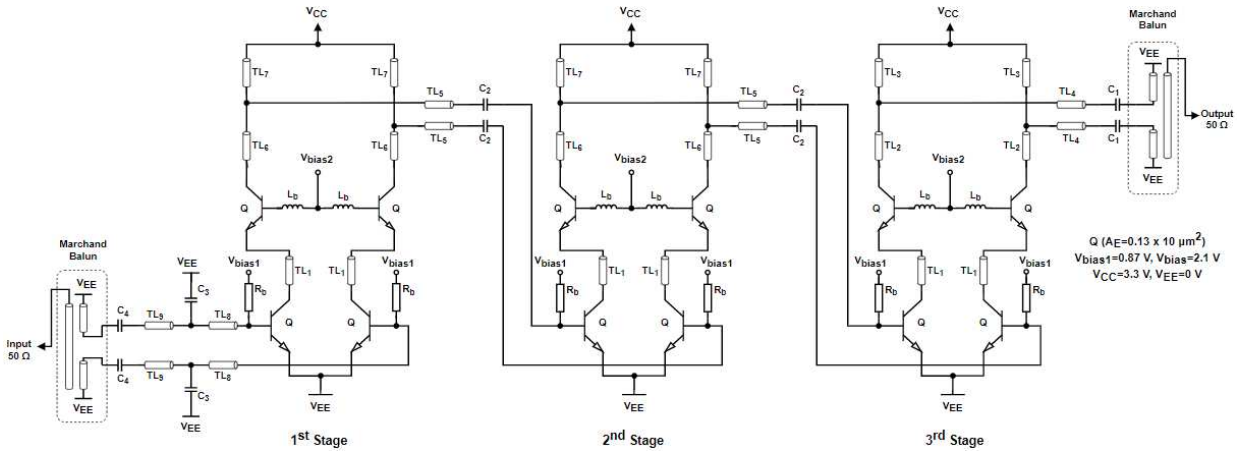

Fig 2. Schematic of the proposed D-Band PA.

The contribution of each stage in the final simulated small-signal gain is shown in Figure 3. As follows, the combination of the output stage (3rd) and the intermediate stage (2nd) generates the broadband behavior of the proposed PA, while the input stage (1st) contributes to gain flatness over the entire D-band.

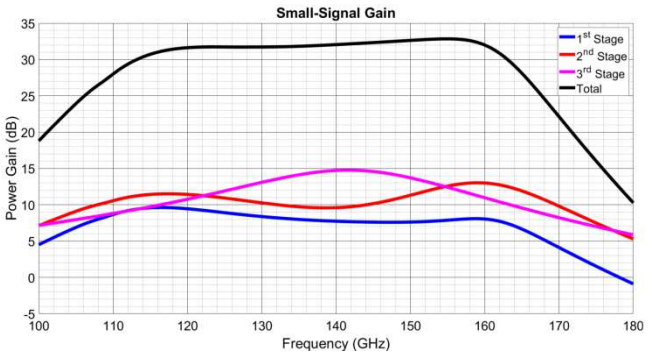

Fig 3. Small-signal gain of the various PA stages over the D-band.

As for the input matching between the differential 100 Ω output of the MBL and the bases of the CE HBTs of the first stage, the 50 Ω transmission lines $TL_{8,9}$ and MIM capacitors $C_{3,4}$ are used, since compared to a conventional T-type network, provide a wideband matching. Table I summarizes the values of the PA's passive components.

TABLE I
SUMMARY OF THE PASSIVE COMPONENTS

$\boldsymbol{TL_1}$	16.4 μm	$\boldsymbol{TL_9}$	168 μm
$\boldsymbol{TL_2}$	56.4 μm	$\boldsymbol{C_1}$	80 fF
$\boldsymbol{TL_3}$	67 μm	$\boldsymbol{C_2}$	60 fF
$\boldsymbol{TL_4}$	51 μm	$\boldsymbol{C_3}$	85.6 fF
$\boldsymbol{TL_5}$	37.1 μm	$\boldsymbol{C_4}$	30.3 fF
$\boldsymbol{TL_6}$	88 μm	$\boldsymbol{L_b}$	5 pH
$\boldsymbol{TL_7}$	38 μm	$\boldsymbol{R_b}$	200 Ω
$\boldsymbol{TL_8}$	38.6 μm		

B. Marchand Balun Design

Several on-chip, transformer-based and Marchand Baluns that perform the required single to differential conversion at the D-band, have been published recently [2], since the measurements for differential circuits in sub-THz frequencies are, in general, performed single-ended [10]. Figure 4 shows the 3D view of the MBL used in this work and based on [11].

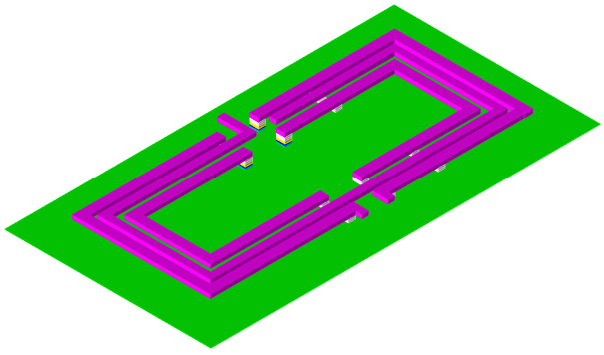

Fig 4. 3D view of the designed Marchand Balun (MBL).

The signal path is realized with the top copper layer (M6) for the minimization of the resistive losses and the capacitive coupling to ground, while the bottom layer (M1) is used as return path, providing a well-defined reference ground plane and thus enforcing the accuracy of its EM simulation. In order the MBL to perform the single to differential conversion, the M6 lines are placed in close proximity for a strong inductive and capacitive coupling between them.

Figure 5 shows the simulated S11 and S21 of the designed MBL. For the s-parameter simulation, 50 Ω and 100 Ω terminations were used in the unbalanced and balanced port, respectively. Simulation results denote that the presented MBL shows a broadband behavior with $S11 < -15\ dB$ and an almost flat $S21$ for the entire D-band. Furthermore, it is worth mentioning that the simulated insertion loss is around 1.5 dB for the same frequency band.

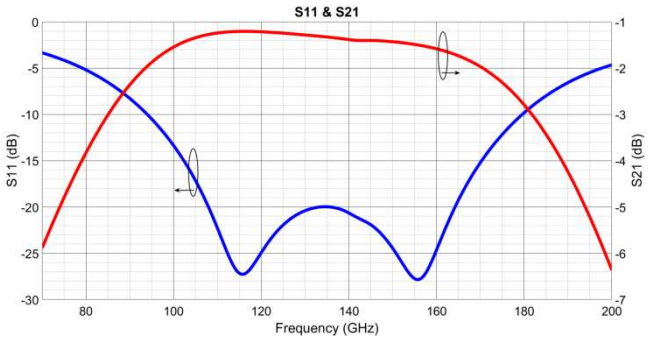

Fig 5. Simulated S11 & S21 of the designed MBL.

Considering the designed MBL as a 3-port network, the simulated amplitude and phase imbalances between the differential ports are shown in Figure 6. The balun shows an amplitude imbalance ranged from -1.5 to 1 dB as well as a phase imbalance between -2.5 and 4 degrees, over the entire D-band.

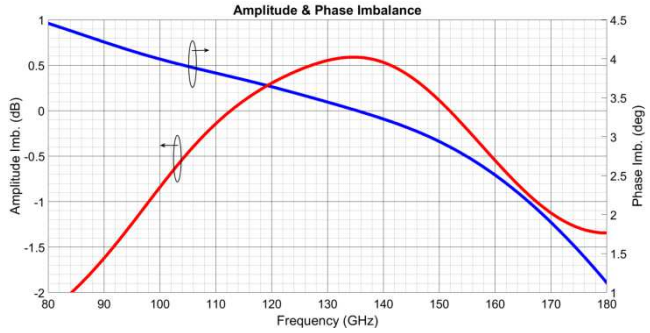

Fig 6. Simulated amplitude and phase imbalances of the designed MBL.

IV. CHIP FABRICATION &SIMULATION RESULTS

Figure 7 shows the photograph of the chip fabricated in 130 nm SiGe process from Infineon. The chip area is $1.150 \times 0.467\ mm^2$, including the MBLs and all the rf pads. The small/large- signal measurements for the presented D-band balanced cascode amplifier are pending.

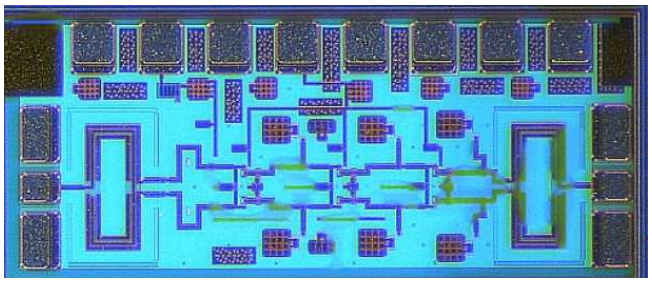

Fig 7. Chip photograph.

The simulated s-parameters of the total 3-stage PA design are presented in Figure 8. The S21 plot shows a 3dB bandwidth of 52 GHz, covering almost the entire D-Band and ensuring the wideband behavior of the presented PA. Moreover, the maximum S21 is almost flat at 32.5 dB, while $S11 < -18\,dB$ in the range $105 - 162$ GHz. The PA is unconditionally stable over all frequencies.

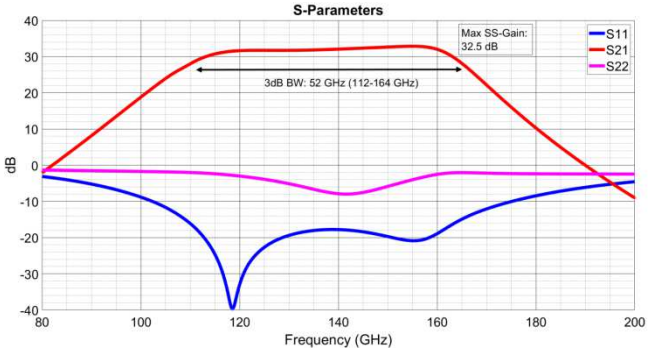

Fig 8. Simulated S-parameters of the designed PA.

As for the large-signal simulation (Fig. 9), the proposed PA exhibits a large signal $Power\ Gain > 32\,dB$ at the operating frequency of 145 GHz, as well as an output 1-dB compression point $OP_{1dB} \approx 9.7\,dBm$ and a saturation delivered power $P_{sat} \approx 12.4\,dBm$. Furthermore, Figure 10 shows the OP_{1dB} and P_{sat} over the D-band.The results denote that the designed PA performs high enough $OP_{1dB} > 7\,dBm$ and $P_{sat} > 9\,dBm$ for the whole band of interest. Other important specifications arising from our simulations results at 145 GHz, are the $IIP_3 \approx -14\,dBm$ as well as the $PAE \approx 5\,\%$. The power consumption (P_{DC}) of our PA approaches 345 mW.

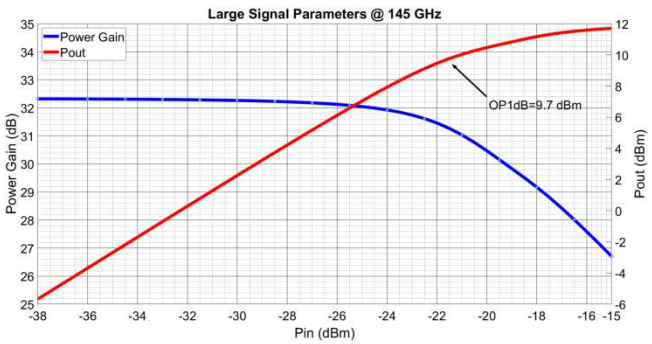

Fig 9. Simulated $Power\ Gain$ and P_{out} versus Input Power P_{in}.

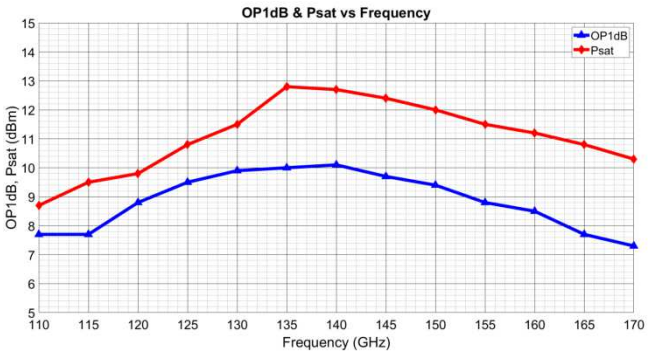

Fig 10. Simulated OP_{1dB} & P_{sat} over frequency.

Table II shows the performance summarization and the comparison with other state-of-the-art D-band PAs, fabricated in 130 nm SiGe processes.

TABLE II
COMPARISON TABLE OF PUBLISHED D-BAND PAS FABRICATED IN SIGE BICMOS PROCESS

Reference	BW (GHz)	f_T/ f_{max} (GHz)	Topology	SS-Gain (dB)	P_{sat} (dBm)	OP1dB (dBm)	PAE (%)	P_{DC} (mW)	Area (mm^2)
This Work**	52	250/370	3-stage differential	32.5	9-13	7-10	5	345	0.537
[12]*	60	300/500	3-stage single-ended	21	11.8-13.9	9.2-12.5	5.1	379	0.3
[6]*	49	250/300	5-stage differential	27	12-14	-	5.5	440	0.48
[13]*	80	250/370	4-stage differential	24.8	7.5-11	-	4.8	262	0.42
[14]*	25	300/500	4-way combining	30.2	18	15.6	4	-	0.85
[15]*	21	300/500	2-stage single-ended	16.7	15	11	7.8	300	0.44
[16]*,+	34	320/370	4-stage single-ended	24	17.6	16.8	17.5	286	0.18
[16]*,+	25	320/370	4-stage differential	22.4	19.3	18.5	13	-	0.26

* measurement results
** simulation results
+ 55 nm SiGe BiCMOS

V. CONCLUSION

This brief presents a high-gain, 3-stage, broadband PA, integrated in a 130 nm SiGe BiCMOS process, suitable for D-band applications. The cascode, pseudo-differential topology is used as the main amplifying core, while gm boosting technique is adopted for further gain enhancement. The PA achieves a record simulated power gain of 32.5 dB in an operating bandwidth of 52 GHz.

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