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Reduced switched seven level multilevel inverter by modified carrier for high voltage industrial applications

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ABSTRACT

Multilevel inverters are widely used in high-power and high-voltage applications due to their lower total harmonic distortion (THD), decreased switching stress on their switches, and other benefits. However, increasing the number of steps results in a drop in THD, which results in a larger size. As a result, a new 7-level reduced switched cascaded multilevel inverter (CMLI) has been designed for the current project. This architecture employs seven switches and seven levels of MLI to achieve the same output as a conservative multilevel inverter (MLI). To generate gate pulses for the switches, conventional and modified carriers were employed, and a third harmonic component was added into the sine wave to increase the fundamental output voltage. Finally, MATLAB or simulation is utilized to test the results of this task's design. According to the analysis, the proposed design may reduce harmonic distortion and improve the fundamental voltage component with fewer switches.

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1. INTRODUCTION

In today's world, businesses, industries, and households all want more and better electricity at lower costs. Because of this, the output voltage, current fundamental component, and total harmonic distortion are being improved by combining renewable energy sources with power electronics. An inverter that converts DC energy to AC with better efficiency is called a multilevel inverter. A typical voltage source inverter (VSI) used in medium and high power/voltage applications results in a decrease in performance. This is mostly due to the inverter's switches, which have certain limits for high-voltage applications, causing power loss. As a result, cascaded multilevel inverters (CMLIs) were established in order to address this issue. High- and medium-voltage applications benefit from the increased efficiency of these inverters. In this way, the implementation of multilevel inverters (MLIs) in enterprises has become commonplace. On the other side, when the MLI level rises, the total harmonic distortion (THD) will fall. However, as the number of power modules in the MLI grows, the isolation between switches and power supplies becomes more complicated.

Pires *et al.* [1] designed an high-voltage direct current (HVDC) transmission system based on twin three-phase, two-level inverters for multilevel power converters. Khounjahan *et al.* [2] first announced cascaded transformer MLI in 2015. In addition to the DC power supply and single-phase lower frequency transformer, there are two switches for switching power and a few additional bi-directional switches. Each

transformer is equipped with its own bidirectional switch. So far, the number of switches in various topologies has been reduced [3]–[40]. Babaei *et al.* [13] developed a unique cascaded MLI in 2015 that used five distinct algorithms to generate voltage at the output. CHMLI has a basic value of 268.9 V and a THD percentage of 26.24 percent, according to the literature. Previous research [15]–[17] compares conventional and unique pulse width modulation (PWM) for CMLI and t-type MLI. Prasadarao and Manohar [18] investigate PV-based symmetric and asymmetric MLI. Pretraining for the consequences of decreasing switching MLIs is included in [19]. Even after much research, two concerns remain unsolved: higher THD and fewer basic components. As a result, the current study presents a novel 7-level cascaded MLI with fewer switches to address all of these limitations. We intend to improve basic component value and THD performance by employing a novel carrier-based PWM technique. As a result, the proposed three-phase design includes seven switches in each phase to offer seven output levels. CMLI is chosen in this circumstance because it is more efficient than the other two MLI topologies. The gating signal for the switches in the PO-SPWM technology is provided by conventional carrier, modified carrier POSPWM, and third harmonic injected POSPWM (THI). In this MLI, only seven switches are required to produce seven different voltage levels.

2. DESIGN OF PROPOSED RSW SEVEN LEVEL CMLI TOPOLOGY

Figure 1 depicts the standard CMLI level, which comprises of bridge-arranged power electronics switches with a single-phase power supply input. The cascaded MLI level is denoted by M, while the number of H bridges and phases is denoted by n. With three H-Bridge connections, the output of the typical CMLI uses a total of 12 switches. Figure 2 depicts the MLI design presented in this paper.

$$n = (M - 1)/2 \quad (1)$$

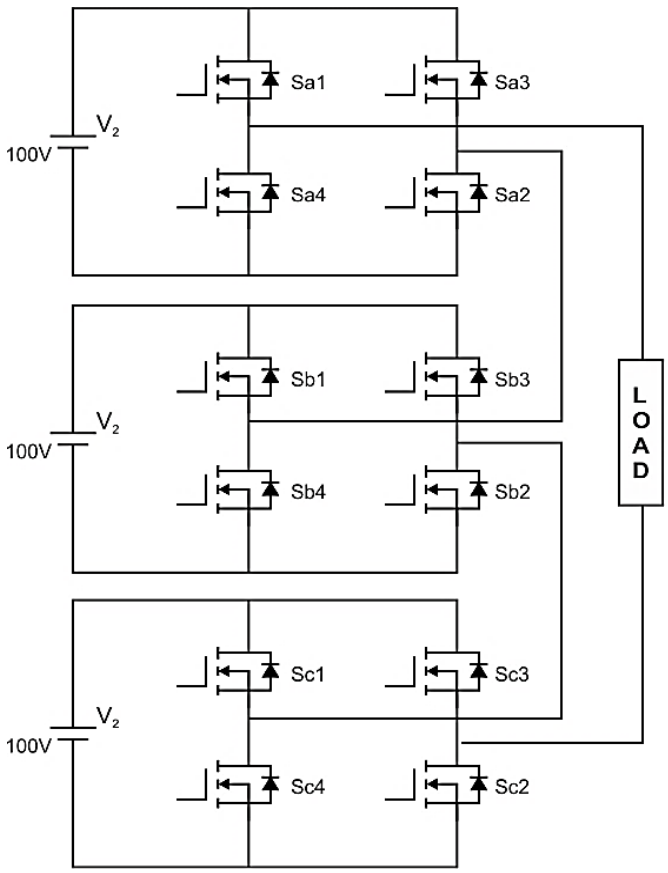


Figure 1. Conventional 7 level MLI (single phase)

Seven MOSFETS are used in this design to create a single phase. H-Bridge uses '3' MOSFETS for level generation, while H-Bridge uses '4' MOSFETS for shifting polarity. With seven possible settings (+1 V,

-1 V, -2 V, -3 V), it is capable of producing seven different voltage outputs. All of the MOSFETS are turned on for the +3 V output voltage, except for S5a, S6a, and S7a, which are all turned off. There are just two switches (S5a and S6a) in the ON position when it comes to the +2 V output voltage. Similarly, the MOSFETS (S5a) stay on while the other MOSFETS (S5b, S5c, and S5d) are turned off. Whereas s1a is used for the production of polarity. Table 1 shows the proposed MLI's switching system. The reduced switched-multi level inverter (RS-MLI) for seven level three phases is shown in Figure 2. Each phase contains three 100V voltage sources, three MOSFETS, and two diode switches. The suggested device has fewer switches than the current seven-level inverters. Costs, losses, and efficiency are all reduced if the number of switches is reduced. This model uses SPWM approach to compare conventional and novel carrier waves, which are both modulated at Mi=0.99 and mF=20, at fc=1 khz, with a load R=100 ohm, 70 mH with a modulation factor of 20. fc is the carrier frequency; fs is fundamental frequency. Table 1 shows that during conduction, only two switches stay on. Consequently, switching costs are considerably minimised.

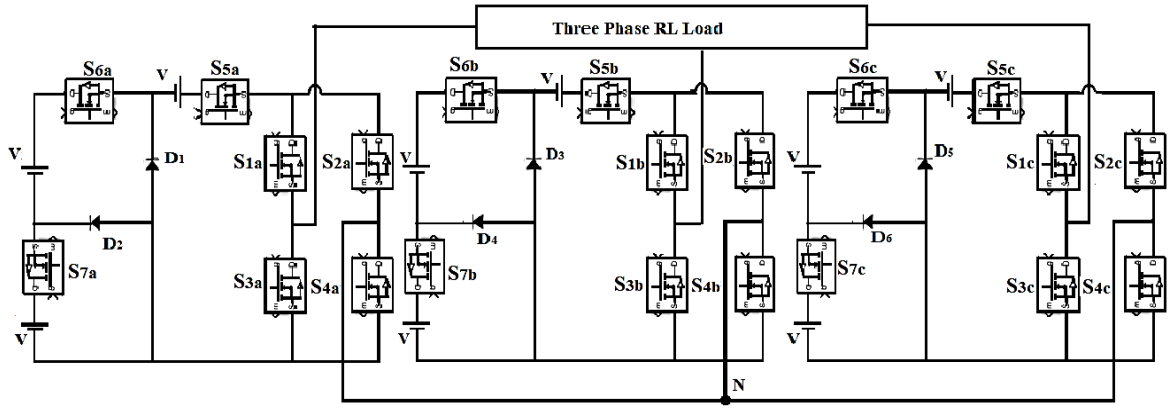


Figure 2. Three phases reduce switched seven level MLI for

Table 1. Switching sequence for RS-7-level 7-switched topology

S.NO	S1a	S2a	S3a	S4a	S5a	S6a	S7a	Output voltage
1	0	0	0	0	0	0	0	+0 Vdc
2	1	0	0	1	1	0	0	+1 Vdc
3	1	0	0	1	1	1	0	+2 Vdc
4	1	0	0	1	1	1	1	+3 Vdc
5	0	1	1	0	0	0	1	-Vdc
6	0	1	1	0	0	1	1	-2 Vdc
7	0	1	1	0	1	1	1	-3 Vdc

3. METHOD

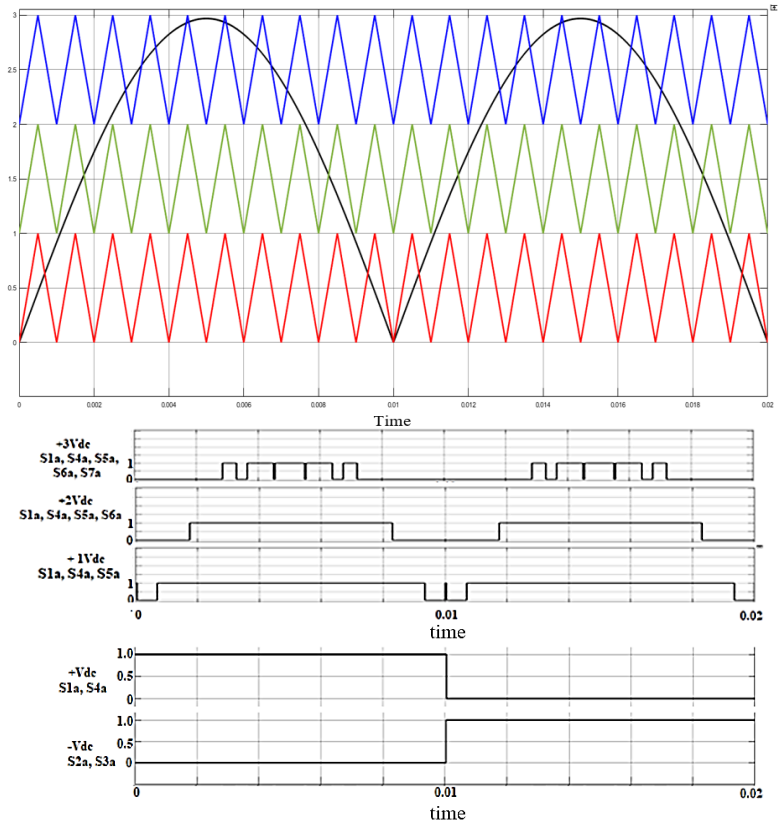
Many applications, such as control of IM, and PMSM, employ the SPWM approach. THD is reduced by using a reference sine wave and a trangular carrier. Typical and modified carrier waves are used to create seven levels of output, which is compared to a conventional cascaded MLI at mf=20, fc=1 kHz, Mi=0.99, R=100 ohms, L=70 m H in this study.

3.1. Convention carrier PO-SPWM technique

The traditional carrier wave PWM production is seen in Figure 3. One reference sine wave and three modified carrier waves comprise the unipolar PO SPWM approach shown in Figure 3(a), from which the pulse is formed in Figure 3(b).

3.2. Modified carrier PO-SPWM technique

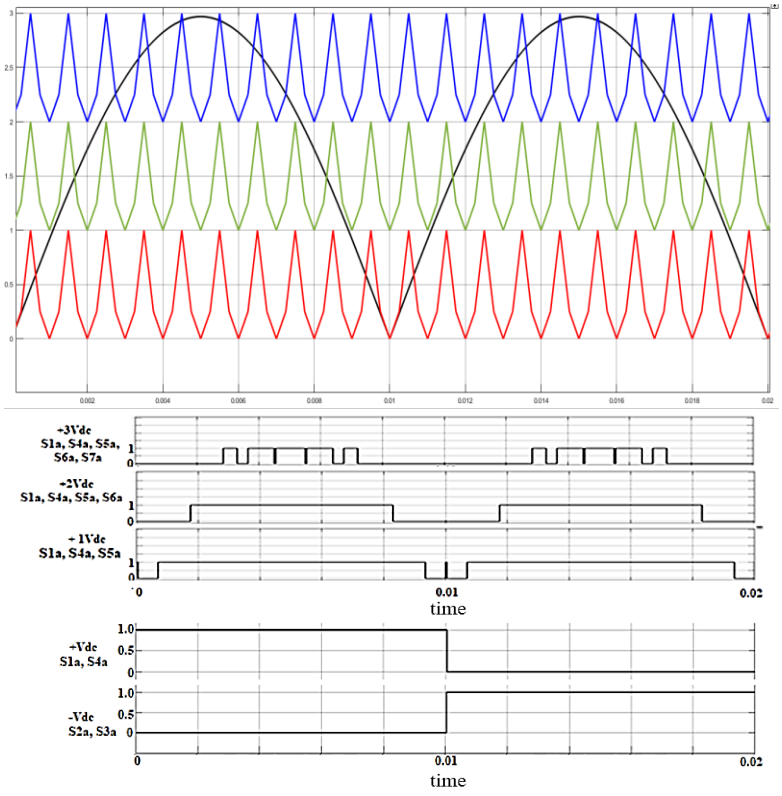
Figure 4 (in Appendix) depicts a new carrier PWM generating method. As shown in Figure 4(a), the pulse is created using a unipolar PO SPWM approach that utilizes a reference sine wave and three modified carrier waves Figure 4(b). New (or modified) triangular waves and a larger number of levels were used in this study to increase the performance of the fundamental value and percent THD. This triangular wave is also more suited for a seven-level inverter than a reference triangular wave.



(a)

(b)

Figure 3. The traditional carrier wave PWM production: (a) conventional carrier wave unipolar PO-SPWM technique and (b) pulse generation



(a)

(b)

Figure 4. PWM generating: (a) modified triangular-carrier wave unipolar PO-SPWM technique and (b) modified carrier wave pulse generation for proposed topology

3.3. Modified carrier PO-THI-SPWM technique

It is shown in Figure 5 how the new carrier PWM generation works. Unipolar PO-THI-SPWM approach has one reference THI sine wave and three modified carrier waves in Figure 5(a), whereas the pulse is created in Figure 5(b). This has the benefit of increasing the fundamental component at Mi=1. Figures 6(a) and 6(b) show the simulation results for phase-voltage, line-voltage, and load-current, as well as their co-related FFT spectrum (b). The benefit here is that the fundamental component is enhanced while the THD is minimized. Figure 7(a) shows the simulation results for phase voltage, line voltage, and load current, as well as the resulting fast Fourier transform FFT spectrum in Figure 7(b). Figure 8(a) shows the simulation results for phase-voltage, line-voltage, and load-current, and their FFT spectrum Figure 8(b).

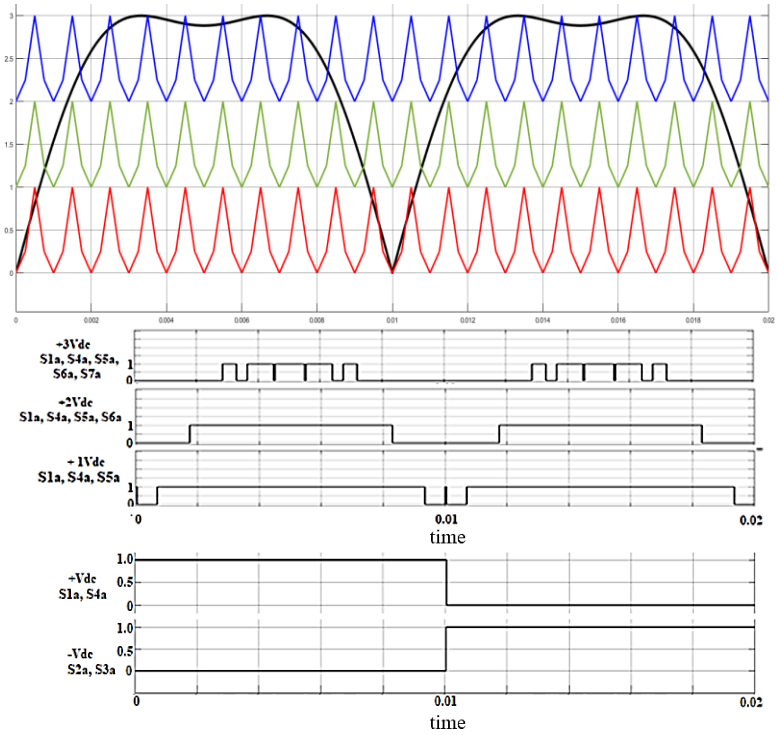
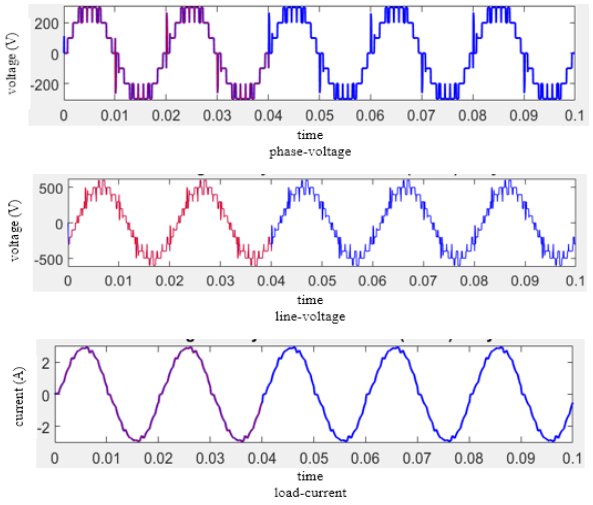


Figure 5. PWM generation works, (a) modified carrier wave unipolar PO-THI-SPWM technique, and (b) modified carrier wave pulse generation for proposed topology

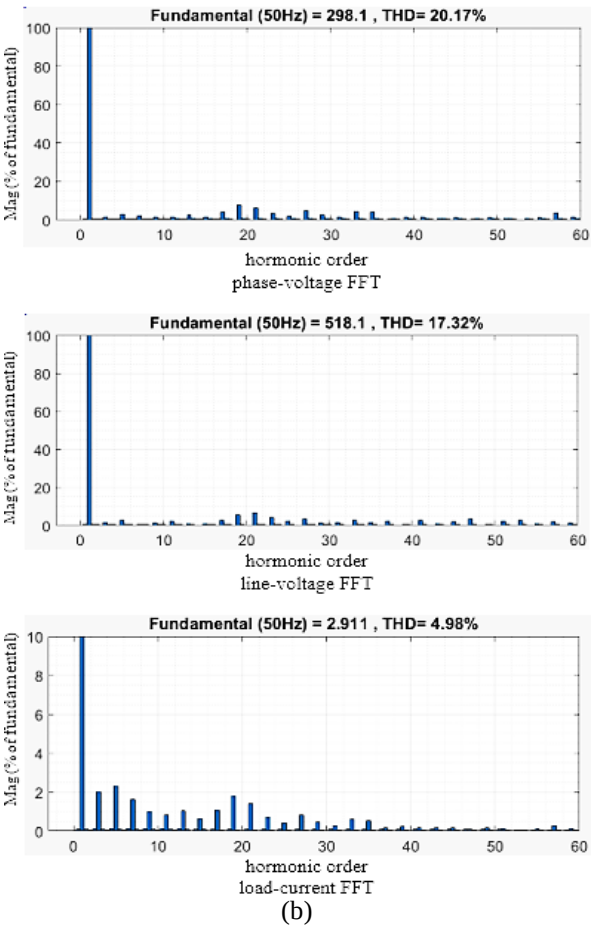
4. RESULTS AND DISCUSSION

A MATLAB simulation is used to evaluate the planned topology's performance. Figure 6(a) shows the output voltage, line voltage, and load current as well as their related FFT spectrum for the proposed three-phase conventional carrier wave PO-SPWM scheme. There is a 20.17 percent increase in phase voltage, a 17.32 percent increase in line voltage, and a 2.911 percent increase in load currents with THDs. Figure 7(a) shows the output voltage, line voltage, load current, and the related FFT spectrum for the suggested topology with modified carrier wave PO-SPWM for three phases, as well as the simulation results and THD. There is a 20.17 percent increase in phase voltage, a 17.46 percent increase in line voltage and a 5.38 percent increase in load current with THDs.

Conventional MLI setups and suggested MLI configurations have been compared in Table 2. With a modified carrier wave, THD is decreased to 19.90 percent, compared to 20.17 percent for traditional carrier waves. According to the structure of the proposed topology, it is compared to conventional topologies in Table 3. Table 2 shows that the proposed RSW-MLI has the greatest fundamental component value compared to the current CML inverters. Modified carriers PO-SPWM and THI-PO-SPWM achieved fundamental/Vrms values of 306 and 351.3 volts, respectively, in the proposed RSW-MLI. THD improvements are beneficial to high-voltage applications, especially in cases when a large voltage magnitude is needed. Tables 2 and 3 show that the suggested topology has greater benefits in terms of voltage magnitude than the standard topology. Because we're expanding the essential component's size with Novel Carrier, it's a win-win situation. Table 3 shows that losses are minimized during switches, as shown in [40].

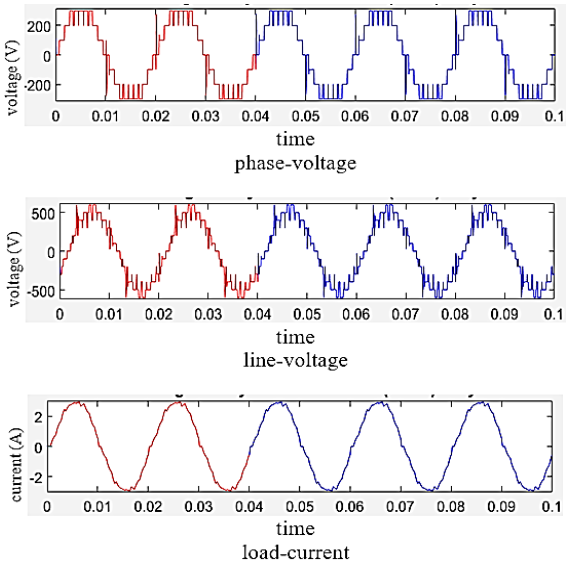


(a)

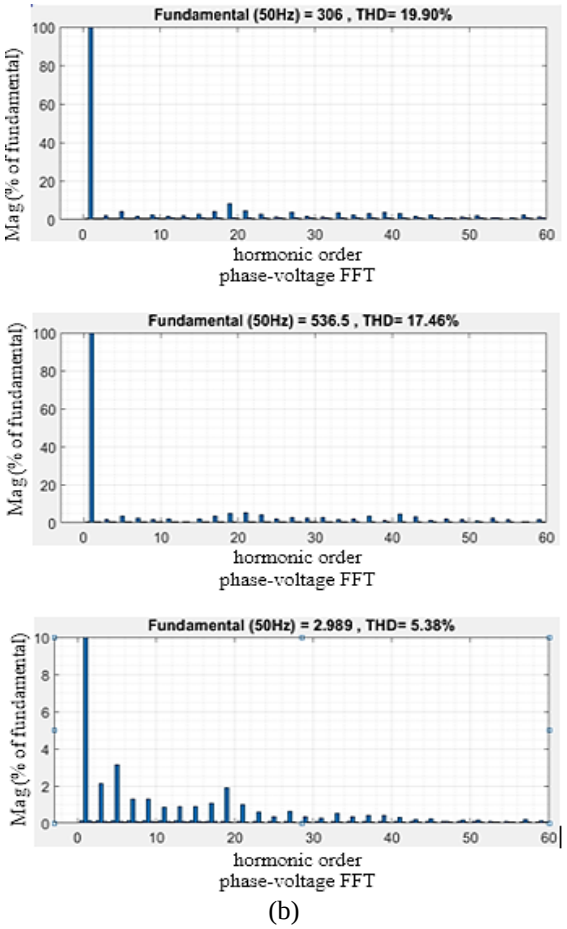


(b)

Figure 6. Simulation results for (a) phase-voltage, Line-voltage and load-current and (b) gives their corresponding FFT analysis at mf=20, r=100, L=70 mH, fc=1 kHz with conventional carrier wave PO-SPWM technique at Mi = 0.99

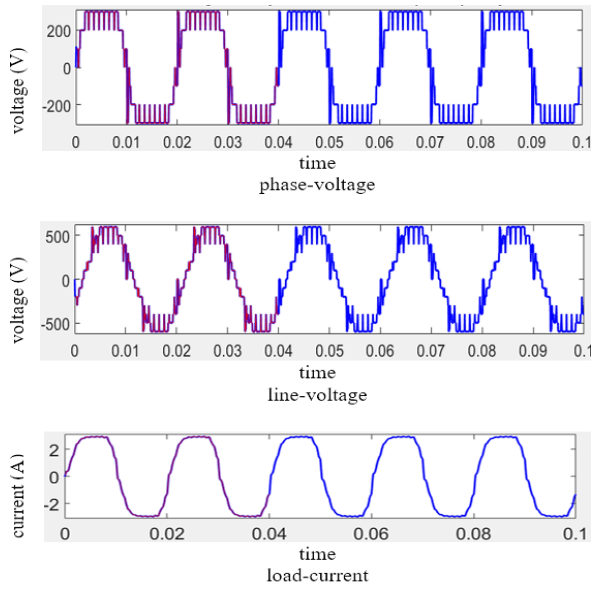


(a)

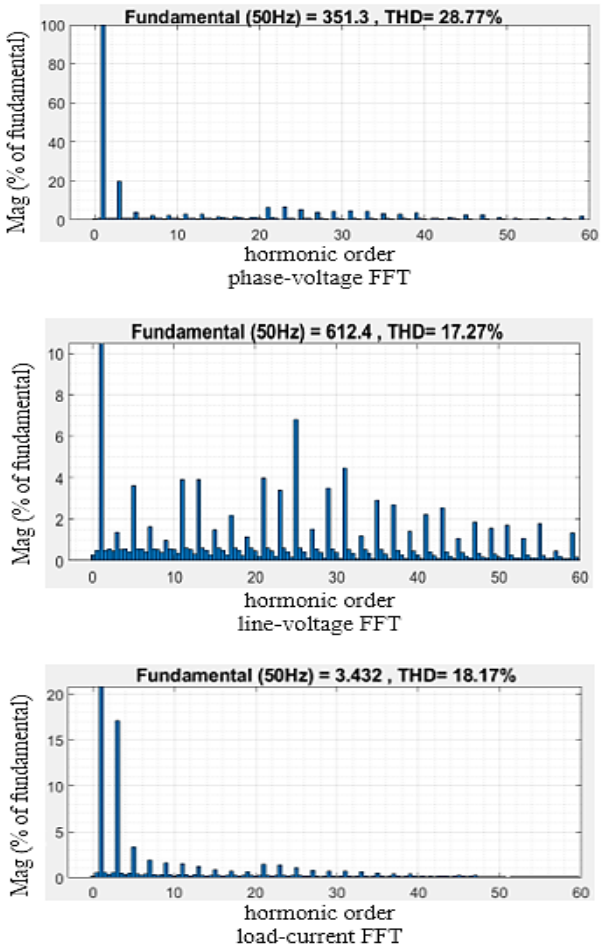


(b)

Figure 7. Simulation results for (a) phase-voltage, Line-voltage and load-current and (b) gives their corresponding FFT analysis at mf=20, r=100, L=70 mH, fc=1 kHz with modified carrier wave PO-SPWM technique at Mi=0.99



(a)



(b)

Figure 8. Simulation results for (a) phase-voltage, line-voltage and load-current and (b) gives their corresponding FFT analysis at mf=20, r=100, L=70 mH, fc=1 kHz with modified PO-THI-SPWM technique at modulation index (Mi)=1

Table 2. Comparison of fundamental, THD of conventional and proposed MLI for seven level

Existing conventional CMLI						RSW- MLI proposed					
Conventional CHMLI		[20]		[19]							
Conventional carrier (SPWM)		Method #1	Method #2	Conventional 12 switch MLI	Three states carrier APOD-PWM	Conventional carrier (SPWM)		Modified carrier (PO-SPWM)		Modified carrier (THI-PO-SPWM)	
Fundamental value (Vrms)	THD (%)	THD (%)	THD (%)	Vrms (V)	Vrms (V)	Vrms (V)	THD (%)	Vrms (V)	THD (%)	Vrms (V)	THD (%)
268.9	26.24	31.35	25.46	296.3	297.6	298.1	20.17	306	19.90	351.3	28.77

Table 3. Comparison of proposed topology with other MLI topology [40]

Inbuilt structure	Flying capacitor	Diode clamped	Cascaded 7-level	7-level, switches (new)
No. of Capacitors	14	6	-	-
No. of Diodes	-	≥8	-	-
No. of Switches	10	10	12	7
No. of dc sources	-	-	3	3

5. CONCLUSION

The paper proposed a novel 7-level cascaded MLI with fewer switches. The 7 switches are used to create a 7-level MLI that produces the same output as a regular one. With the PO-SPWM method, the gate pulse is generated. The results of this study show that the suggested system reduces switching components with reduced THD and a higher fundamental output component. As a result, the overall cost is reduced and total harmonic distortion (THD) is effectively reduced, particularly at higher voltages.

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