Faster-Than-Real-Time Dynamic Simulation of AC/DC Grids on Reconfigurable Hardware

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Abstract—Dynamic simulation of integrated AC and DC grids is paramount to address real-time operation challenges in energy control centers, such as available transfer capacities, relieving grid congestion, and taking effective control actions for improving the integrated grid system stability and reliability. This paper proposes a faster-than-real-time (FTRT) dynamic simulation of integrated AC/DC grids on the reconfigurable parallel hardware architecture of the field programmable gate array (FPGA). A fine-grained relaxation algorithm (FGRA) is proposed for a more efficient solution of the nonlinear differential algebraic equations of the integrated system model, including the detailed nonlinear models of the synchronous generators in the AC system which can be solved in parallel without matrix on the FPGA. The system solution is massively parallelized and pipelined in hardware to realize the lowest latencies and minimum utilization of hardware resource. Two case studies are used to illustrate the efficacy of the proposed algorithm and demonstrated a closed-loop prediction scenario for improving grid stability. Computational acceleration of up to 134 times faster than real-time are reported for the two case studies, and the accuracy of the dynamic interaction is validated using the off-line transient stability simulation tool TSAT of the DSATools package.

Index Terms—AC/DC grid, dynamic simulation, faster than real time, field-programmable gate array (FPGA), fine-grained relaxation, modular multi-level converter (MMC), parallel processing, predictive control, real-time systems, synchronous generator.

I. INTRODUCTION

THE proportion of renewable energy has been increasing significantly worldwide due to enhanced environmental standards, bringing with it a host of technical and operational challenges. Restrictions on available transfer capacities leading to severe congestion of major transmission and distribution corridors has been the most common problem, with severe consequences related to voltage and frequency regulation, and transient stability and reliability of the grid. Building new transmission facilities is the only viable long-term solution to assuage the impacts of renewable energy penetration, and increasingly electric utilities are opting to construct new DC transmission lines. With modular multi-level converter (MMC) technology

as the foundation, multi-terminal DC grids have enabled the transfer of large amounts of power, and interconnection of asynchronous AC systems [1], [2]. With varying submodule topologies, MMCs offer faster controllability, higher redundancies, and better fault-tolerant capability [3], [4]. In this scenario, tools for dynamic simulation of integrated AC/DC networks are indispensable. In particular, a faster-than-real-time (FTRT) dynamic simulation tool deployed in the energy control center can accelerate planning schedules, assess the impact of excessive energy penetration at critical locations, predict destabilizing outages, devise newer control strategies, and enhance the overall security and reliability of the grid.

Conventionally, transient stability simulation of AC systems involves the time-domain solution of a set of nonlinear differential algebraic equations (DAEs). The differential equations correspond to the synchronous machine models, and the algebraic equations correspond to the network. For dynamic security assessment (DSA) these simulations are run for a set of critical contingencies [5]–[7]. The differential equations may be discretized by either explicit and implicit numerical integration methods, resulting respectively in a separate (iterated) or simultaneous solution of the machine and network equation sets. The iterative schemes commonly employed are the Gauss-Seidel (G-S), the Newton-Raphson (N-R), or the Very Dishonest Newton (VDHN) methods with their corresponding pros and cons influencing the accuracy, convergence rate, and computational burden of the overall simulation [8], [9]. For large-scale systems, invariably, the computation is distributed over parallel processors by employing domain decomposition and relaxation schemes in space, time, or both dimensions [10]–[12]. Hitherto, large-scale transient stability implementations have been carried out on clusters of CPUs and GPUs for efficient simulation or even real-time execution [14], [16], [17], and dense or sparse libraries are utilized for matrix equation solution in the simulation.

Over the last 10 years there has been tremendous development in reconfigurable hardware logic devices that are FPGAs, in both their VLSI architecture and CAD software tools, that has enabled them to become mainstream processors in many industrial areas. Currently available Ultrascale FPGAs from Xilinx are 16 nm devices with a maximum of 3.8 M system and programmable logic cells, 12,288 DSP slices, and 32.75 GB/s maximum transceiver speed. These features are expected to grow even more in the future. For power systems and power electronic systems, FPGAs have been used in real-time hardware-in-the-loop (HIL) application for detailed device-level modeling of various equipment [18], [19].

In this work, a fine-grained relaxation algorithm (FGRA) is proposed for FTRT dynamic simulation of integrated AC/DC networks on the massively parallel reconfigurable hardware architecture of the FPGA. The floating point operations carried out at the smallest resolution of the proposed algorithm are scalar in nature and any matrix operations are completely avoided. The AC/DC system component models undergo a fully decoupled parallel solution. High parallelism and pipelining is achieved for the FTRT hardware emulation on the Xilinx Virtex UltraScale+ XCVU9P FPGA. Two case studies are emulated to provide insight into the performance of the proposed algorithm.

The rest of the paper is organized as follows: Section II introduces the background of transient stability simulation, and the proposed fine-grained relaxation algorithm. The detailed modeling of the integrated AC/DC grids is specified in Section III, followed by Section IV which demonstrates the hardware design on the FPGA. The simulation results and their comparative analysis with off-line simulations using TSAT are shown in Section V. Section VI presents the conclusion and prospective work.

II. ITERATIVE FINE-GRAINED RELAXATION ALGORITHM FOR DYNAMIC SIMULATION

A. Formulation of Transient Stability Problem

The power system dynamic simulation for transient stability analysis is basically solving the following set of differential algebraic equations (DAEs):

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}, \mathbf{u}, t), \tag{1}$$

$$\mathbf{g}(\mathbf{x}, \mathbf{u}, t) = 0, \tag{2}$$

where $\mathbf{x}$ and $\mathbf{u}$ are vectors of the state variables and the bus voltages, respectively. Prior to the start of the simulation, as always required, the boundary conditions should be given,

$$\mathbf{x}_0 = \mathbf{x}(t_0). \tag{3}$$

A typical power system undergoing dynamic simulation is mainly composed of synchronous generators, buses, transmission lines, and various loads. The differential equation (1) describes the dynamics of all synchronous generators, while the remaining components contribute to the algebraic equation which solves the network in conjunction with stator voltages of the machines. Noticing that the state variables of all synchronous generators form one vector $\mathbf{x}$, and so is $\mathbf{u}$ that contains all bus voltages, it is obvious that a larger power system results in a DAE with higher dimension, which means the solution process consequently turns out to be more inefficient. For example, for the power system with m machines and n buses, the vector $\mathbf{x}$ is $9m$-dimensional since a synchronous generator in this study has 9 state variables, and so is the vector $\mathbf{u}$ which is $2 \cdot n$ of size when the system is studied under the d-q frame.

B. Traditional Solution Methodology

In the traditional proceeding of the dynamic simulation, solving the differential equation accounts for the major computational burden since it follows [20]:

1) Discretization: The continuous differential equation should be discretized prior to its solution, e.g., the corresponding time-discrete nonlinear algebraic equation can be obtained after applying the Trapezoidal rule:

$$\mathbf{F}(\mathbf{z}) = \frac{\Delta t}{2}[\mathbf{f}(\mathbf{x}, \mathbf{u}, t) + \mathbf{f}(\mathbf{x}, \mathbf{u}, t + \Delta t)] - [\mathbf{x}(t + \Delta t) - \mathbf{x}(t)], \tag{4}$$

where $\mathbf{z} = [\mathbf{x}, \mathbf{u}]$, and Δt is the simulation time-step.

2) Nonlinear Algebraic Equation Formation: The N-R iteration method is applied to the aforementioned nonlinear algebraic equation and consequently leads to

$$\mathbf{J}(\mathbf{z}_i) \cdot \Delta \mathbf{z} = -\mathbf{F}(\mathbf{z}_i), \tag{5}$$

where the subscription i is the iteration time, $\mathbf{J}$ refers to the Jacobian matrix whose elements are obtained by the partial derivative of the 9th-order state variable functions, and $\Delta \mathbf{z} = \mathbf{z}_{i+1} - \mathbf{z}_i$.

3) Linear Algebraic Equation Solution: The formation of (5) allows deriving the state variables using traditional linear equation solvers such as Gaussian Elimination and LU decomposition. The simulation speed is deeply affected by the type of solver employed, especially considering the scale of power system always results in a huge matrix equation which often causes a heavy computational burden.

4) Update of Jacobian Matrix: Following the solution, the Jacobian matrix which is changing in every iteration can be updated for the preparation of next iteration or – if the results are convergent – the next time-step.

C. Proposed Fine-Grained Relaxation Algorithm

The adoption of a traditional linear solver for nonlinear equation solution falls short of efficiency, particularly in utilizing the processor's parallelism. The FGRA is thereby proposed to fully exploit the FPGA's parallel hardware architecture by introducing concurrency in solving the $9m$-D matrix equation.

Congregating the 9 state variables of all the synchronous generators as a basic vector unit $\mathbf{x_i}$ in an m-machine system where each one is connected to an individual bus will lead to a diagonal matrix equation expressed as

$$\begin{bmatrix} \Delta \mathbf{x_1} \\ \Delta \mathbf{x_2} \\ \Delta \mathbf{x_3} \\ \vdots \\ \Delta \mathbf{x_m} \end{bmatrix} = \begin{bmatrix} \mathbf{J_1} & 0 & 0 & \cdots & 0 \\ 0 & \mathbf{J_2} & 0 & \cdots & 0 \\ 0 & 0 & \mathbf{J_3} & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & 0 & \mathbf{J_m} \end{bmatrix}^{-1} \begin{bmatrix} -\mathbf{F_1} \\ -\mathbf{F_2} \\ -\mathbf{F_3} \\ \vdots \\ -\mathbf{F_m} \end{bmatrix}, \tag{6}$$

where $\Delta \mathbf{x_i}$ and $-\mathbf{F_i}$ are 9×1 vectors, and $\mathbf{J_i}$ is a 9×9 matrix. In typical dynamic simulations, all synchronous generators are located on different buses, i.e., one swing bus and the remaining are PV buses, which means the generators are fully independent from each other resulting in non-diagonal elements in the Jacobian matrix are all 0, and therefore the equation can be decomposed into m 9-D matrix equations.

The second level of parallelism is achieved by further decomposing the 9-D matrix equation which solves the state variables

of a single generator. Taking the form of

$$
\begin{bmatrix} \Delta x_1^{n+1} \\ \Delta x_2^{n+1} \\ \Delta x_3^{n+1} \\ \vdots \\ \Delta x_9^{n+1} \end{bmatrix} = \begin{bmatrix} J_{11}^n & J_{12}^n & J_{13}^n & \cdots & J_{19}^n \\ J_{21}^n & J_{22}^n & J_{23}^n & \cdots & J_{29}^n \\ J_{31}^n & J_{32}^n & J_{33}^n & \cdots & J_{39}^n \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ J_{91}^n & J_{92}^n & J_{93}^n & \cdots & J_{99}^n \end{bmatrix}^{-1} \begin{bmatrix} -f_1^n \\ -f_2^n \\ -f_3^n \\ \vdots \\ -f_9^n \end{bmatrix}, \quad (7)
$$

In a specific iteration the Jacobian matrix and function f_i are constant. As mentioned above, the traditional methodology has to calculate at least m times of 9×9 matrix inversion, which poses a severe challenge to realizing the fast-than-real-time simulation. An arbitrary state Δx_i can be derived as

$$
J_{11}^n \Delta x_1^{n+1} + J_{12}^n \Delta x_2^n + \cdots + J_{19}^n \Delta x_9^n = -f_1^n,
$$

$$
J_{21}^n \Delta x_1^n + J_{22}^n \Delta x_2^{n+1} + \cdots + J_{29}^n \Delta x_9^n = -f_2^n,
$$

$$
\vdots
$$

$$
J_{91}^n \Delta x_1^n + J_{92}^n \Delta x_2^n + \cdots + J_{99}^n \Delta x_9^{n+1} = -f_9^n, \quad (8)
$$

$$
\Delta x_i^{n+1} = \frac{-f_i^{n-1} - \sum_{j \neq i}^{j=1-9} J_{ij}^n \Delta x_j^n}{J_{ii}^n}. \quad (9)
$$

where the superscription n denotes the count of Newton-Raphson iteration which is required since the state variable to be solved is built upon the history values of its counterparts, but no extra N-R iteration loop should be introduced since it already existed due to the nonlinear characteristic of the DAE. (9) shows that every arbitrary Δx_i is only related to the ith row in the Jacobian matrix **J**. Generally, the Jacobian matrix is sparse; therefore, we can further substitute (9) via eliminating the zero coefficients. This approach can significantly shrink the calculation time and reduce the hardware resources. Moreover, the fact that the synchronous generator is a nonlinear component means that the coefficients have to be updated within every iteration. The terms with superscription $n + 1$ can be set as initial values or updated from the last iteration.

Compared with traditional Waveform Relaxation [13] and its evolutive algorithms [14], [15], FGRA has the advantages of low iteration and usage of hardware resource. The proposal of (9) enhances parallelism as it can be seen that the original matrix equation with a dimension of $9m$ solved using traditional matrix solution methods is decomposed into $9m$ algebraic equations which, due to mutual independence, is suitable for hardware parallelism on the FPGA board.

III. AC/DC GRID COMPONENTS MODELING

A. AC/DC Grid Interface

Fig. 1 shows a typical integrated AC/DC grid as the 1st case of dynamic-electromagnetic transient (EMT) co-simulation for analyzing system stability. The 3-terminal HVDC system that undergoes EMT simulation is linked to its AC counterpart via Bus 7 and 9, and considering that it is EMT simulation, a time-step of 200 μs is adopted to reveal more details as well as to keep the computation convergent; whilst the AC grid subjected
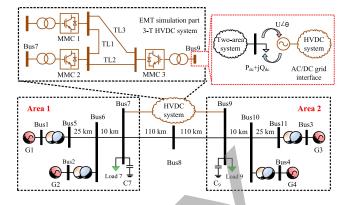

Fig. 1. Case 1: integrated AC/DC grid for dynamic-EMT co-simulation.

to stability analysis is based on Kundur's two-area system which has 4 synchronous generators in addition to 11 buses. The dynamic simulation focuses on the transient stability of the synchronous machines and network data with a large time-step of 10 ms, 50 times that of the EMT simulation. Therefore, in order to establish the co-simulation with a unified time scheme, the AC system synchronizes the active power data with the DC side after the EMT simulation calculates 50 steps. Therefore the AC system solves a new admittance matrix before the iteration in every time-step.

Since different simulation algorithms are applied to the AC and DC systems, an interface is introduced to enable the two types of simulation compatible in one program. However, the HVDC stations denoted by $MMC_1 \sim MMC_3$ are dynamic processes, regardless of the type, i.e., rectifier or inverter, which can be modeled as time-varying $P + jQ$ loads, or to be more specific, both P and Q values are updated in every time-step to reflect the real dynamic process on the point of common coupling (PCC), as shown in Fig. 1. The mechanism of the interface is as follows, after the introduction of the AC/DC grid interface, the AC grid dynamic simulation is concurrent with its EMT counterpart with the former type of simulation yields the PCC voltage in every time-step for the latter to proceed. In return, the DC grid undergoing EMT simulation provides the power P + jQ to the AC grid in the same manner. Therefore, both the PCC voltage and the power are not constant and the dynamic processes is enabled. Furthermore, in dynamic simulation, the HVDC stations are taken as loads so that the bus phase voltages $U \angle \theta$ can be obtained; on the other hand, the instantaneous bus voltages are calculated to keep the EMT simulation going on and consequently the power of each station can be derived and returned to the AC grid.

B. AC Grid Modeling

1) Synchronous Machine Model: The differential equation (1) containing the dynamics of a synchronous generator has 9 types of state variables, i.e., in the equations of motion

$$
\dot{\delta} = \omega_R \cdot \Delta \omega(t), \quad (10)
$$

$$
\dot{\Delta \omega}(t) = \frac{1}{2H}[T_e + T_m - D \cdot \Delta \omega(t)], \quad (11)
$$

in the rotor electrical circuit equations which include 2 windings on the d-axis and 2 damping windings on the q-axis

$$\dot{\psi}_{fd}(t) = \omega_R \cdot [e_{fd}(t) - R_{fd}i_{fd}(t)], \tag{12}$$

$$\dot{\psi}_{1d}(t) = -\omega_R \cdot R_{1d}i_{1d}(t), \tag{13}$$

$$\dot{\psi}_{1q}(t) = -\omega_R \cdot R_{1q}i_{1q}(t), \tag{14}$$

$$\dot{\psi}_{2q}(t) = -\omega_R \cdot R_{2q}i_{2q}(t), \tag{15}$$

and in the excitation system which includes an AVR and PSS

$$\dot{v}_1(t) = \frac{1}{T_R} \cdot [v_t(t) - v_1(t)], \tag{16}$$

$$\dot{v}_2(t) = K_{stab} \cdot \Delta\dot{\omega}(t) - \frac{1}{T_\omega}v_2(t), \tag{17}$$

$$\dot{v}_3(t) = \frac{1}{T_2} \cdot [T_1\dot{v}_2(t) + v_2(t) - v_3(t)]. \tag{18}$$

Therefore, the vector $\mathbf{x}$ is repetitive when multiple synchronous generators exist in the power system, with a basic 9-D unit for a single generator as

$$\mathbf{x} = [\delta, \Delta\omega, \psi_{fd}, \psi_{1d}, \psi_{1q}, \psi_{2q}, v_1, v_2, v_3]. \tag{19}$$

In the stator, neglecting the transformer voltage terms and the effect of speed variations as it is justified to do so in the stability analysis [21], the equations turn out to be

$$e_d(t) = -R_ai_d(t) + L_q''i_q(t) - E_d''(t).$$

$$e_q(t) = -R_ai_d(t) + L_d''i_d(t) - E_q''(t). \tag{20}$$

2) AC Network Model: The AC network mainly includes transmission lines and loads. The former is modeled by a π section, while the latter is discounted into admittance attached to the bus, given as

$$Y_{Load} = \frac{(P_{Load} + j \cdot Q_{Load})}{V_{Bus}^2}, \tag{21}$$

where P_{Load} and Q_{Load} refer to the active and reactive power of the load, respectively, and V_{Bus} is the absolute voltage value of a bus to which the load is connected.

3) Machine Network Interfacing: The generator's stator equations are solved together with the AC network using the following matrix equation

$$\begin{bmatrix} \mathbf{I_m} \\ \mathbf{I_r} \end{bmatrix} = \begin{bmatrix} \mathbf{Y_{mm}} & \mathbf{Y_{mr}} \\ \mathbf{Y_{rm}} & \mathbf{Y_{rr}} \end{bmatrix} \begin{bmatrix} \mathbf{V_m} \\ \mathbf{V_r} \end{bmatrix}, \tag{22}$$

where m is the number of synchronous generator nodes, r is the number of remaining nodes. Absence of current injection into the non-generator buses means $I_r = [\mathbf{0}]$ and

$$\mathbf{I_m} = \mathbf{Y_R}\mathbf{V_m}, \tag{23}$$

where $\mathbf{Y_R} = \mathbf{Y_{mm}} - \mathbf{Y_{mr}}\mathbf{Y_{rr}^{-1}}\mathbf{Y_{rm}}$ is the reduced admittance matrix of $m \times m$ dimension. Under the D-Q frame,

$$\mathbf{I_{Dm}} = \mathbf{G_m}\mathbf{V_{Dm}} - \mathbf{B_m}\mathbf{V_{Qm}},$$

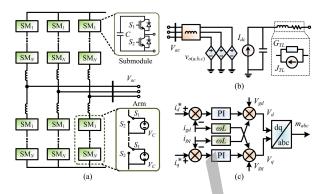$$\mathbf{I_{Qm}} = \mathbf{G_m}\mathbf{V_{Qm}} + \mathbf{B_m}\mathbf{V_{Dm}}, \tag{24}$$

Fig. 2. Three-phase MMC as an HVDC converter: (a) Circuit configuration, (b) average value model, and (c) current controller in d-q frame.

where $\mathbf{G_m}$ and $\mathbf{B_m}$ are the real and imaginary part of the reduced admittance matrix, respectively. The relationship between the voltage and current is

$$V_D = I_D \cdot u_1 + I_Q \cdot u_2 + u_5,$$

$$V_Q = I_D \cdot u_3 + I_Q \cdot u_4 + u_6, \tag{25}$$

where u_{1-6} can be calculated from the state variables. Following the acquirement of new state variables the relationship between $\mathbf{I_m}$ and $\mathbf{V_m}$ can be ascertained. Meanwhile, the matrix $\mathbf{Y_R}$ can be obtained from the original admittance matrix, and only $\mathbf{I_m}$ is yet to be solved in (23). Then, the rotor current and voltage in d-q frame can be derived according to their D-Q common frame counterparts, i.e.,

$$i_{dq} = I_{DQ} \cdot e^{-j\delta},$$

$$e_{dq} = V_{DQ} \cdot e^{-j\delta}. \tag{26}$$

The variables i_{dq} and e_{dq} lay foundation for calculating the voltages including their phases at non-generator nodes, the power flow, etc.

C. DC Grid Modeling

1) Modular Multilevel Converters: Fig. 2(a) shows a 3-phase $(N + 1)$-level MMC operating as an HVDC grid terminal. Within a half-bridge submodule, there are 2 IGBTs and a DC capacitor. When the upper switch S_1 is turned on, the capacitor is inserted; otherwise, it is bypassed. Therefore, the Thévenin equivalent circuit of a submodule can be expressed by

$$v_{SM} = \int \left(V_{g1} \cdot \frac{i_{arm}}{C}\right) dt + i_{arm} \cdot r_{on}, \tag{27}$$

where i_{arm} means the MMC arm current, V_{g1} is a binary denoting the gate signal of the upper switch S_1, and r_{on} represents the on-state resistance of the switch.

a) MMC average value model: For predictive regulation of the hybrid AC/DC grid, a high faster-than-real-time ratio is preferred, making the MMC average value model (AVM) given in Fig. 2(b) attractive for its simplicity and capability of being interactive with a basic converter controller to study its impact on the primary system.

In the MMC AVM, the 3 phases, the upper and lower arms, and the submodule capacitor voltages are assumed well-balanced [22]. Therefore, a submodule can be represented by a controlled voltage source, as

$$v_{SM} = V_{g1} \cdot \frac{V_{dc}}{N}, \qquad (28)$$

which means when the upper switch is under on-state, $V_{g1} = 1$ and the submodule output voltage is V_{dc}/N; when the submodule is bypassed, the output voltage is 0. Then, on the ac side, the output voltage of an arm is

$$v_{u,d} = \frac{V_{dc}}{N} \sum_{i=1}^{N} V_{g(u,d)(i)}. \qquad (29)$$

Since the circulating current is assumed to be 0 in the AVM, the output voltage on the AC side can be calculated as

$$v_{o(a,b,c)} = \frac{V_{dc}}{N} \sum_{i=1}^{N} (V_{gu(i)} - V_{gd(i)}), \qquad (30)$$

which further simplifies an MMC phase as a voltage source to reduce the number of nodes in the EMT simulation to achieve the maximum possible speedup over real-time.

b) MMC fully detailed model: To gain a higher accuracy, the fully detailed model is adopted. The conventional method considering the IGBT and its anti-parallel diode as a gate-signal-controlled two-state resistor falls short of revealing correct system performance when the DC line fault occurs. To avoid that, the unidirectional feature of the diode is taken into account, i.e., when the anode potential is higher than that of the cathode, the diode conducts, otherwise, it is under OFF state. The improvement in the switch model is accompanied by adopting the N-R iteration, which makes the computation more burdensome than the AVM. However, the configuration can be significantly simplified by circuit partitioning which separates all submodules containing nonlinear elements from the arm to constitute individual subsystems that can be computed independently on the parallel processor.

2) MMC Controller: The MMC adopts a two-loop control scheme in which the outer-loop controller is in charge of converter functions, e.g., regulation of the active/reactive power and the AC bus voltage, which yields the reference current $i_{d,q}^*$ under the d-q frame:

$$i_{d,q}^* = K_p(T_{ar}^* - T_{ar}) + K_i \int (T_{ar}^* - T_{ar}) dt, \qquad (31)$$

where K_p and K_i are constants, T_{ar}^* and T_{ar} represent the control target and the actual output, respectively. The current controller given in Fig. 2(c) is the core part which amplifies the current error to gain the voltage $V_{d,q}$, which is then converted to the 3-phase signals m_{abc} that are sent to the MMC inner-loop controller employing phase-shift strategy [23].

3) DC Network Model: The MMC DC side is represented by a current source in parallel with a capacitor. The injected DC current is

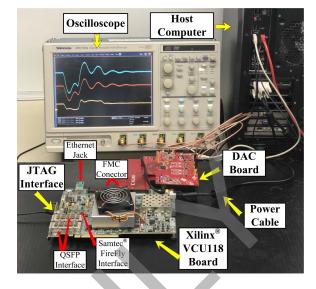$$I_{dc} = \frac{\eta P_{ac}}{V_{dc}} = \frac{3\eta(V_d I_d + V_q I_q)}{2V_{dc}}. \qquad (32)$$

Fig. 3. Hardware setup for FTRT simulation.

where η is the converter efficiency, and $V_{d,q}$, $I_{d,q}$ are the AC side voltage and current in d-q frame.

The DC transmission lines are represented by the π model, the parasitic capacitance is merged with the MMC DC side capacitor, while the internal node in the series R-L is eliminated by expressing the Norton equivalent circuit as

$$G_{TL} = \left(\frac{2L_{dc}}{dt} + R_{dc} \right)^{-1}, \qquad (33)$$

$$J_{TL} = 2v_L^i \cdot \left(\frac{2L_{dc}}{dt} + R_{dc} \right)^{-1}, \qquad (34)$$

where v_L^i is the incident pulse of the inductor modeled as a section of lossless transmission line [24].

IV. HARDWARE EMULATION ON FPGA

The emulation of integrated AC/DC grids is conducted on the Xilinx Virtex UltraScale+ XCVU9P FPGA board which has 1182240 look-up tables (LUTs), 2364480 flip-flops (FFs), and 6840 DSP slices to accommodate various hardware designs. The parallelism and pipelined designed approach enables a high FTRT ratio for system performance prediction and subsequently appropriate regulations which help to stabilize the power system. The package Xilinx Vivado allows designing hardware modules by coding in C/C++ in its high-level synthesis (HLS) tool to shorten the design cycle, and the AC/DC grid given in Fig. 1 is taken as an example since other configurations also conform to the same hardware design principle, i.e., the modularity, which means each of the power system components, or functions such as the FGRA, is written as an individual C/C++ function and then transformed into a hardware module in HLS that can be imported into Vivado to form the top-level using the hardware description language VHDL. Fig. 3 shows the hardware configuration for the FTRT simulation.

In this work, we emulated the two-area system and IEEE 39-bus system with various contingencies. The data and the program in VHDL language were downloaded from the host
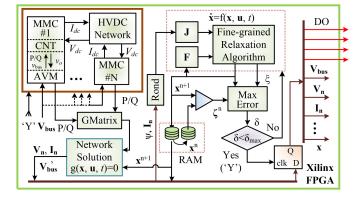
Fig. 4.   Integrated AC/DC grid top-level hardware design scheme and signal flow routes.

Fig. 5.   Top-level finite state machine for the coordination of hardware modules of the integrated AC/DC grid.

computer via the JTAG interface, which has the ability of in-circuit-debug, in-circuit-emulator, and in-system-program. The digital output of the FPGA board was transferred into analog data by the digital-and-analogic-converter (DAC) board through the FPGA Mezzanine Card (FMC) connector so that the waveforms can be displayed on the oscilloscope. However, in a power grid control center, the data from the real system can be delivered to the FPGA board running a virtual grid via Samtec FireFly connector, Quad Small Form-factor Pluggable (QSFP) interface which has dual cages with a maximum transmission speed of up to 4×28 Gbps, and the Ethernet interface, and vice visa for the output since all these three ports are bidirectional regarding data transmission. The QSFP interface is constructed with fiber optic material, which can significantly reduce the signal attenuation, and therefore, in the power grid control center, it is applied for data exchange with external devices, including other FPGAs. In the meantime, a significantly reduced data communication delay of the QSFP connector helps maintain FTRT simulation. It is also available for transferring data through Ethernet jack as a backup since the Ethernet connector can reach a maximum speed of 1000 Mbps. On the other hand, the FireFly connector is the latest on-board data communication interface with both copper and optical modules. Nowadays, the QSFP interface and FireFly connector have the same transmission speed of 28 Gbps per lane and similar features. However, the FireFly connector will be widely used in the future with the advantages such as small size and low power consumption. When an actual contingency occurs, the FTRT hardware platform in the control center can yield several solutions to mitigate the frequency rise and other damage. Therefore, the control center may have sufficient time to deal with the faults as well as make an optimal decision.

Fig. 4 shows a concise hardware architecture of the integrated AC/DC grid. The solution of the discretized form of the differential equation is conducted with parallelism due to the proposed FGRA, which, along with the nonlinear nature of the differential equation, requires iteration until the maximum error among all state variables and those caused by fine-grained relaxation algorithm is less than the tolerance $\delta_{\max}$. Meanwhile, the EMT simulation mainly involves 3 modules: the MMC including the AVM and its controller (CNT), and the HVDC network is conducted simultaneously. As the only type of signal that
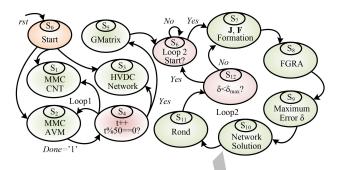
the dynamic simulation needs from the DC grid is the dynamic active power, which is converted into admittance according to the voltage of the bus the HVDC station connects to, the admittance matrix of the AC system can be formed in the module $GMatrix$. The iterative solution of (1) may yield the state variables multiple times in a single time-step, forcing the hardware module Network Solution to follow the same procedure. Once the dynamic simulation results converge, the AC bus voltages are fed back to the DC grid so that the EMT simulation can move forward to the next time-step. Any results produced during the co-simulation, denoted as DO in the figure, can be exported and displayed on the oscilloscope.

Noticing that the time-step required by EMT simulation should be much smaller than that of dynamic simulation in addition to a correct sequence that all the hardware modules need to follow, a top-level finite state machine (FSM) is required, as shown in Fig. 5. The co-simulation starts once the reset order is issued, and the EMT simulation of the DC grid starts in $Loop1$. A time-step of 10 ms used in the dynamic simulation means that the DC grid is computed 50 times more frequent than its AC counterpart. In $Loop2$, the discretized differential equation is first solved to obtain the state variables using the proposed FGRA. The calculation of the maximum error of the results is followed by solving the network equation, and the results are used to update the synchronous generators. The necessity of FGRA iteration in computing the overall loop is determined by the maximum error δ and its threshold $\delta_{\max}$: repetition of the loop is mandatory if the results are not sufficiently accurate; on the other hand, a convergence does not guarantee a new start of the dynamic simulation unless – as mentioned above – the DC grid has proceeded to another 50 ms. Table I gives the design specifics of major hardware modules, where the "MMCCNT," "MMVAVM," and "DCGrid" denote the functions in DC system. The "Gmatrix," "JMatrix," and "FVector" refer to the modules of calculating admittance matrix, Jacobian matrix, and the F vector in (7), respectively. The "Rond" function presents the function of updating of the Jacobian matrix elements. All the modules except for the "GMatrix" are inside the iteration loop. Since there is nearly no time-delay of values assignment in hardware simulation, the new state variables updating function is not shown in Table I. With the latencies above, it can calculate the accelerator factor theoretically, then validate in hardware emulation. The DC grid parts are fully parallelized with the largest

TABLE I
SPECIFICS OF MAJOR AC/DC GRID HARDWARE MODULES

Module	BRAM	DSP	FF	LUT	Latency
MMCCNT	0	54	5733	11085	85 T_{clk}
MMCAVM	16	208	8292	19277	90 T_{clk}
DCGrid	0	17	2209	2868	73 T_{clk}
GMatrix	12	1045	123388	126767	1313 T_{clk}
JMatrix	0	53	5045	4984	30 T_{clk}
FVector	0	87	8376	8219	32 T_{clk}
Maxerror	0	4	3874	4570	394 T_{clk}
ACNet	16	534	43928	57664	269 T_{clk}
Rond	16	402	27032	42750	98 T_{clk}
FGRA	0	8	1010	1596	35 T_{clk}
Gauss	0	4807	554584	925577	1464 T_{clk}
LU	$\geq$78	$\geq$480	$\geq$157849	$\geq$225383	>1805 T_{clk}
Case 1	28	3819	416284	535773	7462 T_{clk}
	0.6%	55.8%	17.6%	45.3%	–
Case 2	32	4127	560929	866576	7462 T_{clk}
	0.7%	60.3%	23.7%	73.3%	–
XCVU9P	4320	6840	2364480	1182240	–

latency of 90 T_{clk}, i.e., 90 clock cycles, under an FPGA clock frequency of 10ns, meaning with an EMT simulation time-step of 200 μs, the FTRT ratio is over 222 times. Meanwhile, in a TS time-step, the latencies inside the iteration can be calculated as $32 + 35 + 394 + 98 = 559 \ T_{clk}$, where the "FVector" and "JMatrix" can be parallelized, similarly, the "MaxError" and "ACNet" functions should be synchronized, therefore we choose the maximum latency between the parallel parts. Nevertheless, it is not the actual latency since the iteration is not taken into account. Take the hybrid two-area AC/DC system as an example, the maximum iteration is 11. Since the number of iterations in every time-step varies significantly, the FGRA function may need to calculate 11 times in every time-step on the FPGA, or calculate with less than 11 times and wait idly till an equivalent amount of time expires. With a maximum FGRA iteration of 11, the estimated overall latency of the dynamic simulation is $559 \times 11 + 1313 = 7462$ clock cycles, where the "GMatrix" with a latency of 1313 T_{clk} is only calculated outside of the iteration loop, meaning with a time-step of 10 ms, the FTRT ratio reaches over $\frac{10 \text{ ms}}{7462 \times 10 \text{ ns}} \approx 134$. Meanwhile, the EMT model can be solved in parallel with the TS model which is the AC grid, i.e., the DC grid will send data to the AC system in every 50 steps, considering that the DC part is 222 times faster than real-time which is faster than AC grid, the DC grid needs to wait the AC grid in every 50 EMT time-steps. So we can estimate that the hardware emulation is 134 times faster than real-time. By comparison, if the traditional matrix-based method is adopted, with a maximum iteration number of 5, the overall latency would be 11253 clock cycles – larger than the proposed FGRA method. In addition to Case 1, the HVDC grid is also integrated into two IEEE 39-bus systems for the study of a more practical scenario, given as Case 2 in Fig. 6. It shows that the chosen FPGA board has sufficient hardware resources for the final designs of both cases.

V. FTRT SIMULATION RESULTS AND VALIDATION

The two dynamic-EMT co-simulation cases are tested to showcase the predictive regulation of FTRT in stabilizing the power system following various contingencies, and the results
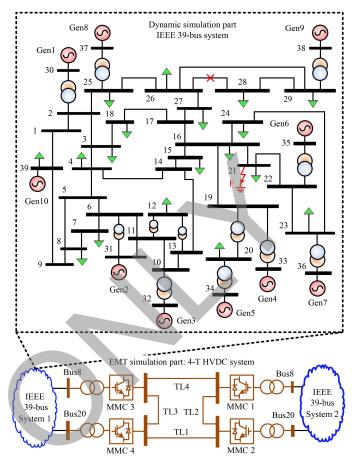

Fig. 6. Case 2: integrated large-scale AC/DC grid based on 2 IEEE 39-bus systems interconnected with a 4-terminal HVDC grid.

based on FPGA are validated by the off-line transient stability simulation tool TSAT in the DSATools suite.

A. Two-Area System

In the two-area system, the 2 MMCs connected to Bus 7 and 9 operate as inverter stations, while the remaining one as the rectifier station is linked to an infinite bus. At $t = 5$ s, a load of 183.5 MW and 383.5 MW are removed temporarily from Bus 7 and 9 respectively, causing instability to the AC system which cannot be restored even the loads are recovered 2 s later to its original capacity of 767 MW and 1567 MW, as can be seen from Fig. 7(a), the frequency keeps rising and eventually it is far beyond the maximum allowed 1% threshold, i.e., 60.6 Hz. On the contrary, the integration of HVDC system greatly improves the stability issue by doubling the rectifier's output power to 800 MW following the detection of the grid frequency exceeding the threshold at around 7 s, and it lasts till the frequency is restored to the standard 60 Hz at $t = 10$ s, as Fig. 7(b) shows. Meanwhile, when Bus 7 and 9 are unloaded, the output power of the 4 synchronous generators, as expected, decrease, accompanied by a severe rise of all AC bus voltages given in Fig. 7(c). The intervention of HVDC suppresses all the voltages, which are finally restored, and so are the output powers of the synchronous generators.

Fig. 7.   Predictive control based on FTRT co-simulation for power system stability analysis: (a) AC grid frequency, (b) output power of synchronous generators and MMCs, and (c) AC bus voltages.
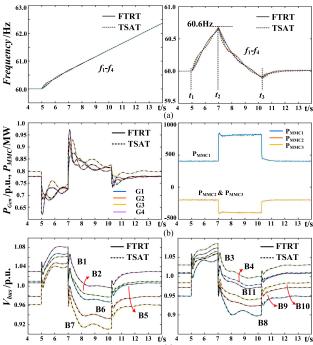

Fig. 8.   FTRT co-simulation for preview of generator behaviors under AC system ground fault: (a) Rotor angles, (b) voltages, and (c) frequencies.

B. Large-Scale AC/DC Grid

In Fig. 6, $MMC3$ and $MMC4$ operate as the rectifiers while the other two operate as inverters. At $t = 5$ s, a ground fault lasting 270 ms occurs at Bus 21 in $System$ 1. The imminent impacts are severe disturbances to the AC system, including the synchronous generators' rotor angle, the bus voltage, and the frequency, as shown in Fig. 8, e.g., the rotor angle of $G5$ surges to over $200°$ in less than 0.3 s, the voltage of the synchronous generator $G6$ plummet to below 0.5 p.u., and the frequencies rise beyond the 60.6 Hz threshold. An initial test by the dynamic-EMT co-simulation proved that the AC system cannot restore its frequency to below 60.6 Hz even when the fault is cleared, which is why the HVDC grid participates in stabilizing the AC power system by maintaining a continuous injection of an additional 200 MW and 100 MW from the two rectifiers respectively into the DC grid between $t = 5.2$ s and $t = 9$ s. Therefore, the FTRT simulation is able to help tackle power system stability issues by providing necessary solutions as well as quantifying the exact change to be made such as the amount of power to be injected in this case prior to action from the actual system.

The inter-area oscillation test is also conducted to further demonstrate the predictive regulation function of FTRT in stabilizing the power system, and the results are given in Fig. 9. At $t = 5$ s, the transmission line between Bus 26 and Bus 28 in the $System$ 1 is temporarily removed, so that the normal operation of the load on Bus 28 is mainly sustained by the 9th generator. At $t = 10$ s, the line is recovered while the one between Bus 28 and 29 is disconnected. It can be seen that the system starts to oscillate, e.g., rotor angles of the generators, and the

output powers of many of them, as given in Fig. 9(a)–(c). At $t = 15$ s, the connection between Bus 28 and 29 is restored, and the two rectifiers begins to deliver more power from the AC system subjected to inter-area oscillation, i.e., an additional extraction of 100 MW and 50 MW from Bus 8 and Bus 20, respectively. The benefit of FTRT is thoroughly demonstrated by the fact that the all artificial interventions, including that by the HVDC system, can stop at $t = 17.5$ s even when the system is still undergoing severe oscillations since the power system is able to recover gradually by itself at around $t = 25$ s, as shown in Fig. 9(d)–(f), and the actual system action can follow suit since this scenario has already been simulated in advance and proven to be effective. It should be pointed out that representing the HVDC converter by the time-varying P+jQ load plays a significant role in stabilizing the AC grid frequency, as shown in Fig. 7(b) and Fig. 9(d); on the contrary, the AC grid will not stabilize if the equivalent load is kept constant.

With its results proven to be correct, the FTRT ratio that the hardware emulation can achieve in both cases is validated by the oscilloscope waveforms. The 4 synchronous generators' voltages and their relative angles to generator $G4$ are given in Fig. 10(a), and the former waveforms show an identical trend to that of AC buses in Case 1. Similarly, the generator waveforms under inter-area oscillation of Case 2 are shown in Fig. 10(b). It should be particularly pointed out that both of the waveforms in Fig. 10(a) have the time interval in real-time of 13.4 s. Meanwhile, 1 division in the oscilloscope presents 10 ms which refers to 100 ms on the x-axis. The discrepancy between the oscilloscope scan time and the duration that these waveforms actually denote indicates that the proposed FTRT
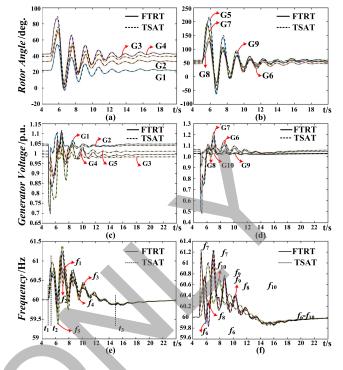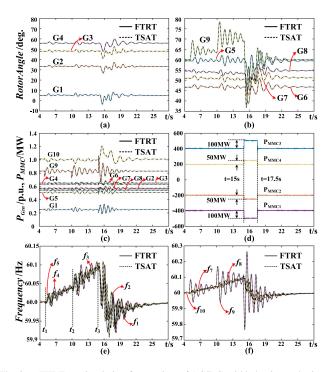
Fig. 9. FTRT co-simulation for preview of AC/DC grid behavior under inter-area oscillation: (a) Generator rotor angles, (b) output power of generators and MMCs, and (c) generator frequencies.
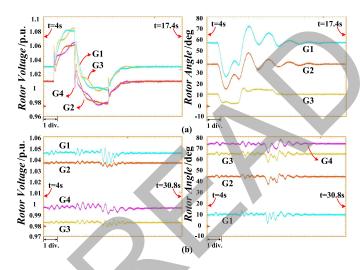

Fig. 10. FTRT co-simulation results displayed in the oscilloscope from: (a) Case 1 (x-axis: 10 ms/div.) and (b) Case 2 (x-axis: 20 ms/div.).

co-simulation is approximately 134 times faster than real-time, meaning it leaves a sufficient margin for the actual power system to react and adopt the strategy tested in advance by the hardware emulation on FPGA.
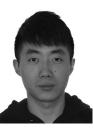
VI. CONCLUSION

This paper proposed a fine-grained relaxation algorithm for faster-than-real-time dynamic simulation of integrated AC/DC grids. The proposed algorithm is iterative and is completely devoid of matrix operations; as such it is perfectly suited for

mapping to the massively paralleled and pipelined hardware architecture of the FPGA. The emulated dynamic network model achieved a factor of 134 faster than real-time execution. The time-domain results from the case studies of integrated AC/DC methods demonstrate, in comparison with a commercial transient stability simulation tool, that the proposed algorithm is numerically stable and highly accurate in computing system states. Furthermore, the closed-loop HVDC grid control demonstrated the efficiency of the FTRT in predicting future system dynamic performance and taking effective control action to mitigate unforeseen contingencies with the potential to adversely impact grid stability.

While the emulation of the proposed FTRT dynamic studies was carried out on a single Xilinx Virtex UltraScale+ XCVU9P FPGA, the proposed fine-grained relaxation algorithm is fully scalable for execution on multiple FPGAs interfaced with high speed data communication links. Since the system components undergo fully decoupled solution, the proposed algorithm is also amenable to multi-rate or variable time-step FTRT simulations in the future. To assess the impact on individual system components, selective inclusion of defaulted EMT models of specific equipment is achieved resulting in a hybrid dynamic-EMT FTRT simulation.

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