Grant Agreement No: 101004761

AIDAinnova

Advancement and Innovation for Detectors at Accelerators

Horizon 2020 Research Infrastructures project AIDAINNOVA

MILESTONE REPORT

Common read-out boards designed

MILESTONE: MS11

Document identifier:	AIDAinnova-MS11.docx
Due date of milestone:	End of Month 23 (February 2023)
Report release date:	11/02/2023
Work package:	WP3: [Test Beam and DAQ Infrastructure]
Lead beneficiary:	[CERN]
Document status:	Final

Abstract:

The modular DAQ development projects Caribou (for silicon detectors) and SRS-VMM3 (for gas detectors) provide common open-source platforms with reusable hardware, firmware and software. This document reports on the design of the two readout boards, which constitutes MS11 in month 23.

For more information on AIDAinnova, its partners and contributors please see http://aidainnova.web.cern.ch/

The Advancement and Innovation for Detectors at Accelerators (AIDAinnova) project has received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement no. 101004761. AIDAinnova began in April 2021 and will run for 4 years.

Delivery Slip

	Name	Partner	Date
Authored by	D. Dannheim E. Oliveri E. Buschmann L. Scharenberg H. Muller	CERN	11/02/2023
Edited by	D. Dannheim E. Oliveri	CERN	
Reviewed by	D. Dannheim [Task coordinator] M. Stanitzki [WP coordinator] M. Wing [WP coordinator]	CERN DESY UCL	20/02/2023
Approved by	Daniela Bortoletto [Deputy Scientific coordinator] Steering Committee		28/02/2023

TABLE OF CONTENTS

Executive summary

Caribou is a modular open-source DAQ system developed and used within AIDAinnova and other collaborative frameworks (CERN EP R&D, RD50, Tangerine) for laboratory and high-rate beam tests and easy integration of new silicon-pixel detector prototypes. It uses common hardware, firmware and software components shared across different projects, reducing the development effort and cost for such readout systems significantly. The common BNL Carboard readout hardware provides resources such as power supplies, reference voltages and currents, and interfaces to various detector-specific chip boards housing the detectors under test. The Carboard revision 1.4 has been designed and the design has been validated with prototype boards.

SRS-VMM3 is a general-purpose modular laboratory, test-beam and middle size experiment DAQ system for Micro-Pattern Gaseous Detectors (MPGDs) based on the RD51 Scalable Readout System (SRS) and the BNL/ATLAS front-end ASIC VMM3a. The front-end ASIC VMM3a is mounted on a readout PCB carrier that, using optional adapter cards, can be plugged into any detector. The chip provides signal amplitude and timing, is self-triggering, allows continuous readout, and has a high throughput in acquisition rate (MHz/channels). Several internal amplifier parameters, such as gain and peaking time are adjustable, favouring integration with different detector technologies. A full-system prototype has been designed and the design has been validated with prototype boards in test beam campaigns at the SPS.

1. INTRODUCTION

Within AIDAinnova WP 3, two modular open-source DAQ developments are pursued, targeting laboratory and test-beam measurements: the Caribou DAQ [1-3] is designed for silicon detectors developed in WP 5 and 6, while the SRS-VMM3 DAQ [7-9] serves the gas-detector developments in WP 7. The use of common hardware, firmware and software components shared across different projects significantly reduces the DAQ development effort. This report focuses on the design of the reusable common readout boards, which constitute the core hardware components of the projects. The completion of the design has been a prerequisite for the production and dissemination of the boards to the participating institutes.

2. DESIGN OF COMMON READOUT BOARDS FOR CARIBOU

2.1. THE CARIBOU HARDWARE ARCHITECTURE

Figure 1 shows a schematic representation of the hardware components of the Caribou system. At the detector side of the readout chain, a custom-designed chip board implements the routing from a specific detector under test to the Carboard readout board. The Carboard provides resources such as power supplies, reference voltages and currents, and detector interfaces. The core of the Caribou system is a Xilinx Zynq System-on-Chip (SoC) device hosted on a ZC706 evaluation board, which is interfaced with the Carboard via an FMC interface. The SoC combines a dual-core ARM Cortex-A9 CPU and a Kintex-7 Field Programmable Gate Array (FPGA) fabric connected through a silicon interposer.

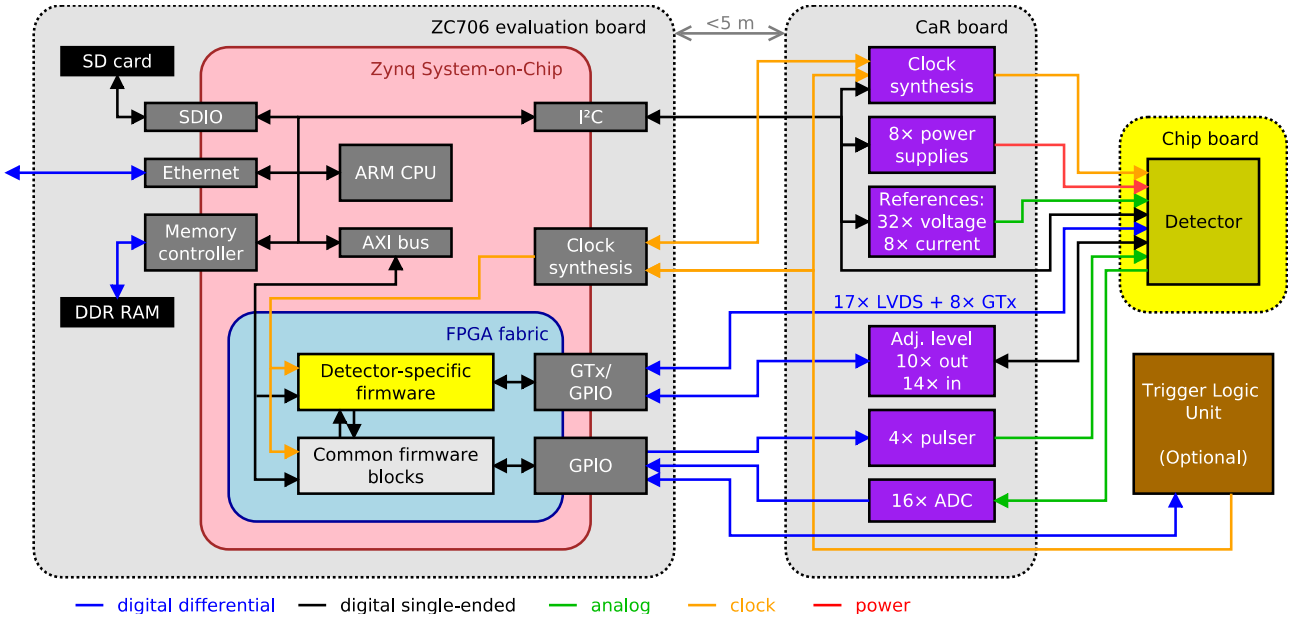

Figure 1: Schematic representation of the Caribou hardware architecture, consisting of a ZC706 evaluation board, a universal Carboard and an application-specific chip board. From [4].

2.2. CARBOARD REVISION 1.4 DESIGN

The readout board (Carboard rev. 1.4) provides the hardware environment for the various target silicon detectors. The resources contained on the board and their main design parameters are listed in Tab. 1. Programmable power supplies with monitoring, programmable voltage and current references, analogue-to-digital converters (ADCs), an I2C interface bus, as well as several general-purpose communication links including high-speed full-duplex serial links up to 12.5 Gbps (GTx), differential links for up to 1.2 Gbps (LVDS) and single-ended general-purpose inputs and outputs (GPIO) with adjustable voltage level are included. Furthermore, the Carboard is equipped with a clock generator which can be used to generate stable clock signals for use in both the detector and the firmware blocks. The Carboard can receive an external clock and triggers from a trigger logic unit (TLU) to synchronise with external devices and other readout systems. The board is connected to the application-specific chip board via a 320 pin SEARAY connector and is therefore re-usable for different devices and setups. The ZC706 evaluation board is connected to the Carboard via an FMC interface.

Resource	# channels	parameters
Adjustable power supplies with monitoring and over-current protection	8	0.8-3.6 V, 3 A
Adjustable voltage references	32	0-4 V
Adjustable current references	8	0-1 mA
Slow (50 kSPS) 12-bit ADC	8	0-4 V
Fast (65 MSPS) 14-bit ADC	16	0-1 V
Programmable injection pulsers	4	
Full-duplex high-speed GTx links	8	12.5 Gbps

Bidirectional LVDS links	17	1.2 Gbps
Output / input links, adjustable level	10/14	0.8-3.6 V
Programmable clock generator	1	
Inputs for high voltage, clock reference, trigger	1	
FMC interface to ZC706 FPGA board	1	
320-pin SEARY connector to detector	1	

Table 1: Resources on the Carboard rev. 1.4

New features contained in rev. 1.4 are an over-current protection for the power supplies and the possibility to select the chip-board type in software.

The design of the Carboard rev. 1.4 has been completed and all design files are available in an open-source repository [5]. Figure 2 shows the drawing of the top side of the Carboard rev. 1.4 PCB.

A batch of 20 prototype rev. 1.4 boards has been produced (Fig. 3) and disseminated within the participating groups. Measurements with various detector types have validated the Carboard design and confirmed that the performance targets are reached [6].

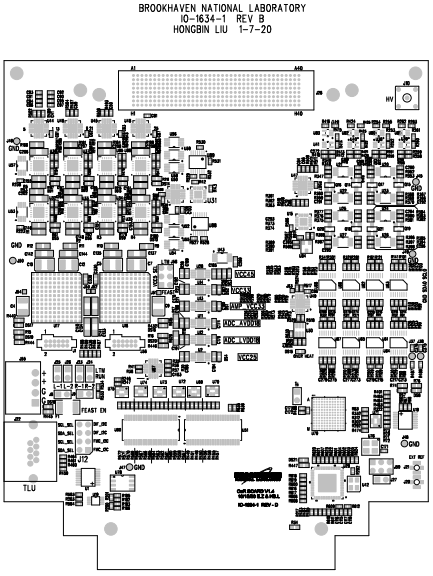

Figure 2: Carboard rev. 1.4 PCB top drawing

Figure 3: Carboard rev.1.4 prototype board

3. DESIGN OF COMMON READOUT BOARDS FOR VMM3A

A prototype system of a DAQ based on the RD51 SRS (Scalable Readout System) and VMM3a (BNL/ATLAS NSW ASICs) has been delivered [10]. Within AIDAinnova task 3.5.2, developments specific to the use in test beam for tracking and timing telescopes, and DUT studies are being performed. Distributed systems and compatibility with different detector technologies, synchronization, high throughput, flexible triggering schemes, data integrity and common DAQ, have been addressed towards a final design suitable for operation in test beams. The results reported here have been achieved in the context of the RD51 collaboration with essential contributions from RD51

(H. Muller), the ESS-NMX team (D. Pfeiffer), the CERN Gas Detector Development (GDD) team (L. Scharenberg), and the CERN spin-off SRS-Technology (A.Rusu).

3.1. THE SRS/VMM3A DAQ

An example of a typical SRS setup is shown in Fig. 4 and Fig. 5. Synchronization between different FEC cards is obtained via the CTF (clock and trigger fanout card). The system is intrinsically scalable to a large number of channels.

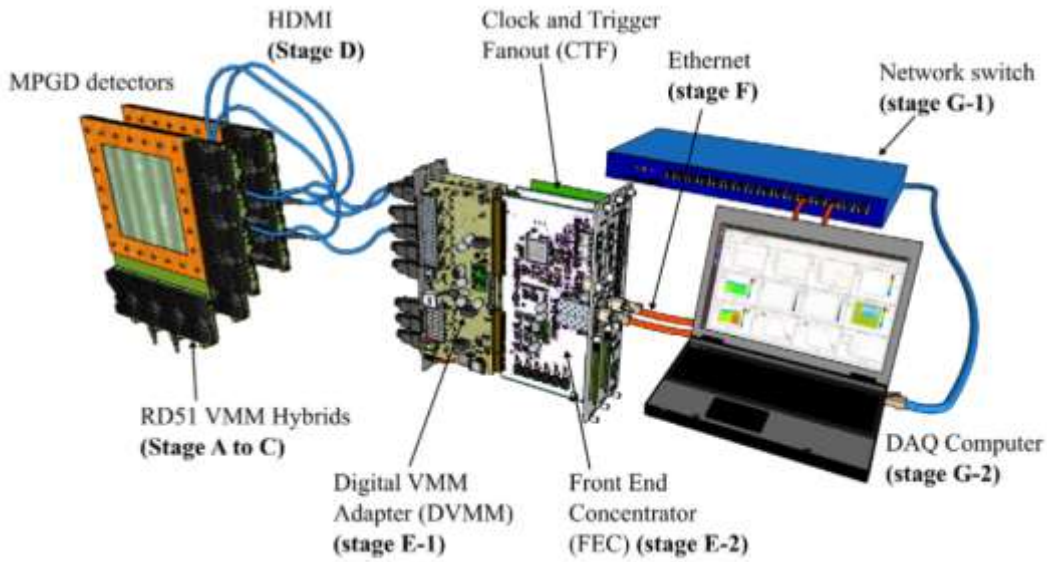

Figure 4: The RD51 VMM hybrid contains two VMM3a ASICs (stage A) that are connected (stage B) to a Spartan-6 FPGA (stage C). Each hybrid is connected via HDMI (stage D) to the combination of DVMM card and FEC card (stage E) that here is shown outside the minicrate 2k. The FEC is then connected via ethernet (stage F) to the DAQ computer (stage G).

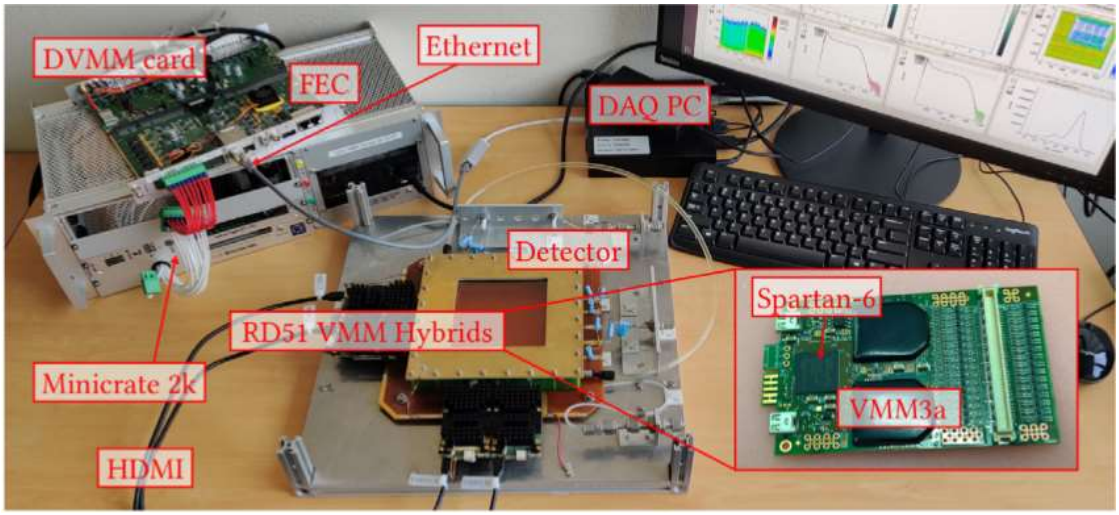

Figure 5: The RD51 VMM hybrid contains two VMM3a ASICs (stage A) that are connected (stage B) to a Spartan-6 FPGA (stage C). Each hybrid is connected via HDMI (stage D) to the combination of DVMM card and FEC card (stage

E) that is shown here outside the minicrate 2k. The FEC is then connected via ethernet (stage F) to the DAQ computer (stage G).

3.2. RELEASED VERSION FOR TEST BEAM

This section reports on the system configuration that has been designed and tested. The system satisfies the prerequisite for the production and dissemination of the boards in the community.

Hardware

Hardware related documentation is updated and publicly accessible at [11].

The RD51 VMM3a hybrid

The core element for the SRS/VMM3a system is the chip carrier. Figure 6 shows the hybrid version 4.0 previously developed and integrated in the current system. This hybrid has been developed with the essential contribution of the SRS-Technology spin-off, which takes care of the hybrid production.

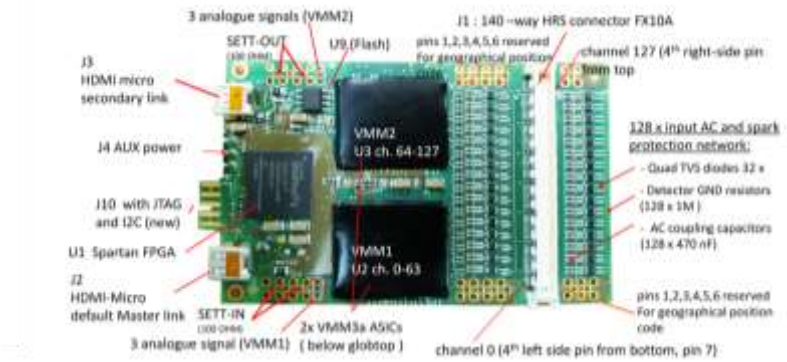

Figure 6: 5 cm × 8 cm Printed Circuit Board (PCB) equipped with two VMM3a ASICs, providing 128 charge input channels. A 144 pin Hirose connector on the hybrid connects to the readout of the detector.

A new revision (Rev. 5, 2022+) has been developed and tested in 2021. The most relevant changes are the replacement of the Spartan-6 FPGA with Spartan7, I2C bus extended to the detector connector (HRS), geographical identification of the chip, new Flash memory and ID chip/Eprom. All new productions will use Rev. 5, but backward compatibility with the previous version will be guaranteed.

The SRS system

The core of the SRS system is shown in Fig. 7. It consists of the Front End Concentrator (FEC) card, the Digital VMM Card Adapter (DVMM) and the Clock and Trigger Fan-out (CTF) card. The cards are hosted and powered via the SRS 2K minicrate. Each FEC card can read up to 8 RD51 VMM3a hybrids (128 channels each). A CTF can synchronize the clocks of up to 8 FEC Cards.

Figure 7: The SRS DAQ system to operate the VMM3a FE ASIC

During the design and development of the system for test-beam operation, the issue of powering many FE ASICs per FEC and the need to have delocalized systems (long HDMI cables between the DVMM card and the hybrids) called for an optimization of the power and grounding scheme. A power box PMX (Fig. 8 and 9) to be locally installed on the detector has been developed to power up to 8 hybrids. Further, in order to allow for stable operation for long HDMI cables, a new PMX-2 version with extended functionalities and remote control is under test. Both versions will be accessible to the community.

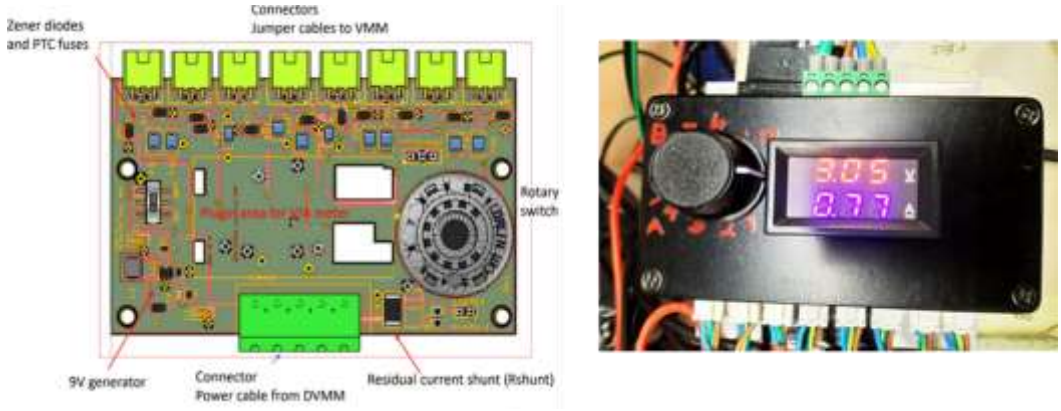

Figure 8 Power box. Each power box can supply power to 8 RD51 VMM Hybrids.

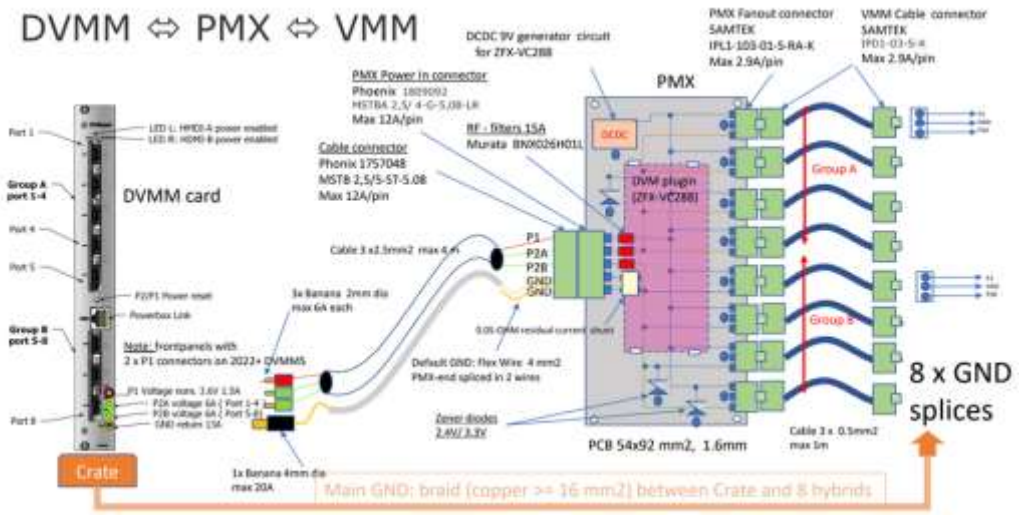

Figure 9: Interconnections between the DVM card, the PMX power box and the VMM3a hybrids.

The system documentation [12] and user manual of the system [13] are available and continuously updated.

4. REFERENCES

[1] H. Liu et al., Development of a modular test system for the silicon sensor R&D of the ATLAS Upgrade, JINST 12 (2017) P01008, DOI: 10.1088/1748-0221/12/01/P01008.

[2] A. Fiergolski, A Multi-chip Data Acquisition System Based on a Heterogeneous System-on-Chip Platform, Proceedings of TIPP 2017, Beijing, China, 2017, p. 303,

DOI: 10.1007/978-981-13-1313-4_57.

[3] T. Vanat, Caribou–A versatile data acquisition system, PoS TWEPP2019 (2020) 100, https://doi:10.22323/1.370.0100.

[4] Detector Technologies for CLIC, edited by D. Dannheim, K. Krüger, A. Levy, A. Nürnberg, E. Sicking, CERN–2019–001 (CERN, Geneva, 2019), http://dx.doi.org/10.23731/CYRM-2019-001.

[5] Caribou project git repository, [Online; Last accessed 11.02.2023], URL: https://gitlab.cern.ch/Caribou.

[6] E. Buschmann, Status and recent extensions of the Caribou DAQ system for picosecond timing with an FPGA TDC, JINST 18 (2022) C02005, DOI: 10.1088/1748-0221/18/02/C02005.

[7] S. Martoiu, et al., Development of the scalable readout system for micro-pattern gas detectors and other applications, J. Instrum. 8 (2013) C03015, http://dx.doi.org/10.1088/1748-0221/8/03/c03015.

[8] G. Iakovidis, VMM3a, an ASIC for tracking detectors, J. Phys. Conf. Ser. 1498

(2020) 012051, http://dx.doi.org/10.1088/1742-6596/1498/1/012051.

[9] M. Lupberger, et al., Implementation of the VMM ASIC in the scalable readout system, Nucl. Instrum. Methods Phys. Res. A 903 (2018) 91–98, http://dx.doi.org/10.1016/j.nima.2018.06.046.

[10] http://cds.cern.ch/record/2316257/files/AIDA-2020-MS83.pdf

[11] SRS Hardware Manuals and links,

https://drive.google.com/drive/folders/1h5KLMAa7-bxbPoisnip5Adb4mYc2YMdq?usp=share_link

[12] https://vmm-srs.docs.cern.ch/

[13] https://vmm-srs.docs.cern.ch/operating/#operating-the-system

ANNEX: GLOSSARY

Acronym	Definition
ASIC	Application Specific Integrated Circuit
DAQ	Data Acquisition System
FE	Front End
HDMI	High-Definition Multimedia Interface
MPGD	Micro-Pattern Gaseous Detector
PCB	Printed Circuit Board
SoC	System-on-Chip