Published in final edited form as:
IEEE J Solid-State Circuits. 2021 August ; 56(8): 2466–2475. doi:10.1109/JSSC.2021.3066043.

Extracellular Recording of Entire Neural Networks Using a Dual-Mode Microelectrode Array With 19584 Electrodes and High SNR

Xinyue Yuan,
Department of Biosystems Science and Engineering, ETH Zurich, 4058 Basel, Switzerland. She is now with MaxWell Biosystems AG, 8047 Zurich, Switzerland

Andreas Hierlemann [Member, IEEE],
Department of Biosystems Science and Engineering, ETH Zurich, 4058 Basel, Switzerland

Urs Frey [Member, IEEE]
Urs Frey was with the Department of Biosystems Science and Engineering, ETH Zurich, 4058 Basel, Switzerland. He is now with MaxWell Biosystems AG, 8047 Zurich, Switzerland

Xinyue Yuan: xinyue.yuan@bsse.ethz.ch; Andreas Hierlemann: andreas.hierlemann@bsse.ethz.ch; Urs Frey: urs.frey@mxwbio.com

Abstract

Electrophysiological research on neural networks and their activity focuses on the recording and analysis of large data sets that include information of thousands of neurons. CMOS microelectrode arrays (MEAs) feature thousands of electrodes at a spatial resolution on the scale of single cells and are, therefore, ideal tools to support neural-network research. Moreover, they offer high spatio-temporal resolution and signal to-noise ratio (SNR) to capture all features and subcellular resolution details of neuronal signaling. Here, we present a dual-mode (DM) MEA, which enables simultaneous: 1) full-frame readout from all electrodes and 2) high-SNR readout from an arbitrarily selectable subset of electrodes. The DM-MEA includes 19584 electrodes, 19584 full-frame recording channels with noise levels of 10.4 μV_{rms} in the action potential (AP) frequency band (300 Hz–5 kHz), 246 low-noise recording channels with noise levels of 3.0 μV_{rms} in the AP band and eight stimulation units. The capacity to simultaneously perform full-frame and high-SNR recordings endows the presented DM-MEA with great flexibility for various applications in neuroscience and pharmacology.

Index Terms

Extracellular recording; full-frame readout; microelectrode array (MEA); signal-to-noise ratio (SNR); switch-matrix (SM)

Correspondence to: Xinyue Yuan, xinyue.yuan@bsse.ethz.ch.

This article was approved by Associate Editor Nick van Helleputte. This work was supported in part by the European Research Council Advanced Grant 694829 “neuroXscales” and the Corresponding Proof-of-Concept Grant 875609 “HD-Neu-Screen,” in part by the Swiss National Science Foundation under Contract 205320_188910/1, and in part by the European Union’s Horizon 2020 Research and Innovation Programme under Grant 863245 (NEUREKA).

Conflict Of Interest U.F. is a co-founder of MaxWell Biosystems AG, Zürich, Switzerland.

I Introduction

THERE is an increasing interest in studying cultured neural networks as a method toward understanding how the brain works and as a tool in drug discovery to test how pharmaceutical compounds act on the brain. In addition, recent advances in induced-pluripotent-stem-cell (iPSC) technology provide a promising approach to study neurological disorders with human *in vitro* systems [1]–[3]. To study the network activity of neurons, researchers are using various methods, including imaging techniques, such as calcium imaging [4], intracellular recording methods, such as patch clamp [5], and extracellular recording techniques, such as electrical imaging [6]. Through the recording of optical or electrical signals generated by neurons, such as action potentials (APs) and local-field potentials (LFPs), single-neuron behavior and neuronal signaling in neuronal networks can be studied.

Among the applied methods, extracellular recording of electrical signals using microelectrode arrays (MEAs) is one of the most efficient ways of acquiring neural signals from a large number of neurons in terms of number of recording sites, temporal resolution, spatial resolution, and signal-to-noise ratio (SNR) [6], [7]. Compared to standard electrophysiological methods, such as calcium imaging and patch clamp, MEA systems offer a better temporal resolution and more flexibility for the study of large-scale neural networks with thousands of neurons. By using CMOS technology, the electrodes can be designed to achieve single-cell or even subcellular spatial resolution, and the entire electronic system including amplification and filtering circuitry can be implemented on the same chip. Recent trends for the development of CMOS-based MEA systems point toward larger arrays with more electrodes, higher spatial resolution, higher SNR, and readouts with multiple modalities for different applications. The number of electrodes reported for CMOS-based MEA systems can be larger than 60 k [8]–[10], and the electrode diameter can be as small as a few micrometers [11]. Moreover, a low noise level below 5 μV_{rms} has been achieved [9], [12]–[15], thereby enabling reliable spike detection of small extracellular APs or axonal signals. In addition, multi-modality MEA systems have been developed [9], [16] to not only record electrical signals but also measure electrochemical signals of neurotransmitters as well as electrode impedance. In addition, an intracellular recording was proven to be possible [16], [17] with *in vitro* MEAs using an electroporation method with current or voltage stimulation techniques. Access to intracellular signals relaxes the noise requirements for the MEA system and gives access to sub-threshold events, such as post-synaptic potentials.

Despite the recent rapid advancements in developing MEA systems, the trade-off between SNR and the number of readout channels that can be realized on chip remains a limiting factor for MEA designs. Owing to this tradeoff, two major circuit strategies have been used. The first strategy is to implement an as large as possible array but with a limited number of readout channels outside the array to record from a subset of electrodes. A switch matrix (SM) is then commonly used to route the electrodes in the array flexibly to the limited number of readout channels outside the array [9], [12], [14] [see Fig. 1(a)]. With this SM structure, the readout circuits can be designed to achieve noise levels below 5 μV_{rms}, which, in turn, yields a high SNR. The other strategy is to implement as many readout channels as

possible and limit the overall number of electrodes so that all electrodes can be read out simultaneously. For this approach, a structure called “active pixel sensor” (APS) has been prevailingly used [10], [16], [18], [19] with readout circuits inside each pixel [see Fig. 1(b)]. This structure can achieve high coverage of recording electrodes, however, at the expenses of a lower SNR owing to the limited area inside each pixel for implementing readout and routing circuitry. As the study of neural networks of thousands of neurons requires both high SNR and high channel count, we developed a dual-mode (DM) MEA that combines SM and APS modes in a single chip [20].

The DM-MEA concept is an attempt to optimize as many features of MEA designs as possible, including spatial resolution, SNR, and consumption of power of such systems. Compared to single-mode devices, the design challenges of DM-MEA do not only include to meet the specifications of each recording mode, but also to ensure that both modes work reliably and efficiently together in recording simultaneously from the same electrodes. As both readout circuits compete for silicon area within the pixel, an only marginal increase of the performance of one of the readout modes is a challenging task. Despite the design challenges, the performance of both, the APS and SM readout circuitry of the DM-MEA turned out to be comparable to those of state of-the-art single-mode devices [6], [9], [12], [14], [21]–[24], or even better in comparison to other APS devices [21]– [24] that feature noise levels around 20 μV. In addition, the new combination enables a broader range of applications. For example, the DM-MEA not only combines the advantages of APS full-frame readouts and high-SNR recordings in SM mode in one device, but also offers the possibility of detecting small signals in the SM mode and using those as trigger signals for averaging of recordings in the APS mode [25]. Through this feature, the system is capable of recording small-amplitude signals, such as electrical signals of human iPSC-derived neurons or propagating axonal APs (<50 μV), over large active areas at high throughput, which is hardly possible using any of the SM-only or APS-only devices. Therefore, the DM-MEA is, e.g., particularly useful for applications involving human iPSC-derived neurons, where it outperforms single-mode devices. In addition, it is also much more versatile for a broad range of applications, due to the fact that it offers the advantages of both modes in a single device.

In [25] we demonstrated the application of this chip for studying neuronal dynamics at subcellular, single-cell and network levels. This article complements [26], in that it reports the design of the CMOS IC in much more detail, including detailed description of the circuits and electrical characterization results. This article is organized as follows. Section II describes the implementation of the DM-MEA system, Section III details the fabrication of the chip and the measurement setup, Section IV presents the experimental results, and Section V concludes this article.

II System Description

The DM-MEA system consists of an array of 19 584 electrodes, 19 584 APS readout channels, 246 SM readout channels for low-noise recording, and eight stimulation buffers for voltage or current stimulation (see Fig. 2). With multiple functions combined in a single chip, the DM-MEA has been designed for a wide range of applications.

A Microelectrode Array

The DM-MEA consists of 192 × 108 pixels in a hexagonal arrangement [12] with a pixel size of 16.85 × 18.24 μm^2, which yields 19 584 electrodes at a pixel pitch of 18.0 μm and an electrode density of 3050 mm^{-2}. Within the limited pixel area, several blocks were implemented, including the routing scheme for APS and SM readouts, SRAM cells for SM configuration, and pixel amplifiers for the APS readout (see Fig. 2). To avoid crosstalk between different signals, additional shielding layers were implemented to separate analog and digital signals.

The addressing and routing of the array for APS and SM readout were implemented separately. For the APS readout, the whole array was divided into two halves (top and bottom), and the scanning rate for full-frame recording was 11.6 kframes/s. The APS row-selection signal was generated by the row decoder located outside the array. Different options can be configured for scanning through the array. In addition to scanning the full array, one can define scanning parameters, such as starting and ending rows, scanning steps, and scanning directions. By setting these options, the APS readout can be configured to scan only a defined area of interest and to perform oversampling. The SM configuration was stored in an SRAM integrated into the array and controlled by the bit-line (BL) registers and a word-line (WL) decoder. The 1-bit 6T SRAM cells, integrated in each pixel, were used to control the switches in the pixel for routing within the array. Routing wires and switches were arranged in the same way as in the previously reported SM devices [12]. The stimulation buffers were connected through the SM routing. Additionally, any electrode in the array can be configured to connect to external stimulation sources.

B APS Readout Circuits

For the APS readout, the array was divided into two halves, each with 54 rows. There are 24 column readout banks per half, with one bank serving eight columns. To carry out full-frame recording of the entire array, the APS first-stage amplifier has been implemented inside each pixel. Owing to the limited area inside each pixel, we designed the pixel amplifier with two stages. The first stage is an inverter-based amplifier, whereas the second stage is a buffer to drive the output signal [see Fig. 3(a)]. An input MIM capacitor (350 fF) was inserted between the electrode and the amplifier for ac coupling. The first-stage amplifier operates at 0.8 V, and the inverter-based structure was chosen owing to its simple structure and high ac gain. A feedback transmission-gate-based MOS resistor is connected between the input and output of the first-stage amplifier to implement a high-pass filter (HPF). The resistance could be tuned by varying the external reference V_{hpf}, and the high-pass corner could be set as low as 0.1 Hz. After the first stage, an MOS resistor (tunable V_{lpf})was connected. It formed a low-pass filter (LPF) with a MOS capacitor (450 fF capacitance) to prevent aliasing noise. The low-pass corner could be tuned from 900 Hz to 4.9 kHz. The second stage of the pixel amplifier was a common-source amplifier acting as a buffer to drive the signal along the long routing path. This amplifier was designed to be turned on only when a certain column was selected to reduce the power consumption of the system.

After the pixel amplifier, the signal was transmitted outside the array, first buffered by a two-stage operational amplifier (A2) with Miller compensation, and then further amplified by a

sample-and-hold (S/H) amplifier (A3) that employed an auto-zeroing technique to reduce the common-mode noise. The single-ended signal was converted to a differential signal for further processing [see Fig. 3(b)]. Non-overlapping clock signals (S1,S2) were generated for S/H operation. The S/H amplifier had a programmable gain of 6–18 dB with a sampling capacitor C_s of 635 fF. Afterward, the signal was multiplexed by an 8-to-1 multiplexer and digitized by a 10-bit SAR ADC [see Fig. 3(c)]. A4 was used to drive the signals for the ADC without amplification and had a similar structure as A2. The ADC samples at a rate of 5 MSamples/s, with a time-interleaving structure comprising two capacitor arrays with a split-array structure (C_0 to C_9) to interleave sampling (φ_1) and converting (φ_0) periods. This allowed for a longer sampling time, thus relieving the design requirements for the ADC driver (A4) and reducing power consumption. The digital output of the ADC was multiplexed to reduce the number of outputs off chip.

The timing of the APS readout was controlled by a central control unit shown in Fig. 3, which generated the timing signals for the ADC, column selection (EN), S/H amplifier (SH), and multiplexer (MUX addr). The controller could be configured with different timing configurations for different testing purposes, such as oversampling of a sparser electrode grid (e.g., skipping every other column or sampling only every eighth column).

C SM Readout Circuit and Stimulation Unit

For the SM readout, we used the same circuitry as published in [9], with four amplification stages, 4.76-pF input capacitor and a 10-bit SAR ADC for digitization [see Fig. 4(a)]. There are 256 SM channels, 246 of which could be routed to the electrode array, while the ten additional channels could be used for oversampling and recording of external signals. The routing inside the array was controlled by the SRAM cells integrated in each pixel. Every readout channel could achieve a maximum gain of 76.4 dB, and the high-pass corner could be tuned from below 1 Hz to up to 80 Hz to allow for measurements of both, APs and LFPs. The pseudo-resistors for the LPF and HPF are shown in Fig. 4(b). A current-biased transmission-gate-based structure was used to achieve large resistance with little variation [9]. In addition, the SM channels could be connected to a temperature sensor to read out the on-chip temperature.

The stimulation buffer circuitry was similar to that reported in [9] [see Fig. 4(c)], with each buffer connected to one 10-bit DAC_0 as the input, whereas the output was connected through the SM routing to different electrodes. DAC_1 and DAC_2 were shared among four buffers to limit the output voltage. The stimulation unit could be configured for either voltage-controlled or current-controlled stimulation. The voltage stimulation range was from -250 to 250 mV, and the current stimulation range extended from -5 to 5μA.

III System Integration

A Chip Fabrication and Post-Processing

The DM-MEA was fabricated in 0.18-μm CMOS technology [see Fig. 5(a)], with a chip size of 6.0 × 9.0 mm^2 and an active array area of 1.8 × 3.5 mm^2. After CMOS fabrication, the electrode array was post-processed to make it compatible with bio-applications. For long-

term stability, platinum (Pt) was deposited as electrode material. A passivation layer was deposited to insulate the electronics from the biological preparation [12]. The final electrode size was 8.6 × 10.2 μm^2. Electrode sizes have to be selected in view of the specific preparation and electrical signal characteristics that are targeted [27]. Here, we used a relatively large electrode size to serve a broad range of applications and to have a comparably low signal attenuation and noise. Furthermore, Pt-black was electrochemically deposited on the electrodes to reduce their impedance [27].

B Measurement Setup

Fig. 5(b)shows the packaged chip for experiments with only the active array area exposed. We used a custom PCB to generate power supplies, references, and external clock signals, with 50 MHz for the APS readout and 25 MHz for the SM readout. The setup was controlled by an external data-acquisition (DAQ) card connected to a PC with a custom-made LabVIEW interface. The control signal was generated by the interface and sent to the on-chip serial peripheral interface (SPI) to control the operation of the chip. The digital outputs were connected to another high-speed DAQ card for DAQ. For full-frame recording, the data rate was 300 MB/s.

IV Experimental Results

A Electrical Characterization

1) Gain and Noise Measurement—After the chip was fabricated and post-processed, we characterized the electrical properties of the system (see Fig. 6). The results are displayed for all readouts using 19 584 APS channels and 246 SM channels. By applying an 800 μVpp sinusoidal input and sweeping its frequency from 0.1 Hz to 10 kHz on all electrodes (the connection of the electrodes was actuated by setting the SM switches inside the pixel), we measured the transfer function for APS readout and SM readout, including amplifiers, multiplexers, and ADCs. Typical gain settings are shown in Fig. 6, and all gain settings were tested and within expectations. For the APS readout, all measurement data were acquired in full-frame mode. The measured mid-band gain was 38.9 dB for the readout chain, while the measured gain of the pixel amplifier was 30.9 dB. There was a 1.3% standard deviation in the mid-band gain caused by the structure of the first-stage amplifier. Given that the gain of the first stage was set by an open-loop inverter, which was dependent on the W/L ratio of nMOS and pMOS transistors, small fabrication variations led to a large mismatch of the gain between different channels. The low-pass corner, calculated from the averaged transfer function of all the APS channels, was 3.3 kHz, and by adjusting the resistance of the voltage-controlled MOS resistor, we were able to adjust the low-pass corner to the required frequency. This frequency was chosen according to the calculation of the SNR for different low-pass corners as shown in Fig. 7. We calculated the signal amplitude by filtering a spike train, recorded with the SM readout in experiments with cortical neurons. We noticed that the signal amplitude decreased rapidly, when the LPF was set to less than 2 kHz. Given that the noise level decreased faster than the signal amplitude at higher frequencies, the SNR was optimal for an LPF set at 3.3 kHz. Therefore, we used this frequency for all our experiments. Moreover, the LPF is tunable, so that a higher LPF could be set for other applications. The high-pass corner was set to 0.2 Hz to filter the low-

frequency fluctuations from the electrodes. For SM readout, the measured transfer functions of all the readout channels exhibited very small variations with only 0.2% standard deviation of the mid-band gain. The LPF and HPF were set to 6.9 kHz and 0.6 Hz, respectively, to obtain signals from both, AP and LFP band without distortion. We plotted the variation of gain, LPF and HPF; the variation of LPF and HPF was larger in the APS readout than in the SM readout. The variation of the LPF will affect the aliasing noise, however, the noise level for most of the channels was in an acceptable range as shown in Fig. 6.

Noise measurements were conducted for the circuits only (w/o electrode) and for the readout circuits connected to Pt-black-covered array electrodes while the MEA was immersed in a saline solution (w electrode). All measurements were performed with the complete readout chain, including ADCs. The APS readout circuits featured an input-referred noise level of 10.4 μV_{rms} in the AP band without electrodes. We also measured the noise of the pixel amplifier without sampling and aliasing noise, which amounted to 8.9 μV_{rms}. With electrodes, the noise level increased to 11.1 μV_{rms}. Since there is no structure to reject supply noise, the PSRR for the APS readout was low (6 dB). We employed most of the space in the pixel for the input transistors M1 and M2 to reduce noise levels, so that the space was insufficient to implement differential or cascode structures to improve PSRR. Instead, in the setup, we used an off-chip low-noise LDO for the power supply of the first stage amplifier. It is possible to remove the 50-Hz harmonics coming from the power supply during data processing, which reduces the noise levels by around 1–2 μV_{rms}. However, we did not use such data processing for any characterization and measurement results reported in this and other articles [25]. For the SM readout, the noise in the AP band was 3.0 μV_{rms} without electrode, and 3.2 μV_{rms} with electrode. Moreover, the APS SAR-ADC achieved an SNDR of 52.2 dB (ENOB = 8.4) at a sampling rate of 5 MS/s and an input signal frequency of 1.1 kHz. The input range for the measured gain and noise was 8 mV_{pp} for APS and 1.5 mV_{pp} for SM.

Finally, we measured the power consumption of the system (see Fig. 8) including all the circuits (on-chip ADC, IO, biasing, etc.). The power consumption of APS and SM circuits amounted to 5.9 μW/channel and 39 μW/channel, respectively. The measured noise efficiency factor (NEF) [28] and power efficiency factor (PEF) [29] for the APS pixel amplifier amounted to 0.227 and 0.049, respectively. The performance of the DM MEA was compared to that of state-of-the-art devices as summarized in Table I.

2) Light Sensitivity—An open issue with many MEA systems is their light sensitivity, especially when the system needs to be used for retina-related applications, where light patterns are projected onto the array. Many systems show high light sensitivity owing to the leakage currents in the feedback pseudo-resistors [30], [31]. Upon changing light intensity, the drift of the dc offset can cause the readout signal to saturate. For the DM-MEA, we characterized the light sensitivity for both, APS and SM modes. The input-referred recorded raw traces are shown in Fig. 9. The chip was first kept in the dark, and then suddenly exposed to light (approx. 500 lux) after 3.5 s. The corresponding APS and SM voltage traces were recorded simultaneously. The dc offset and gain of both readout modes for darkness and light exposure were calculated (see Fig. 9). The resulting box plot of dc offsets is shown at the right of Fig. 9. Note that the APS readout had a large variation in the dc offset (±0.5

mV), however, it did not show any significant sensitivity to light changes, while the SM readout was more sensitive to light. One possible reason for this difference in light sensitivity may include that different structures of feedback pseudo-resistors were used for the HPF in the first stage. For APS, the MOS resistor was implemented with a transmission gate, including both, pMOS and nMOS elements, connected in parallel. Thus, the leakage current, caused by light, could be compensated. However, for the SM, the pseudo-resistor was composed of nMOS and pMOS elements with a back-to-back connection. As a result, the uncompensated leakage current directly affected the dc levels of the input transistor. The insensitivity to the light of the APS readout renders it suitable for retina-related applications. Moreover, the APS readout could be used with optogenetic techniques to correlate the electrical extracellular signals to could provide more information about the dynamics of the those obtained using optogenetics, the combination of which neurons.

3) Stimulation Unit— Fig. 10 shows exemplary stimulation pulses using the on-chip stimulation buffer. The output of the stimulation buffer was connected to a 500-pF capacitor. Fig. 10(a) shows a ±250-mV voltage stimulation pulse, and Fig. 10(b) shows a ±0.9-μA current pulse and the corresponding voltage changes.

B Electrophysiological Measurements

After initial electrical and functional characterization of the DM-MEA, we used the system to record from biological preparations. Fig. 11 shows the measurement results of various biological preparations. We recorded signals through the same electrode simultaneously with the APS and SM readouts [see Fig. 11(a)]. As expected, the two spike trains were synchronized and the spike amplitudes were similar, while the noise levels and SNR were clearly distinct. In Fig. 11(b), we recorded signals from various biological samples using the APS readout, including primary neurons (preparation protocol described in [32]), mouse hippocampal slices (preparation protocol described in [33]), and iPSC-derived cardiomyocytes (Fujifilm Cellular Dynamics). These signals had different bandwidths, and showed distinct signal shapes.

For cardiomyocytes, we recorded the synchronous beating using APS readouts [see Fig. 11(c)]. We measured the peak to-peak amplitude on each electrode to show the activity of cardiomyocytes across the entire array. Moreover, by plotting the raw signals in frames at different times, we observed the propagation of the cardiac field potentials across the array [see Fig. 11(c)].

Moreover, we characterized dissociated E18 Wistar rat neurons [see Fig. 11(d)]. Fig. 11(d) shows 2-D maps of spike amplitudes and firing rates, recorded by the APS full-frame readout, together with the confocal image of the same culture, which shows that the electrically active areas match the areas showing stained cells in the confocal image. We then extracted an exemplary electrical “footprint” of a neuron [see Fig. 11(e)], which represents the extracellular electrical-potential landscape of a neuron. The plot includes short 5-ms signal cutouts from 924 electrodes averaged over 996 spiking events. From the footprint we could see the morphology and axonal arbors of the respective neuron. Measurements of more biological preparations have been described in [25].

V Conclusion And Outlook

In summary, we presented a DM-MEA system with 19 584 electrodes, 19 584 APS readout channels, 246 SM readout channels, and eight stimulation units. From both, the characterization results and the biological-measurement results, we can conclude that the APS mode offers the possibility of performing large-scale recordings of thousands of neurons across the entire array area at good SNR. In addition, the APS mode shows little sensitivity to light. The SM mode achieves a higher SNR with only 3-μV noise, which offers the possibility to connect SM channels to selected electrodes that may be used to specifically detect low-amplitude neuronal signals including brain-slice signals or axonal signals. Having both modes implemented in a single chip provides great flexibility to serve a wide range of applications with different requirements.

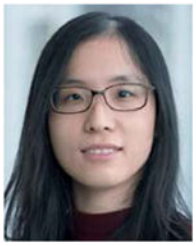
Obvious measures to enhance the DM-MEA performance include, for example, improving the PSRR and CMRR of the APS mode and precisely controlling the high-pass and low-pass corners. Moreover, the applicability could be enhanced by adding more electrodes or by implementing more functionalities on chip, including, e.g., impedance measurements or intracellular recordings.

Acknowledgment

All experimental protocols were approved by the Basel Stadt Veterinary Office, Basel, Switzerland, according to Swiss federal laws on animal welfare and were carried out in accordance with the approved guidelines.

The authors would like to thank A. Stettler, P. Rimpf, and T. Rebac, all at ETH Zurich, for support with CMOS wafer postprocessing, and the Zentrum fur Mikroskopie (ZMB) of the University of Basel, Basel, Switzerland, for taking the scanning-electron-microscope (SEM) pictures. They would also like to thank V. Emmenegger, S. Ronchi, and J. Lee at ETH Zurich, Zurich, Switzerland, and M. E. J. Obien at MaxWell Biosystems, Zurich, for technical support with sample preparations.

Biographical Sketches



Xinyue Yuan received the B.Sc. degree in microelectronics from Fudan University, Shanghai, China, in 2013, the M.Sc. degree in biomedical engineering from ETH Zurich, Zurich, Switzerland, in 2015, and the Ph.D. degree from the Bioengineering Laboratory, ETH Zurich, Basel, Switzerland, in 2020. Her Ph.D. research was focused on the design of CMOS-based high-density microelectrode arrays for neuroscience and pharmaceutical applications.She is currently working as a Circuit Designer and an Research and Development Engineer with MaxWell Biosystems AG, Zurich.

Andreas Hierlemann (Member, IEEE) received the Ph.D. degree in chemistry from the University of Tübingen, Tübingen, Germany, in 1996. He then held post-doctoral positions at Texas A&M University, College Station, TX, USA, in 1997, and Sandia National Laboratories, Albuquerque, NM, USA, in 1998. In 1999, he joined the Department of Physics, ETH Zurich, Zurich, Switzerland, where he was appointed as an Associate Professor in June 2004. In April 2008, he became a Full Professor with the Department of Biosystems Science and Engineering (BSSE), ETH Zurich, Basel, Switzerland. His research interests include the development and application of microsensor, microfluidic, and microelectronic technologies to address questions in biology and medicine with applications in the fields of systems biology, drug testing, personalized medicine, and neuroscience.

Urs Frey (Member, IEEE) received the Diploma degree in electrical engineering from ETH Zurich, Zurich, Switzerland, in 2003, and the Ph.D. degree for his work on high-density neural interfaces and microhotplate gas sensors from the Physical Electronics Laboratory, ETH Zurich, in 2008.From 2009 to 2010, he was with IBM Research Zurich, Zurich, where he worked on mixed-signal circuit design for non-volatile memory devices. In 2011, he joined the RIKEN Quantitative Biology Center, Kobe, Japan, where he was the Head of the Independent Laboratory, focusing on CMOS-based bioelectronics and biosensors. In 2016, he moved back to Switzerland, joined the Department of Biosystems Science and Engineering, ETH Zurich and co-founded MaxWell Biosystems AG, Zurich, where he is currently the Chief Executive Officer.

References

[1]. Shi Y, Inoue H, Wu JC, Yamanaka S. Induced pluripotent stem cell technology: A decade of progress. Nature Rev Drug Discovery. 2017 Feb; 16(2):115–130. [PubMed: 27980341]

[2]. Takahashi K, et al. Induction of pluripotent stem cells from adult human fibroblasts by defined factors. Cell. 2007 Nov; 131(5):861–872. [PubMed: 18035408]

[3]. Yu J, et al. Induced pluripotent stem cell lines derived from human somatic cells. Science. 2007 Dec.318:1917–1920. [PubMed: 18029452]

[4]. Grienberger C, Konnerth A. Imaging calcium in neurons. Neuron. 2012 Mar; 73(5):862–885. [PubMed: 22405199]

[5]. Walz, W, Boulton, AAAA, Baker, GB. Patch-Clamp Analysis: Advanced Techniques. Humana Press; Totowa, NJ, USA: 2002.

[6]. Obien MEJ, Deligkaris K, Bullmann T, Bakkum DJ, Frey U. Revealing neuronal function through microelectrode array recordings. Frontiers Neurosci. 2015 Jan.8:423.

[7]. Zeck G, Jetter F, Channappa L, Bertotti G, Thewes R. Electrical imaging: Investigating cellular function at high resolution. Adv Biosyst. 2017 Nov.1(11)

[8]. Johnson LJ, Cohen E, Ilg D, Klein R, Skeath P, Scribner DA. A novel high electrode count spike recording array using an 81,920 pixel transimpedance amplifier-based imaging chip. J Neurosci Methods. 2012 Apr; 205(2):223–232. [PubMed: 22266817]

[9]. Dragas J, et al. In vitro multi-functional microelectrode array featuring 59 760 electrodes, 2048 electrophysiology channels, stimulation, impedance measurement, and neurotransmitter detection channels. IEEE J Solid-State Circuits. 2017 Jun; 52(6):1576–1590. [PubMed: 28579632]

[10]. Tsai D, Yuste R, Shepard KL. Statistically reconstructed multiplexing for very dense, high-channel-count acquisition systems. IEEE Trans Biomed Circuits Syst. 2018 Feb; 12(1):13–23. [PubMed: 29377795]

[11]. Eversmann B, et al. A 128 × 128 CMOS biosensor array for extracellular recording of neural activity. IEEE J Solid-State Circuits. 2003 Dec; 38(12):2306–2317.

[12]. Frey U, et al. Switch-matrix-based high-density microelectrode array in CMOS technology. IEEE J Solid-State Circuits. 2010 Feb; 45(2):467–482.

[13]. Lopez CM, et al. An implantable 455-active-electrode 52-channel CMOS neural probe. IEEE J Solid-State Circuits. 2014 Jan; 49(1):248–261.

[14]. Ballini M, et al. A 1024-channel CMOS microelectrode array with 26,400 electrodes for recording and stimulation of electrogenic cells in vitro. IEEE J Solid-State Circuits. 2014 Nov; 49(11):2705–2719. [PubMed: 28502989]

[15]. Jun JJ, et al. Fully integrated silicon probes for high-density recording of neural activity. Nature. 2017 Nov; 551(7679):232–236. [PubMed: 29120427]

[16]. Lopez CM, et al. A multimodal CMOS MEA for high-throughput intracellular action potential measurements and impedance spectroscopy in drug-screening applications. IEEE J Solid-State Circuits. 2018 Nov; 53(11):3076–3086.

[17]. Abbott J, et al. A nanoelectrode array for obtaining intracellular recordings from thousands of connected neurons. Nature Biomed Eng. 2020 Feb; 4(2):232–241. [PubMed: 31548592]

[18]. Ogi J, et al. Twenty-four-micrometer-pitch microelectrode array with 6912-channel readout at 12 kHz via highly scalable implementation for high-spatial-resolution mapping of action potentials. Biointerphases. 2017 Dec.12

[19]. Angotzi GN, et al. SiNAPS: An implantable active pixel sensor CMOS-probe for simultaneous large-scale neural recordings. Biosensors Bioelectron. 2019 Feb.126:355–364.

[20]. Yuan, X; , et al. A microelectrode array with 8,640 electrodes enabling simultaneous full-frame readout at 6.5 kfps and 112-channel switch-matrix readout at 20 kS/s. Proc IEEE Symp VLSI Circuits (VLSI-Circuits); 2016 Jun. 1–2.

[21]. Tsai D, Sawyer D, Bradd A, Yuste R, Shepard KL. A very large-scale microelectrode array for cellular-resolution electrophysiology. Nature Commun. 2017 Dec.8(1):1802. [PubMed: 29176752]

[22]. Eversmann, B; , et al. CMOS sensor array for electrical imaging of neuronal activity. Proc IEEE Int Symp Circuits Syst; 2005 May. 3479–3482.

[23]. Bertotti, G; , et al. A CMOS-based sensor array for in-vitro neural tissue interfacing with 4225 recording sites and 1024 stimulation sites. Proc IEEE Biomed Circuits Syst Conf (BioCAS); Lausanne, Switzerland. 2014 Oct. 304–307.

[24]. Berdondini L, et al. Active pixel sensor array for high spatio-temporal resolution electrophysiological recordings from single cell to large scale neuronal networks. Lab Chip. 2009 Sep.9(18):2644. [PubMed: 19704979]

[25]. Yuan X, et al. Versatile live-cell activity analysis platform for characterization of neuronal dynamics at single-cell and network level. Nature Commun. 2020 Dec.11(1):4854. [PubMed: 32978383]

[26]. Yuan, X, Emmenegger, V, Obien, MEJ, Hierlemann, A, Frey, U. Dual-mode microelectrode array featuring 20k electrodes and high SNR for extracellular recording of neural networksProc IEEE Biomed Circuits Syst Conf (BioCAS). Institute of Electrical and Electronics Engineers; Piscataway, NJ, USA: 2018 Oct. 1–4.

[27]. Viswam V, Obien MEJ, Franke F, Frey U, Hierlemann A. Optimal electrode size for multi-scale extracellular-potential recording from neuronal assemblies. Frontiers Neurosci. 2019 Apr.13:385.

[28]. Steyaert M, Sansen W. A micropower low-noise monolithic instrumentation amplifier for medical purposes. IEEE J Solid-State Circuits. 1987 Dec; 22(6):1163–1168.

[29]. Muller R, Gambini S, Rabaey JM. A 0.013 $mm^2$5μW, DC-coupled neural signal acquisition IC with 0.5 V supply. IEEE J Solid-State Circuits. 2012 Jan.47:232–243.

[30]. Wang S, Lopez CM, Ballini M, Van Helleputte N. Leakage compensation scheme for ultra-high-resistance pseudo-resistors in neural amplifiers. Electron Lett. 2018 Mar; 54(5):270–272.

[31]. Lopez CM, et al. A neural probe with up to 966 electrodes and up to 384 configurable channels in 0.13 μm SOI CMOS. IEEE Trans Biomed Circuits Syst. 2017 Jun; 11(3):510–522. [PubMed: 28422663]

[32]. Bakkum DJ, et al. Tracking axonal action potential propagation on a high-density microelectrode array across hundreds of sites. Nature Commun. 2013 Jul; 4(1):1–12.

[33]. Blanton MG, Turco JJL, Kriegstein AR. Whole cell recording from neurons in slices of reptilian and mammalian cerebral cortex. J Neurosci Methods. 1989 Dec; 30(3):203–210. [PubMed: 2607782]

Europe PMC Funders Author Manuscripts

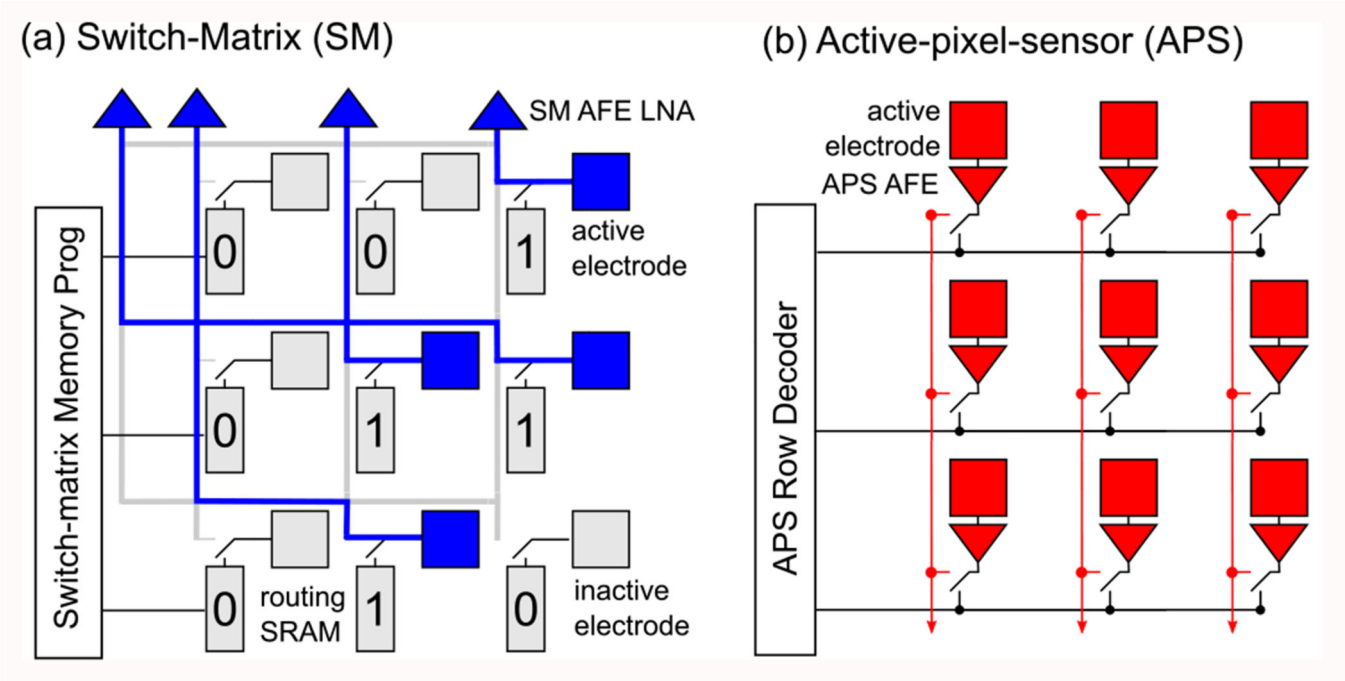


Fig. 1. Illustration of the readout concepts of SM and APS

Europe PMC Funders Author Manuscripts

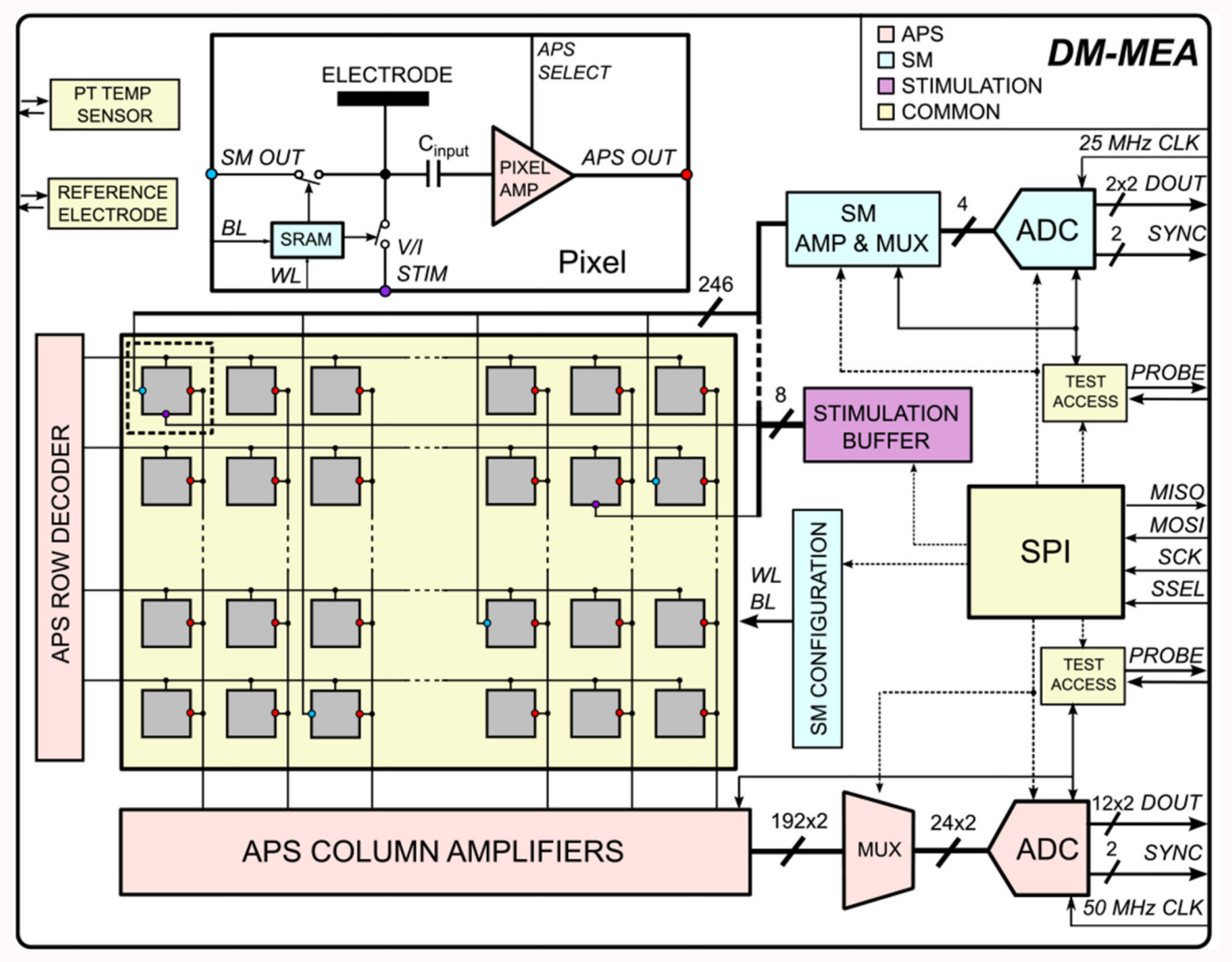


Fig. 2. System diagram of the DM-MEA system, including an electrode array with 19584 electrodes, 19584 APS readout channels, 246 SM readout channels, and eight stimulation units

Europe PMC Funders Author Manuscripts

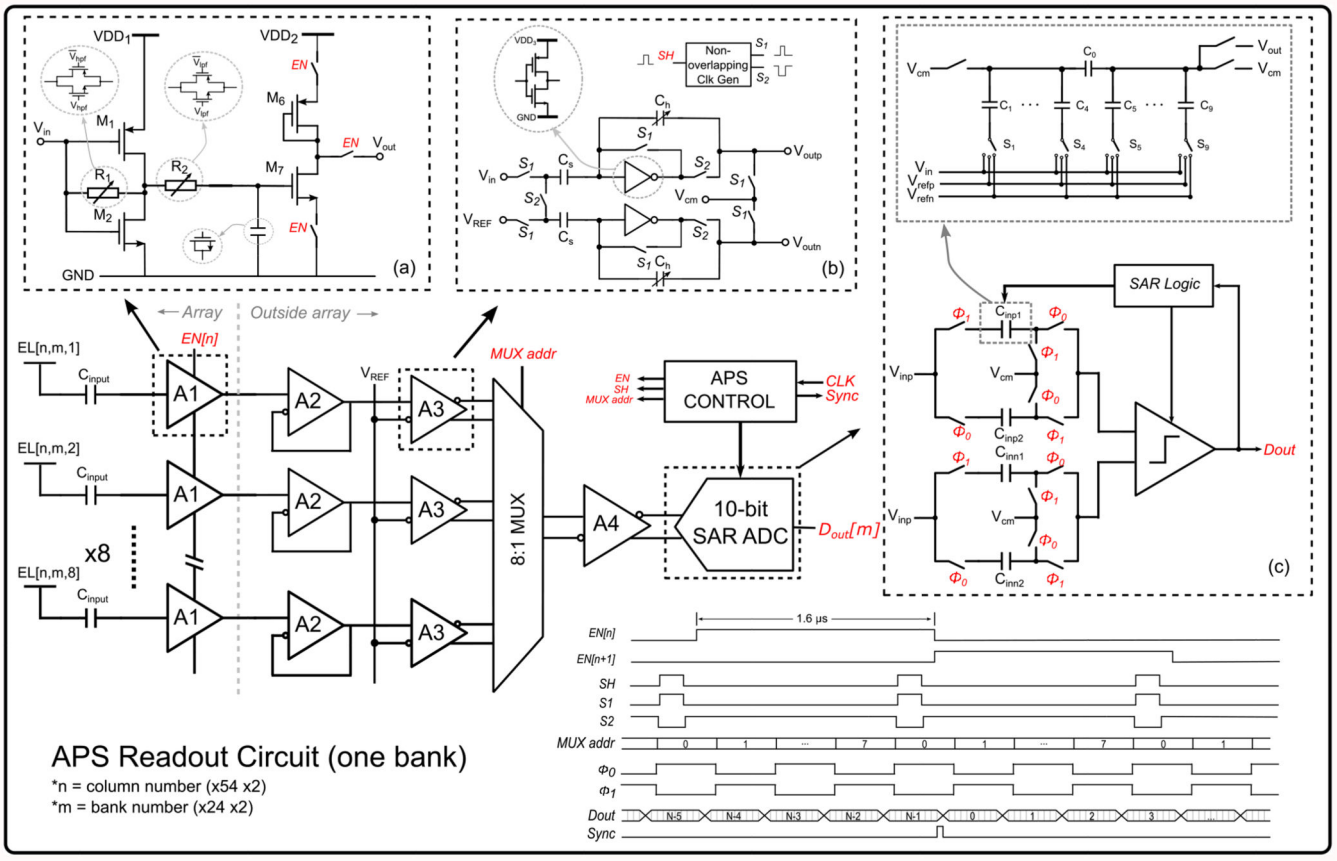


Fig. 3. Circuit for APS readout, including

(a) a pixel amplifier, (b) a S/H amplifier, and (c) a time-interleaved SAR ADC. A total of 54 pixel amplifiers is always connected to one column-readout channel, while eight column-readout channels share one ADC

Europe PMC Funders Author Manuscripts

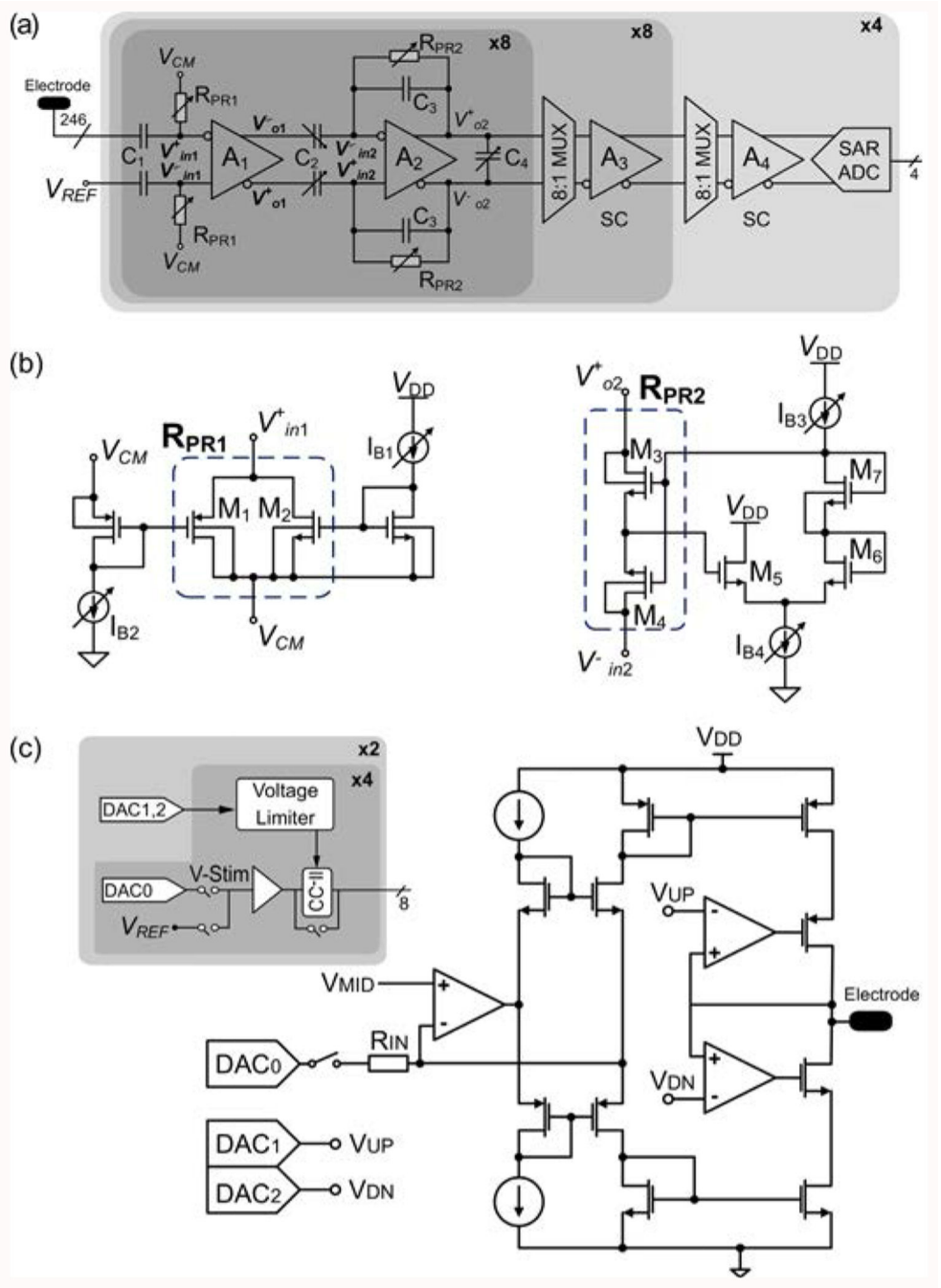


Fig. 4. Circuitry of SM readout and stimulation buffers, adapted from [9]

(a) SM readout circuit (246 channels) with four amplification stages and 10-bit SAR ADC. (b) Structure of the pseudo-resistors RPR1 and RPR2. (c) Circuit diagram of the stimulation buffers, including the connections of DACs (left) and second-generation current conveyor (CC-II, right).

Europe PMC Funders Author Manuscripts

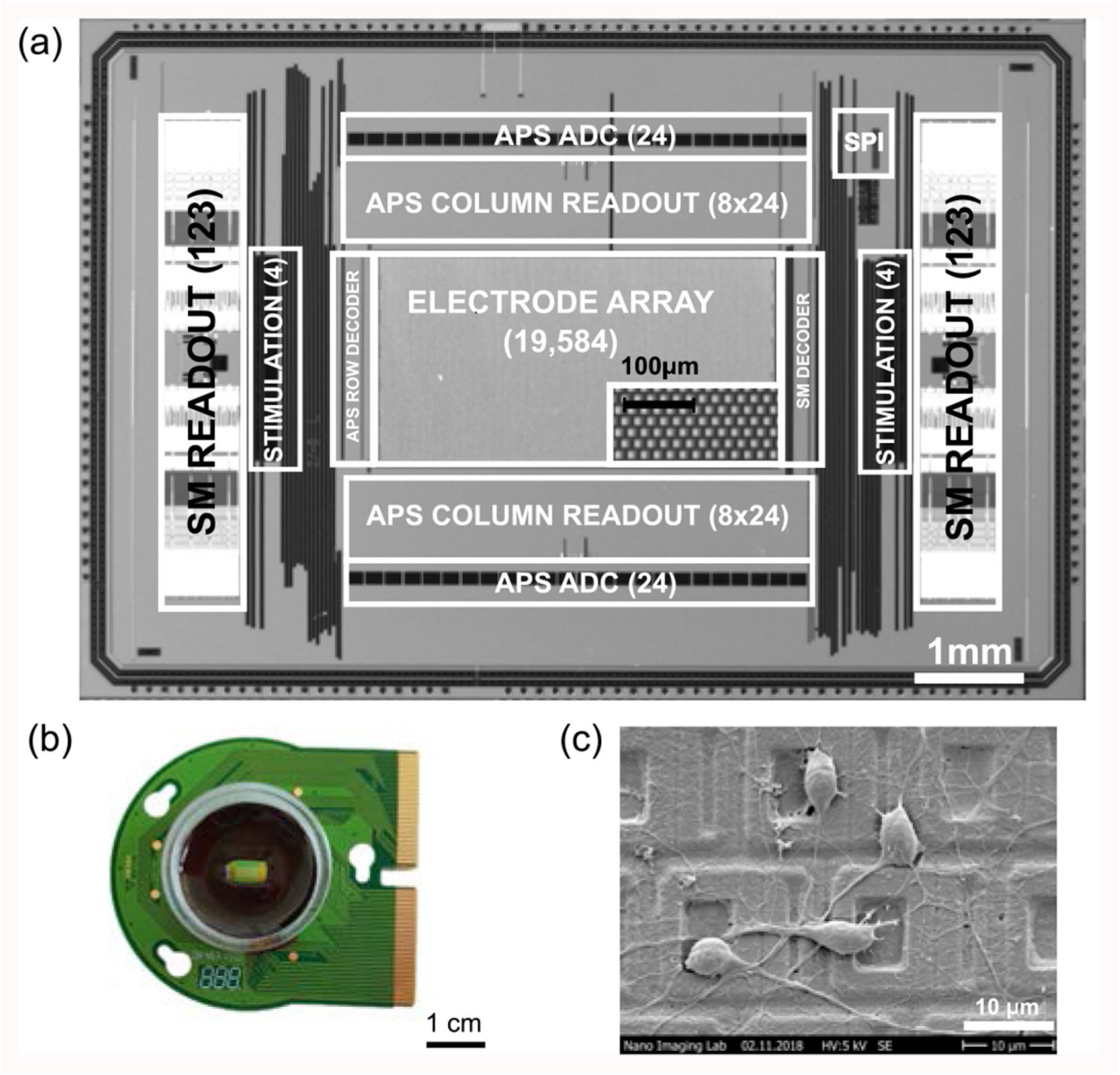


Fig. 5.

(a) Micrograph of the DM-MEA featuring a chip size of 6.0 × 9.0mm^2 andanarraysizeof1.8 × 3.5 mm^2. (b) Packaged chip. (c) Scanning-electron-microscope (SEM) image of cortical neurons on top of the microelectrodes

Europe PMC Funders Author Manuscripts

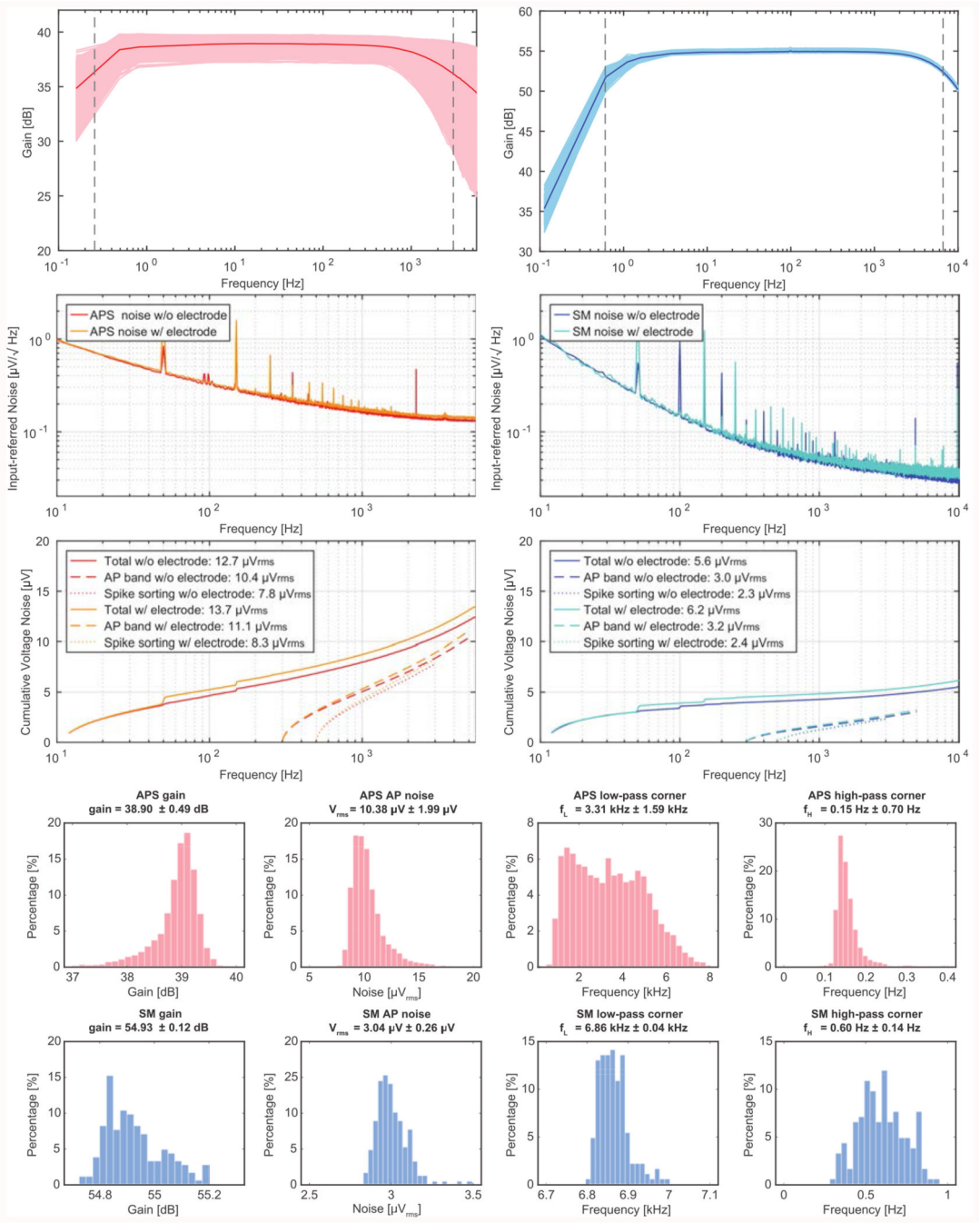


Fig. 6.

Gain and noise measurements for APS and SM readouts, including transfer function, input-referred noise spectra (averaged over 19 584 APS channels and 246 SM channels), noise levels integrated over different frequency bands, and distributions of gain, AP noise, HPF, and LPF. The result is measured for 19 584 APS channels and 246 SM channels

Europe PMC Funders Author Manuscripts

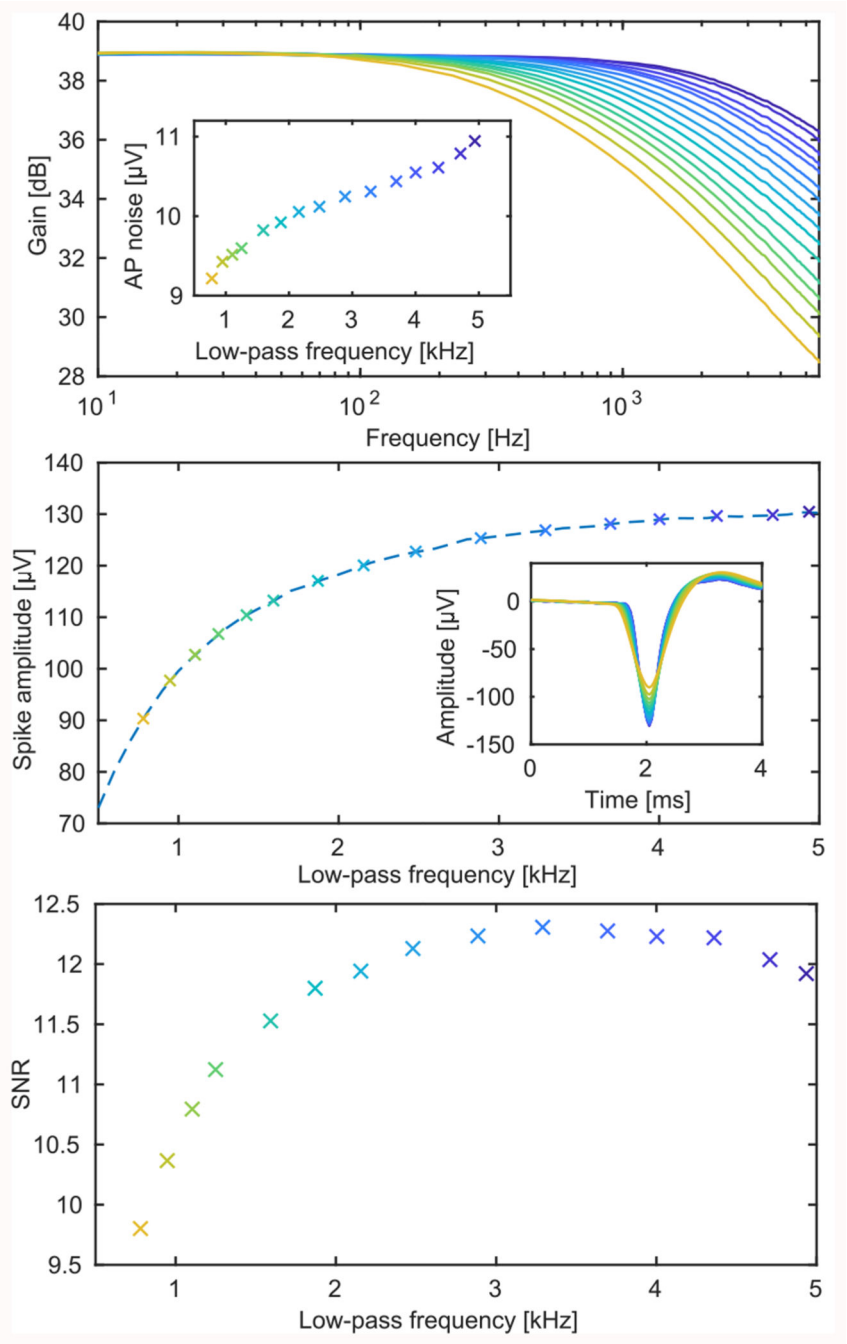


Fig. 7. Low-pass corner measurements including noise and SNR.

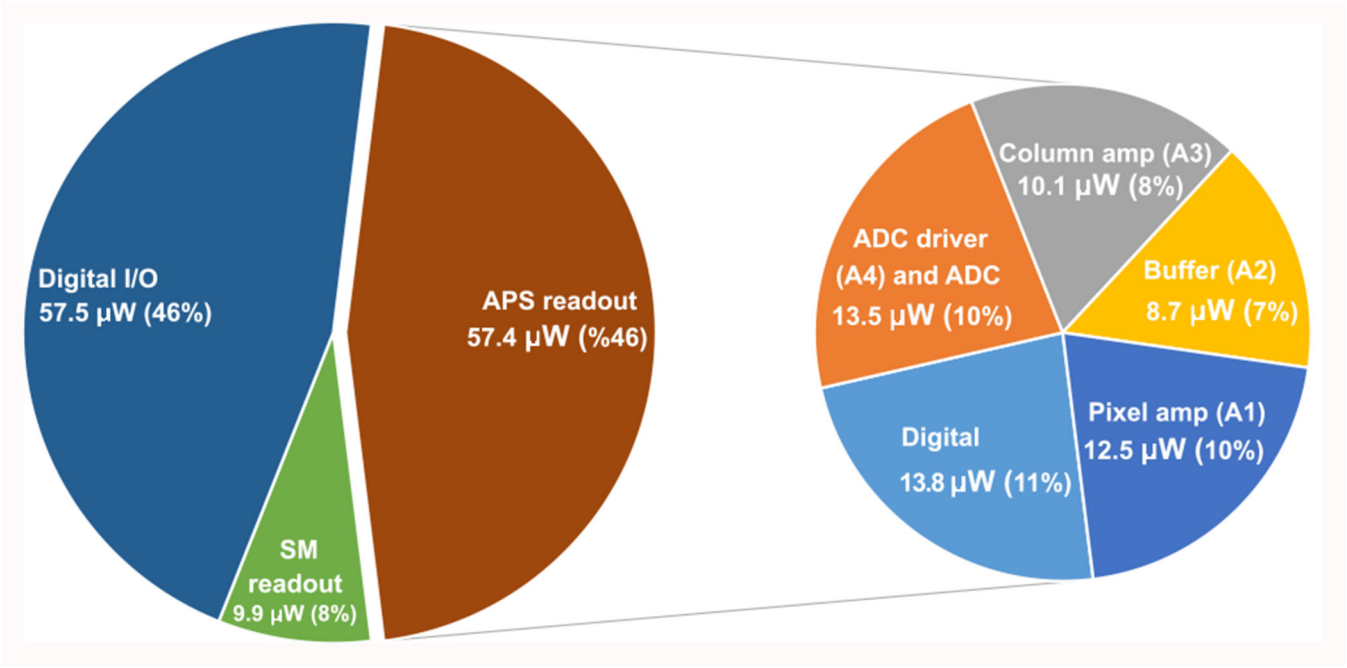


Fig. 8. Pie chart of power consumption contributions of the components of the DM-MEA, which features a total power consumption of 125 mW

Europe PMC Funders Author Manuscripts

Europe PMC Funders Author Manuscripts

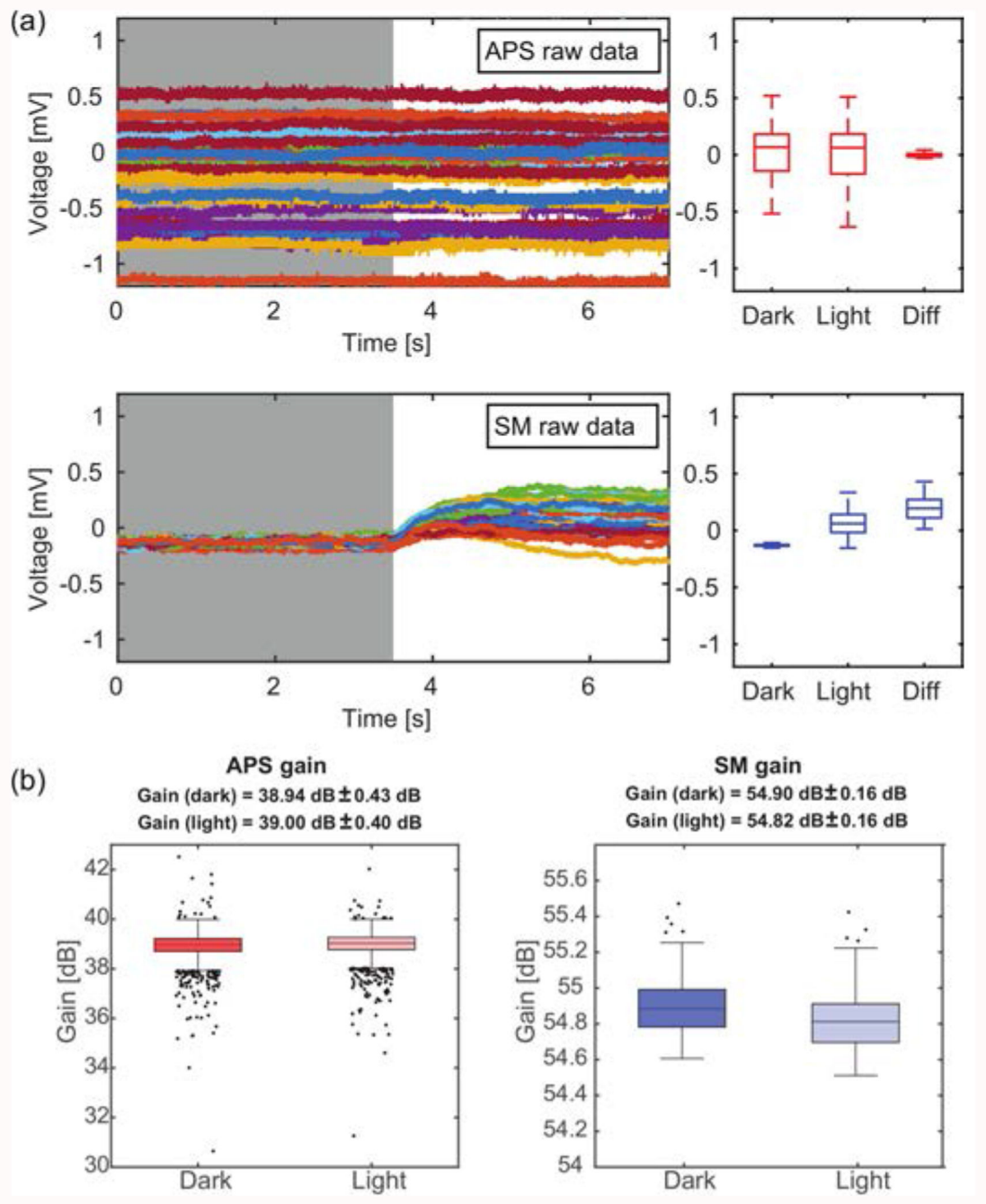


Fig. 9. Characterization of the light sensitivity of the APS and SM readout

(a) Voltage traces of 5184 APS channels and 246 SM channels are plotted for a transition from darkness to white light (500 lux). (b) Characterization for the effect of light on the gain of the APS and SM readout under dark and light conditions. The result is obtained from 19 584 APS channels and 246 SM channel.

Europe PMC Funders Author Manuscripts

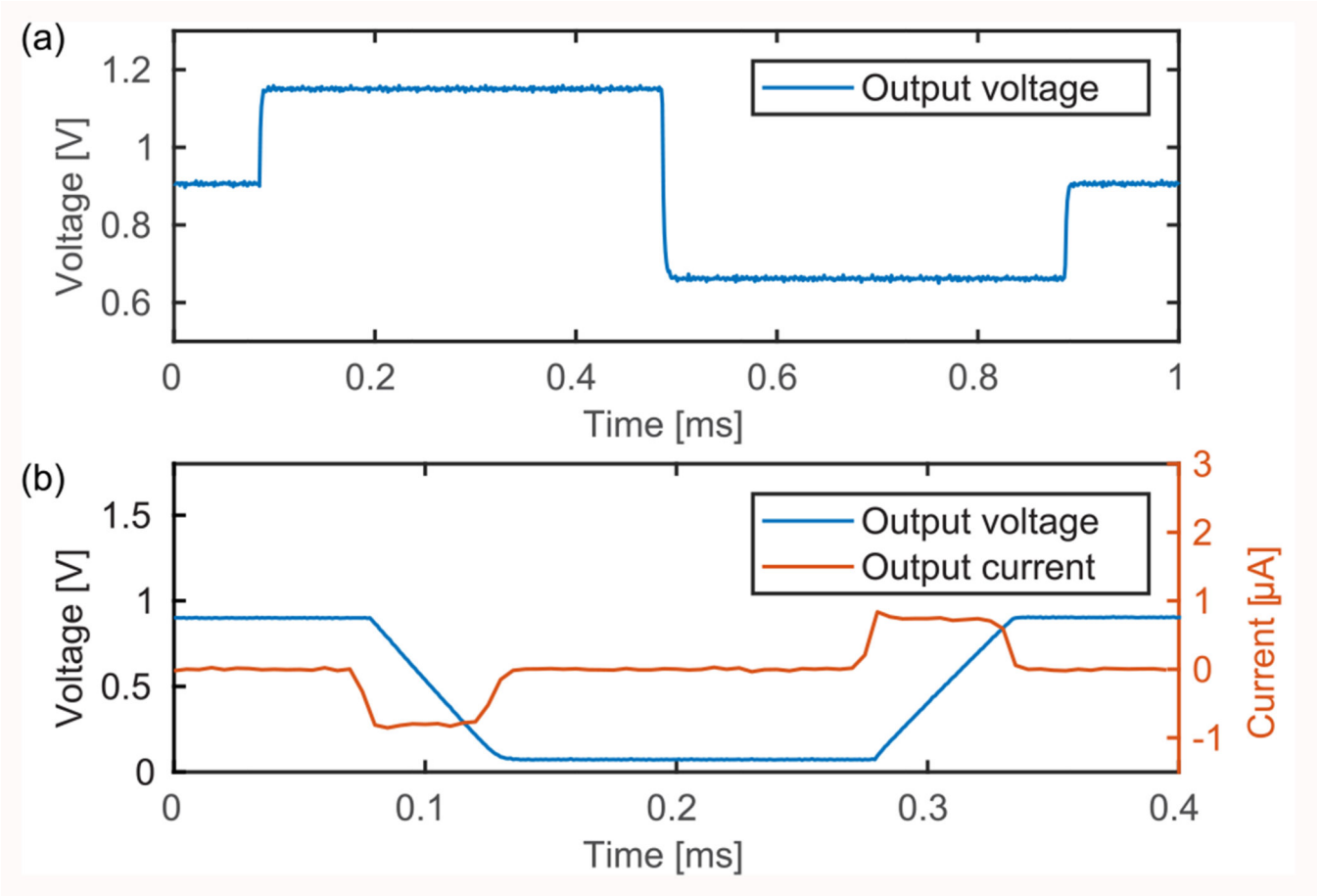


Fig. 10.

Characterization of the stimulation buffer, showing results for (a) voltage-controlled stimulation and (b) current-controlled stimulation.

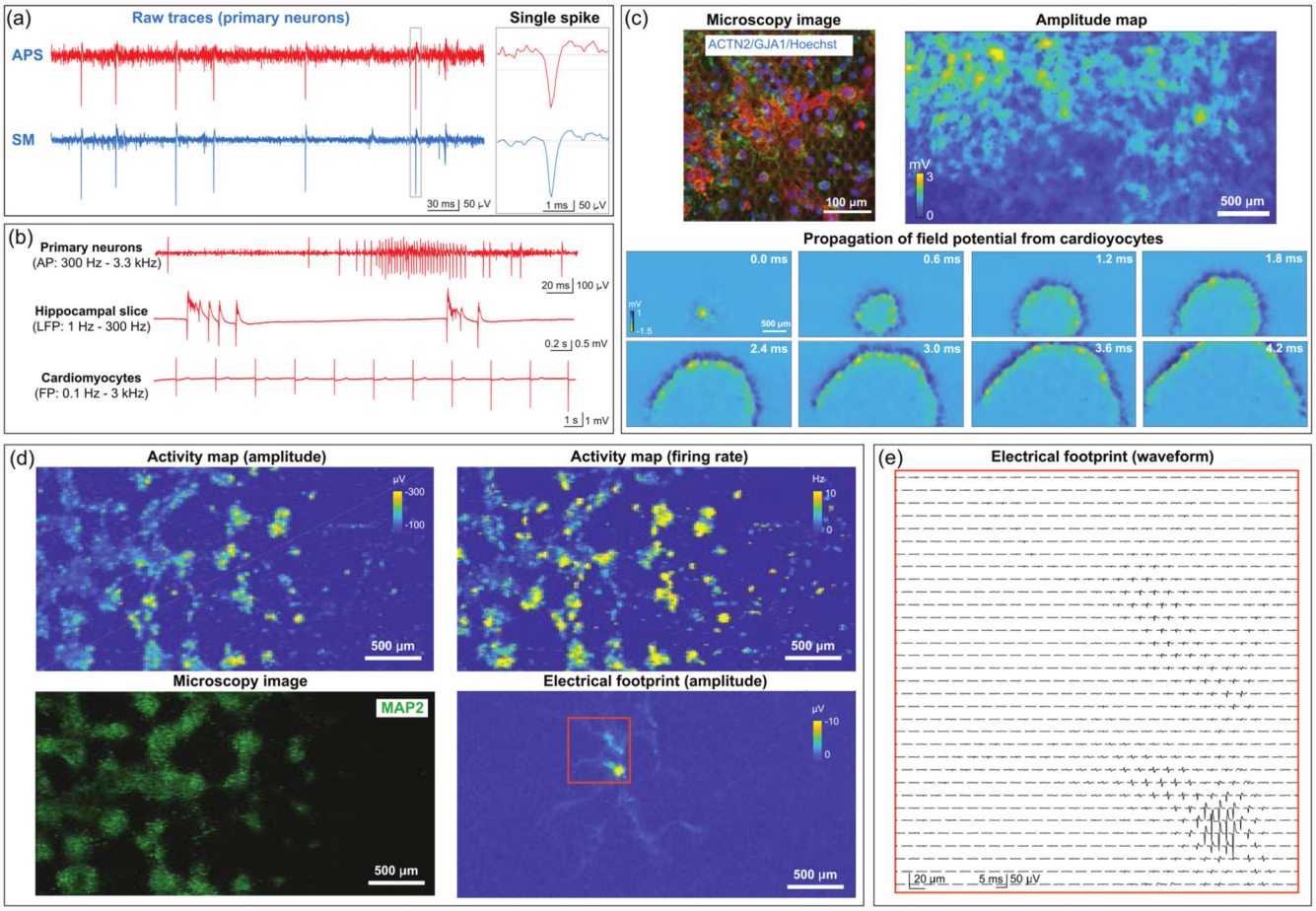


Fig. 11. Measurement results of biological samples

(a) Raw traces of the electrical activity of primary rodent neurons, recorded from the same electrode using APS and SM readouts simultaneously. (b) Signals recorded from various biological samples within different frequency bands using the APS readout, including primary neurons, hippocampal slices and iPSC-derived cardiomyocytes. (c) Measurement results of cardiomyocytes, including a microscopy image, the electrical-activity map (peak-to-peak amplitude), and the temporal evolution of cardiac-field-potential propagation. (d) Measurement results of primary neuronal cultures, including activity maps for spike amplitudes and firing rates, a confocal-microscopy image of the same culture with live immunostaining. (e) Electrical footprint of a single neuron, which shows small 5-ms signal cutouts (averaged from 996 spiking events) from 924 electrodes.

Europe PMC Funders Author Manuscripts

Europe PMC Funders Author Manuscripts

Table 1

Comparison To State-Of-The-Art *In Vitro* CMOS-Based MEA Systems

Reference	Dragas '17 [9]	Ballini '14 [14]	Lopez '18 [16]	Abbott'20 [17]	Tsai'17 [21]	This work	
Mode	**SM**	**SM**	**SM**	**APS**	**APS**	**SM**	**APS**
Technology [μm]	0.18	0.35	0.13	0.18	0.18	0.18	
Die size [mm^2]	12 × 8.9	10.1 × 7.6	19.2 × 10.0	-	-	6.0 × 9.0	
Active area [mm^2]	4.48 × 2.43	3.85 × 2.10	1.92 × 1.92	1.28 × 1.28	6.5 × 6.5	3.5 × 1.8	
No. electrodes	59,760	26,400	16,384	4096	65,536	19,584	
Pixel pitch [μm]	13.5	17.5	15.0	20.0	25.5	18.0	
Electrode density [mm'^{2}]	5,487	3,265	4,444	2,560	1,538	3,050	
No. readout channels	2,048	1,024	1,024	4096	65,536	246	19,584
Sampling rate [kHz]	20.0	20.0	20.0	9.4	10.0	24.4	11.6
ADC resolution	10	10	10	External	External	10	10
Input-referred AP noise [μV_{rms}]	2.4 (300 Hz - 10 kHz)	2.4 (300 Hz - 10 kHz)	7.5 (300 Hz - 10 kHz)	20 (1 Hz - 4.7 KHz)	21.7* (100 Hz - 3 kHz)	3.0 (300 Hz - 5 kHz)	10.4 (300 Hz - 5 kHz)
Power /channel [μW]	42	73	19.8	-	2.3	39.1	5.9

*Noise values before signal processing.