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Performance Analysis of Full Adder using Ganged CMOS Threshold Element with Different Technologies

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ABSTRACT

A threshold gate is a type of digital logic gate that has multiple inputs and a single output. The output of the gate is determined by the number of inputs that are at a high (or 1) state. The threshold value, or number of inputs required to be at a high state, is set by the design of the gate. These gates are used in digital circuits to perform Boolean logic operations and are commonly used in computer processors and other digital devices. The inputs are multiplied by weights (W_i) and added to produce a resultant sum, which is then compared with threshold value 'T' to get the output Y. The values of weights and threshold should be real, finite, positive or negative numbers. In this paper we have designed a Ganged Complementary Metal Oxide Semiconductor Field Effect Transistor (GCMOS) 1- bit Full-Adder (FA) circuit. For all the simulations, A, B and C_{in} are taken as three binary inputs. The major advantage of this Ganged CMOS logic based FA circuit is its simplicity and lower transistor count. The circuit is simulated using Microwind tool with 50nm, 70nm and 90nm CMOS technologies.

Keywords: *Threshold logic gate, GCMOS, CMOS, full adder*

INTRODUCTION

Synapse is a structure in the nervous system that allows a signal to pass from one neuron to the next or to a target effecter cell. A mathematical function conceived as a model of biological neurons is an artificial neuron. Threshold Logic Gate (TLG) or Linear Threshold Unit was the first artificial neuron proposed by Warren McCulloch and Walter Pitts in 1943[1-5]. A TLG is having more than one binary Inputs and a single binary output. The inputs are multiplied by weights (W_i) and added to produce a resultant sum, which is then compared with threshold T to get the output Y. The values of weights and threshold should be real, finite, positive or negative numbers. Threshold function can be represented by Eq.1.

$$\left.\begin{array}{l} Y = \text{Sign}\{F(x)\} = 0, \text{ if } F(x) < 0 \\ \quad\; = 1, \text{ if } F(x) \geq 0 \end{array}\right\} \quad (1)$$

Where, $F(x) = \sum W_i * X_i - T$

Various logic functions can be implemented just by changing the values of W_i and T. TLG circuits designed so far used resistor, capacitor, tunnel-diodes, MOSFET, memristor and negative resistance devices. But owing to the extremely low power consumption and fast signal propagation property, CMOS are considered here as the most versatile component

[6-11] also used for designing threshold

logic gates. Threshold logic-based design can operate at high speed in the range of 400MHz. The logic symbol of TLG is shown in Fig.1.

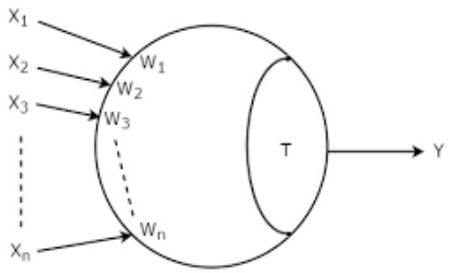

Fig. 1: *Threshold Logic Gate.*

SYNTHESIS OF THRESHOLD FUNCTIONS

Because threshold gates can be used to implement any Boolean function, they are also referred to as universal gates. It may not always be possible to use a single Threshold gate to implement many logic gates and Boolean functions. Multiple threshold gates may be required in that scenario.

To use a single Threshold gate to implement a Boolean function, follow these steps.

Step1: Create a Truth table for the Boolean function you're given.
Step2: Add one more column to the Truth table above to show the relationship between weighted sums and the threshold value.
Step3: Write down the relationship between the threshold and weighted sums for each

Combination of the following inputs:

1. The weighted sum for those input combinations will be greater than or equal to the Threshold value if the Boolean function's output is 1.
2. The weighted sum for those input combinations will be lower than the threshold value if the Boolean function's output is 0.

Step4: Choose the weights and threshold values in such a way that they should satisfy all of the relationships in the table's last column.
Step5: With those weights and threshold values, draw the Threshold gate symbol.

Ganged-CMOS Logic

Ganged-CMOS logic (GCMOS) is a method that drives one or more encoding inverters by using CMOS inverters with their outputs shorted together. Quantifying the non-binary signal at the "ganged" node with these encoding inverters effectively buffers it from external circuitry, allowing for locally smaller noise margins.

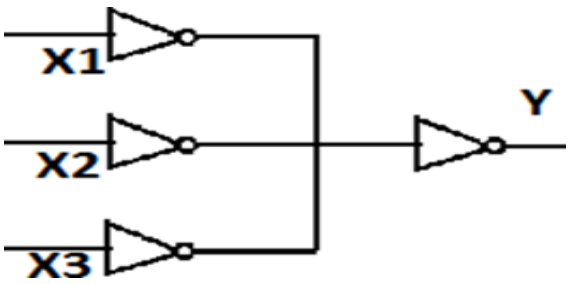

Fig. 2: *Ganged CMOS.*

There are a few benefits to buffering the ganged node with a straightforward CMOS inverter. First and foremost, the ganged node is effectively isolated from external circuitry because its value is not transmitted via long interconnect wires and corrupted by noise, nor does it drive complex gates, where a logic error can be caused by voltages exceeding a transistor threshold [12-19]. In essence, noise margins at a local node are much lower than at a global node. The inverter's inherent encoding action, which results in a clear distinction between low and high inputs thanks to its high gain, amplifies this advantage. Additionally, despite the fact that the inverter's switching point is determined by the square root of the p-n ratio, transistor geometries can be sufficiently varied. GCMOS logic implementation of three input threshold function is shown in Fig.3 which needs eight transistors. The schematic of GCMOS threshold logic element, simulation results and layout is shown in Fig.3, Fig.4 and Fig.5 respectively.

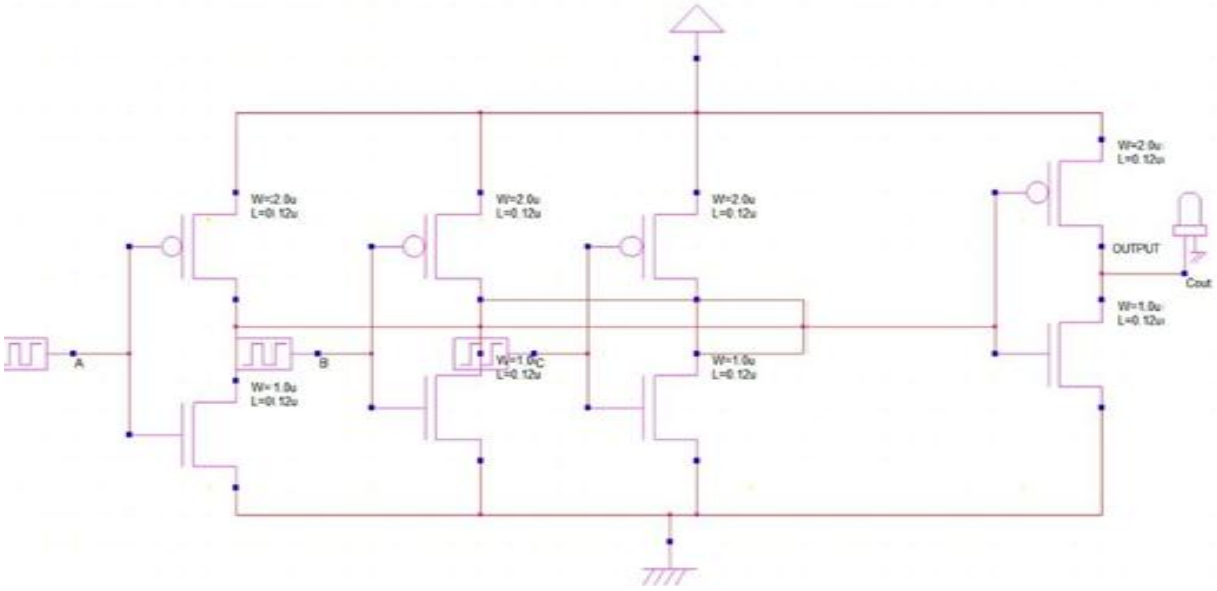

Fig. 3: *Realization of GCMOS logic using MOSFET.*

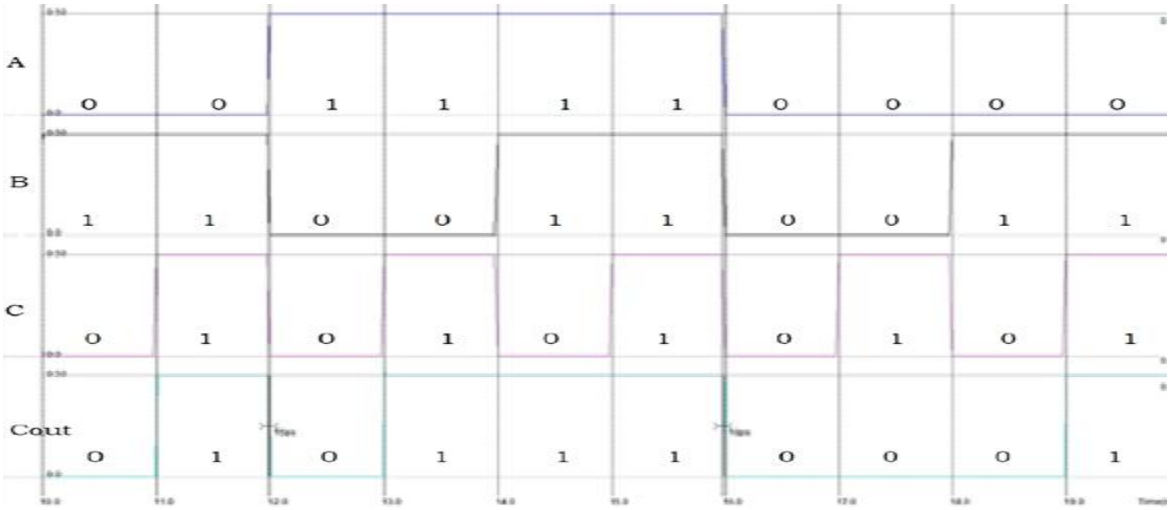

Fig. 4: *Simulation results of GCMOS logic.*

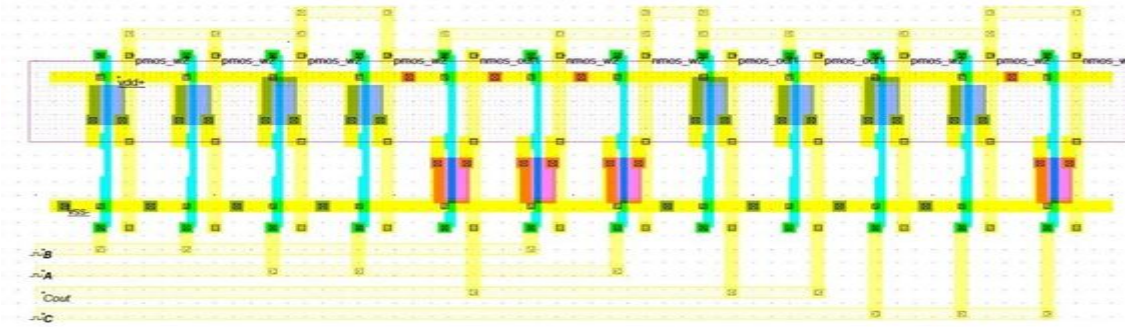

Fig. 5: *Layout of GCMOS logic element.*

Full Adder using GCMOS Logic

A Full Adder is a digital circuit that performs the operation of addition of two binary numbers. It consists of three inputs (A, B, and Cin) and two outputs (Sum and Cout). The input A and B represents the two binary numbers to be added and Cin is the carry input. The output Sum represents the sum of the two binary numbers and Cout is the carry output.Fig.5 shows the realization of FA circuit using GCMOS Threshold Logic. The realization of Full Adder circuit using GCMOS logic is shown in Fig.6.The simulation results of FA with different technologies as shown in Fig.7, 8 and 9 respectively. Fig.10 shows the Full Adder circuit layout in 50nm CMOS technology.

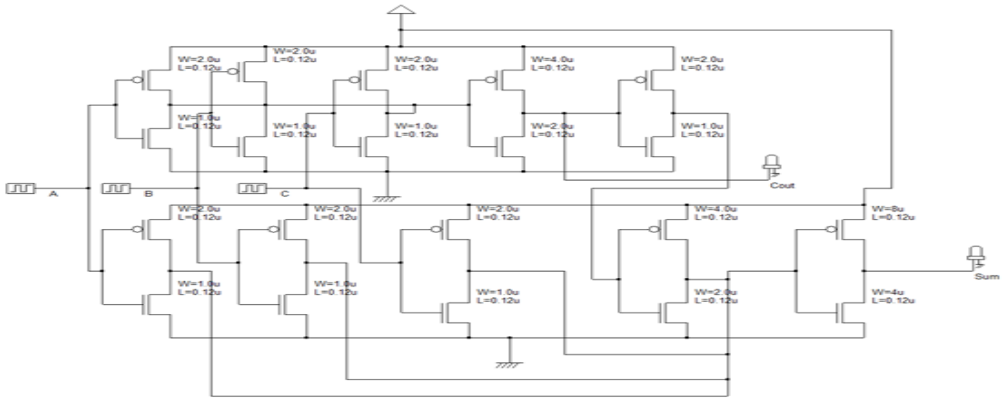

Fig. 6: *Full adder using GCMOS Threshold Logic.*

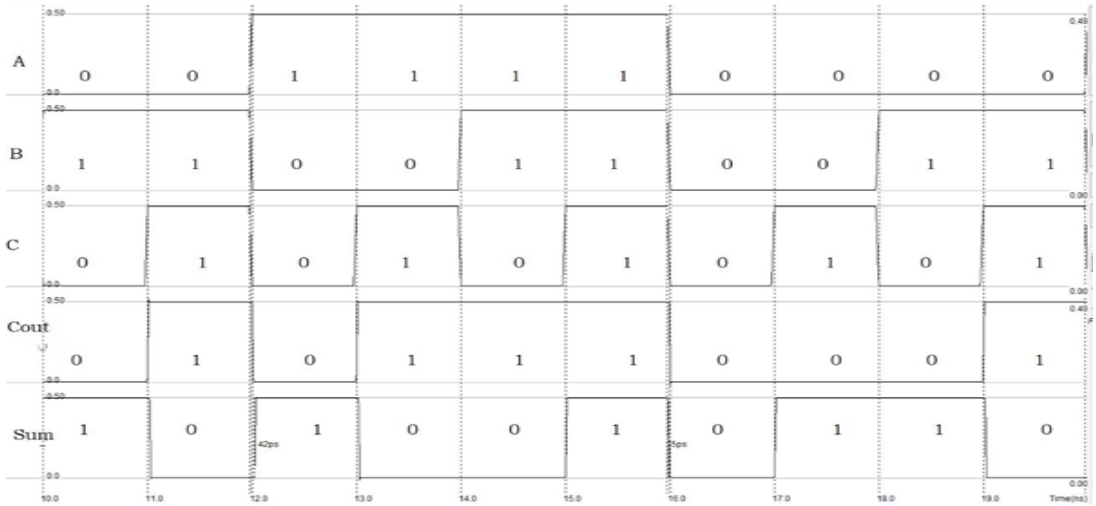

Fig. 7: *Full adder in 50nm CMOS technology.*

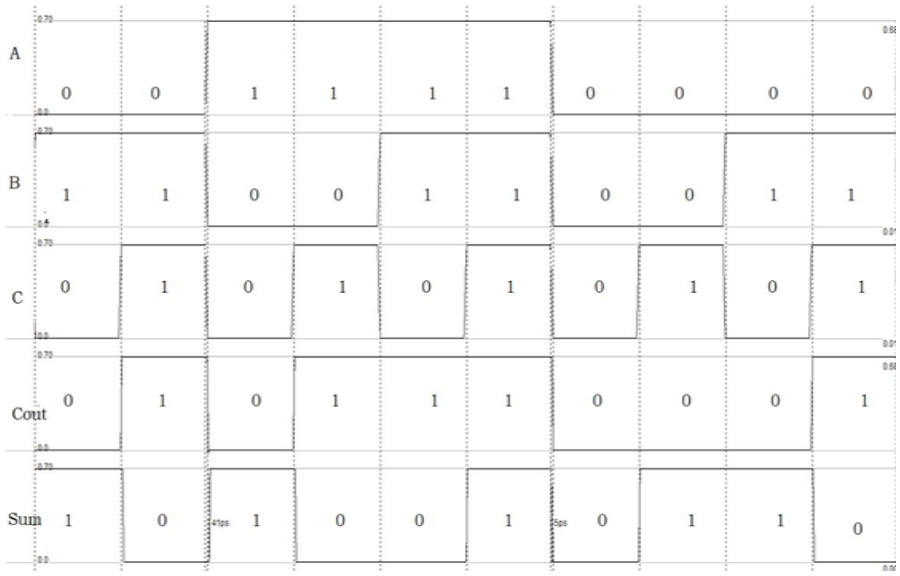

Fig. 8: *Full adder in 50nm CMOS technology.*

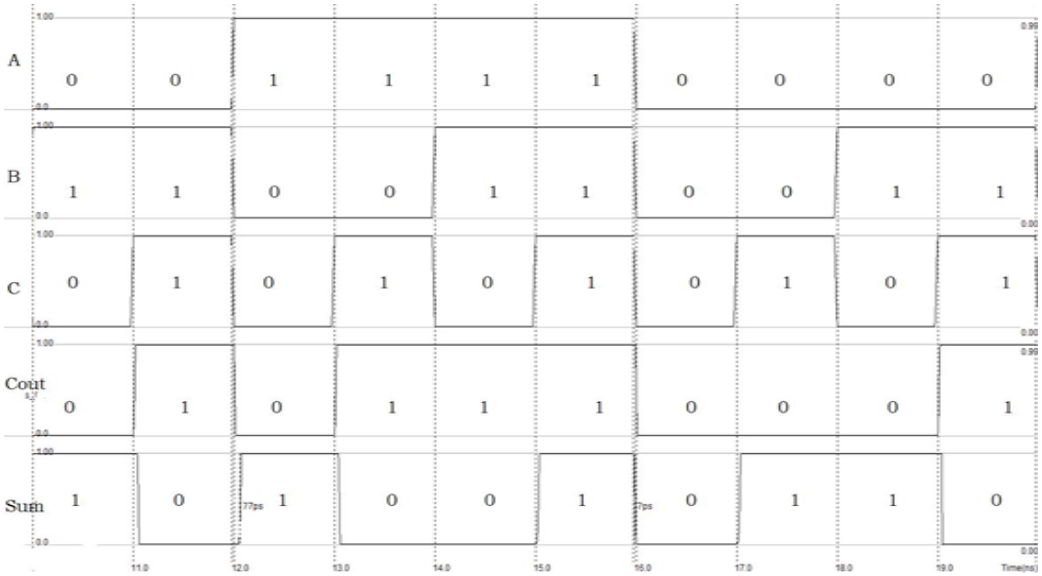

Fig. 9: *Full adder in 50nm CMOS technology.*

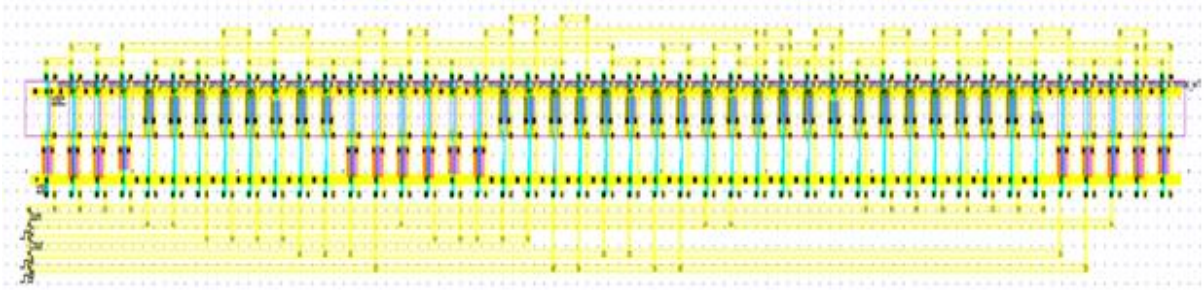

Fig. 10: *Full Adder layout in 50nm CMOS technology.*

Table 1 shows the simulation results of GCMOS Logic element with different CMOS technologies like 50nm, 70nm and 90nm.

Table 2 shows the simulation results of Full Adder circuit using GCMOS Threshold Logic element with different CMOS technologies like 50nm, 70nm and

90nm. The simulation results shows that 50nm technology node gives the 25% accurate than the 70nm and 90nm technology nodes. It has the less power consumption, delay time and area is less when compared with 70 and 90nm technologies.

Table 1: *Simulation results of GCMOS Threshold Logic element.*

Technology (nm)	Power (mW)	Delay (ps)	PDP (fJ)	Area (nm^2)
50nm	0.515	46	2.575	0.02872
70nm	2.060	45	12.36	0.05583
90nm	4.247	87	38.223	0.11585

Table 2: *Simulation results Full Adder using GCMOS Threshold Logic element.*

Technology (nm)	Power (mW)	Delay (ps)	PDP (fJ)	Area (nm^2)
50nm	0.69	5	3.45	0.112
70nm	2.060	6	12.36	0.223
90nm	4.535	9	40.815	0.455

CONCLUSION

In this paper GCMOS Logic threshold element and 1-bit Full Adder circuit using GCMOS threshold Logic element is simulated with different CMOS technologies like 50nm, 70nm and 90nm. The simulation results shows that Full Adder circuit with 50nm technology node gives the 28% accurate than the 70nm and 90nm technology nodes. In this work simulation results are verified using Micro wind tool.

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