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AIDAinnova

Advancement and Innovation for Detectors at Accelerators

Horizon 2020 Research Infrastructures project AIDAINNOVA

MILESTONE REPORT

DESIGN REVIEW OF 65/130 NM RUN

MILESTONE: MS46

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Abstract:

WP11.3 aims at developing ASICs in 65/130nm technology for the readout of detectors developed by the other AIDA-INOVA WPs. An engineering run in TSMC 130nm is foreseen early 2023 to provide such ASICs. The chips ready to go in this fabrication are reviewed for the completion of MS46 milestone.

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Delivery Slip

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TABLE OF CONTENTS

Executive summary

Complex readout ASICs are an essential tool for detector operation and performance, and their development is the objective of task WP11.3 in the microelectronics work-package. These chips are increasingly sophisticated, including multi-channel low noise preamplifiers, shapers, digitizers and signal processing. They are developed for detector characterization in testbench and test beam of the other work-packages and allow to address system issues early in the detector design.

More recently picosecond timing performance is an important aspect of detector R&D and several ASICs have been developed specifically for this issue.

Finally significant chip quantities are necessary for detectors such as imaging calorimeters (WP13), which is provided by shared engineering runs that offer readout for thousands of channels at an affordable price. This is the object of the deliverable of WP11.3 and prior to the fabrication a design review is held to verify the maturity of the designs and this constitutes milestone MS46.

1. INTRODUCTION

New detectors rely more and more heavily on the development of high performance readout ASICs that are often even integrated right into the detectors. For example tracking detectors are bump-bonded to their readout chip or imaging calorimeters need their readout chips inside their layers. Getting the timing performance to a few tens of picoseconds with LGAD sensors or SiPMs requires special high speed (GHz) readout ASICs with integrated Time to Digital Converters (TDCs).

For detector characterization, in particular for calorimeters, several hundreds of chips are needed, which exceed the usual quantity (40) obtained in Multi-Project Wafers (MPW). An engineering run allows our own MPW, getting 10 wafers with 100 chips per wafer. The large price of the engineering run (~250 k€) needs to be shared with other projects in order to reach an affordable price. This way AIDA-INOVA can have 4 ASICs for the project, while contributing only 25% of the total price.

All the chips implemented in this fabrication are re-using several silicon-proven blocks in order to minimize the risks of producing large quantities of non-working chips. However, several innovative features are often added in order to test new blocks with detector, but they can be removed by slow control in case of malfunction.

The chips have been reviewed by the two WP11 convenors at the beginning of November 2022. The reticle is being assembled in December, and the fabrication is reserved at TSMC for January 2023, prompted by the main financial contributors of the run.

Another fabrication at the end of 2023 is very likely to occur so that more chips from other partners which are not yet ready be available in one year.

2. 130 NM AIDA ENGINEERING RUN DESCRIPTION

2.1. LGAD READOUT CHIPS : EICROC [4.1]

EICROC is a 16-channel readout ASIC designed by partner OMEGA for 500x500um AC-LGAD sensors. Comprised of a GHz preamplifier and discriminator followed by a 20 ps TDC (IRFU design) and 8-bit ADC (Krakow design), it provides time and position measurement to an accuracy of 20 ps and 50 um. With a target power of 1 mW/channel, it should be extendable to 16*16 sensors, providing an interesting R&D path to high accuracy, picosecond timing performance trackers. The design re-uses several blocks from other chips, in particular the very front-end from ATLAS HGTD ALTIROC ASIC. The ADC and TDC were derived by the partners from designs implemented in the CMS HGCAL HGCROC chip.

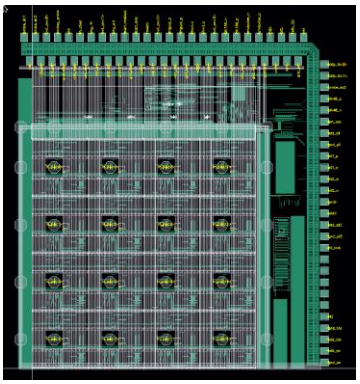

Figure 1: EICROC layout

2.2. GAAS SENSOR READOUT CHIP : FLAXE [4.2]

FLAXE is a 32-channel ASIC designed by partner AGH to readout GaAs semiconductor detectors. Integrating an ultra-low noise preamplifier and a 10bit 40MHz ADC per channel, FLAXE provides large dynamic range waveforms from GaAs sensors. Extra digital signal processing reduces the data volume to extract the main signal parameters, such as amplitude and time of arrival, to 1 ns accuracy. FLAXE is derived from a previous design FLAME from AGH aimed at ILC forward calorimeter readout.

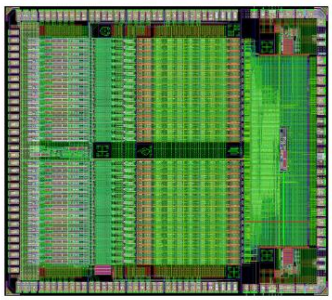

Figure 2: FLAXE layout

2.3. SIPM TIMING READOUT CHIP : LIROC [4.3]

LIROC is a 64-channel chip designed by partners OMEGA and WEEROC to provide high-speed preamplifier and discriminator for SiPM single photon timing resolution. With 1 GHz bandwidth and 3 ns double pulse separation LIROC can be used for LIDAR applications in space. The high-speed CLPS outputs make it natively interfaced with pico-TDC ASIC developed by CERN for picosecond timing resolution.

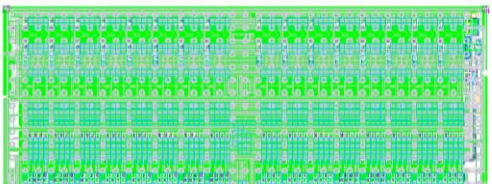

Figure 3: LIROC layout

2.4. SILICON OR GASEOUS DETECTOR READOUT : PSIROC

PSIROC is a 64-channel ASIC designed by partner WEEROC to readout silicon or gaseous detectors. Featuring a low noise charge preamplifier, variable shaper, discriminators and multiplexed readout it can be used with even large capacitance sensors as found in gaseous detectors. Dual input polarity and Time over Threshold capability provide a large dynamic range.

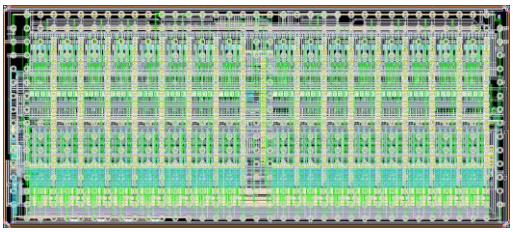

Figure 4: PSIROC layout

3. RETICLE ARRANGEMENT

The reticle for fabrication is shown below in Figure 5. As AIDA INOVA is contributing financially to a small fraction of the total cost (25%), it benefits from a fabrication shared with other chips for other projects which pay for most of the price of the fabrication (~250 k€). This provides an efficient way of getting several hundreds of chips necessary for detector characterization while an MPW would cost 3 times more and provide only 40 chips. The wafers are diced non-sacrificially in order to recover all the chips.

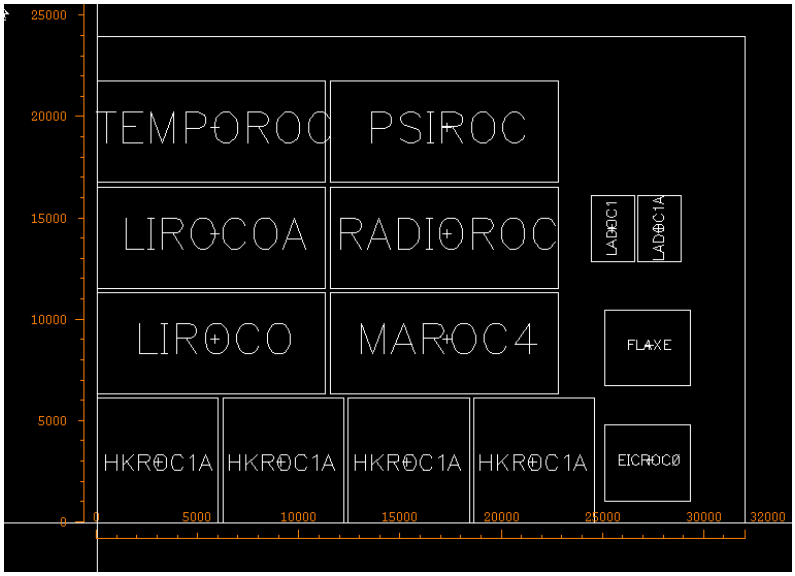

Figure 5:Chip placement in the reticle..

4. REFERENCES

4.1. EICROC0

https://indico.phys.sinica.edu.tw/event/52/contributions/222/attachments/204/339/yezhenyu_TIDC20220819.pdf

4.2. FLAXE

https://indico.desy.de/event/34866/contributions/123792/attachments/75123/96345/idzik_luxe_flaxe_06_2022.pdf

4.3. LIROC

https://phase1.attract-eu.com/showroom/project/novative-radhard-front-end-asic-for-lidar-liroc/

ANNEX: GLOSSARY

Acronym	Definition
ASIC	Application Specific Integrated Circuit
MPW	Multi Project Wafers
LGAD	Low Gain Avalanche Diode
SiPM	Silicon Photo Multiplier