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A comparison statement on DCPWM based conducted EMI noise mitigation process in DC-DC converters for EV

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Article Info	ABSTRACT
	Fast switching techniques at high frequencies are employed for quick charging and energy conversion in electric vehicle (EV) power converters. Electromagnetic interference (EMI) noise is produced due to the fast-switching process, which may result in malfunctioning and degraded EV performance. In this work, a digital chaotic pulse width modulation (DCPWM) technique-based EMI noise mitigation process has been applied to elementary positive output super lift Luo (EPOSLL), two-stage cascaded boost (TSCB), and ultra-lift Luo (ULL) converters, and a comparison study has been conducted with EMI reduction levels as per electromagnetic compatibility (EMC) standards. The duty cycle is varied from 0.5 to 0.67 to get the desired output voltage as an input of 10V to achieve the power ratings of 40 W to 80 W for various load conditions. A total of 4 dBV (3 V) to 15 dBV (10 V) of conducted EMI noise has been mitigated for the above-said converters. Simulation results based on power spectrum density and hardware results based on fast fourier transform (FFT) of output voltages are analyzed. According to the findings, the ULL converter is more acceptable for electromagnetic compatibility in EV applications than EPOSLL and TSCB DC-DC converters. *This is an open access article under the [CC BY-SA](#) license.*

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1. INTRODUCTION

Nowadays compact size solid-state electronic devices-based equipment is occupied in most of the industries and home-based appliances. Further, the design engineers are concentrated on reducing the circuit area and increasing the processing speed by varying the switching frequency rapidly. Due to the above-said reasons, electromagnetic interference (EMI) has been generated and it should be carefully mitigated. Electromagnetic compatibility (EMC) defines a limitation of EMI noise that is generated or radiated from the electronic devices-based circuits when operating at high frequency for the DC-DC conversion process [1], [2]. The classifications of EMC are shown in Figure 1. EMI leads the way to the degradation of nearby devices performance by creating unwanted noise signals in terms of voltage and current. EMI limits as per CISPR-11 for semiconductor components-based circuits are shown in Table 1. EMI filters are designed for the better performance of electric vehicle (EV) converters as per CISPR 11 standards [3], [4]. With the help of active and passive components-based filters are used to select the required signal and to block the unwanted noise which is generated from the conducted EMI source [5]-[9]. Due to external components, the weight and cost have been considered as a drawback. To overcome the drawback of filters, shielding techniques have been promoted. The shielding method is about to cover the entire device or circuit with an enclosure-type metal box to stop the connection with the outside environment for the spreading of EMI noise.

Through input ports, display, wires, and output ports the leakage of EMI is possible. Soft switching technique has been procured instead of hard switching to reduce the high switching loss that occurred due to the large dv/dt, di/dt during switching on and off for high frequency on the output of EV converters as shown in Figure 2. The implementation of the soft switching approach needs a greater number of components and it makes the circuit operation complex [10]. After the filter and shielding approach randomization technique comes into the picture. In this technique, with the help of gate pulse modulation like increasing or decreasing the width of pulse,the peak value of the spectrum noise is spread over the entire cycle instead of a sudden increase and decrease. This way the generated EMI has been suppressed.
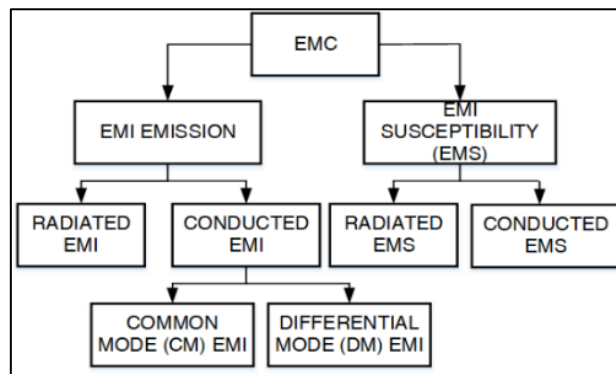

Figure 1. Classifications of EMC [1]

Table 1. CISPR 11 EMI limits on semiconductor devices [4]

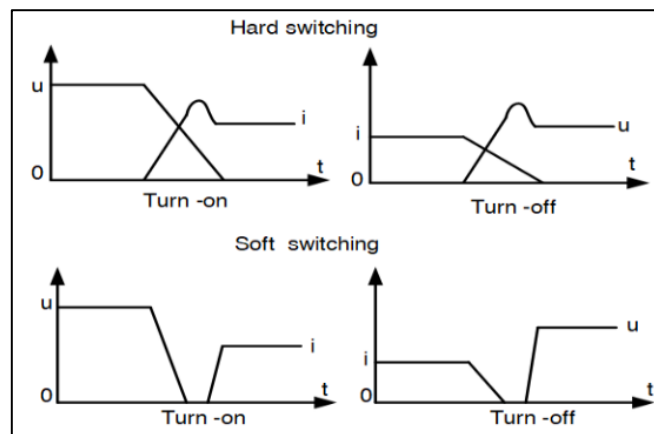| Frequency range (MHz)	Class A limits (dB µV)		Class B limits (dB µV)	
	Quasi-peak	Average	Quasi-peak	Average
0.15 to 0.50	79	66	66–50	56–46
0.50 to 5	79	66	56	46
5 to 30	73	60	60	50

Figure 2. MOSFET switching process

But generating a random pulse module makes the circuit complicated. Chaotic pulse width modulation technique is derived from random pulse modulation and the DC-DC converters are operated in chaotic mode by incorporating an external circuit that is used to generate chaotic carrier signal [11]-[13]. Analog and digital approaches are the two types of approaches used to generate chaotic carrier waves. The digital approach is mostly used in power converters due to its accuracy, frequency, and amplitude values can be reprogrammable with the help of digital programmable devices. Implementing this approach, the spike of the output voltage has been flattened throughout the total time period and maintaining the total energy constantly and EMI has been reduced. Chaotic pulse width modulation (PWM-based) EMI mitigation process gives better results compared with other EMI mitigation techniques.

In EV, DC-DC converters play an important role in the energy conversion process and energy storage. Most of the converters are operating at the high-frequency range to increase the gain based on the duty cycle as shown in Table 2 and the respected chart is also shown in Figure 3. Hence, EMI has been generated. In this analysis, the digital chaotic (DCPWM) technique is applied on single switch MOSFET based high gain converters like elementary positive output super lift Luo (EPOSLL), two-stage cascaded boost (TSCB), ultra-lift Luo (ULL), the respected EMI mitigation values are compared with each other, and the performance of that converters is also discussed. Single switch MOSFET-based converters reduce the cost and complexity of the hardware embedding process. In addition, researchers working in the above converters for EV application or some other applications may concentrate on CPWM based EMI mitigation process to eliminate the nearby devices malfunction due to EMI noises. The present work is systemized as follows, section 2 discusses the study of EPOSLL, TSCB, and ULL converter working and its switching characteristics, section 3 deals with digital chaotic PWM techniques and their implementation using an field-programmable gate array (FPGA) controller. The proposed EMI mitigation method on EPOSLL, TSCB, and ULL converters are presented in section 4, simulation and results are discussed in section 5, section 6 is about hardware setup and its working, concluded this work in section 7.

Table 2. Converters gain for different duty cycle

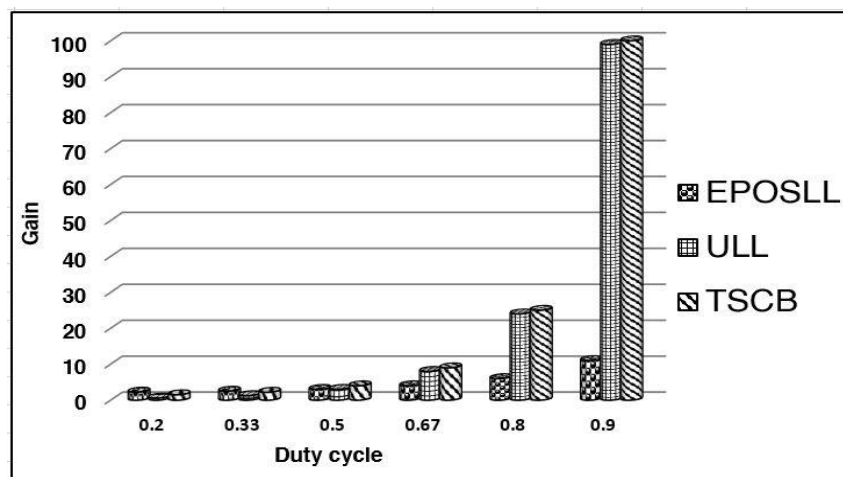| K	0.2	0.33	0.5	0.67	0.8	0.9
EPOSLL	2.25	2.5	3	4	6	11
ULL	0.56	1.25	3	8	24	99
TSCB	1.5	2.2	4	9	25	100

Figure 3. Comparison chart from Table 2

2. SINGLE SWITCH MOSFET BASED BOOST CONVERTERS: EPOSLL, TSCB, AND ULL

In EV applications energy conversion is an important area to store as well as to drive the load. Mostly, solid-state DC-DC converters are used for the above-said process with a high gain voltage ratio. The following section explains the various DC-DC converters working and their switching waveforms. Topology comparisons of EPOSLL, TSCB, and ULL are mentioned in Table 3 [14].

2.1. Elementary positive output super lift Luo converter

The EPOSLL converter is derived from the Luo converter, which is working based upon the concept of voltage lifting technique [15]. The input is boosted by three times based upon the duty cycle. By increasing the duty cycle ratio, the gain is also increasing. The elementary positive output super-lift Luo converter circuit is consisting of DC supply voltage V_{in}, 2n capacitors (C_1 and C_2), n inductor L_1, one power switch (n-channel MOSFET) S, (3n-1) diodes (D_1, D_2), and load resistance R. The circuit operation of the EPOSLL converter and its switching waveforms has explained in the following two conditions as shown in Figure 4:
− During ON condition: switch S is in ON state, diode D_1 is conducting and D_2 is not conducting, capacitor C_1 is charged through input voltage V_{in} and the inductor current I_{L1} also increases with the

help of V_{in}. So, the inductor and capacitor voltages are circulating in the loop and produces the capacitor voltage V_{C1} is ($V_{in}+V_L-V_o$). The voltage is build-up within the specified path.

- During OFF condition: switch S is in OFF state, diode D_1 is not conducting and D_2 is conducting, and the inductor current decreases with voltage $V_o–2V_{in}$. So, the total current is flowing through the load. Based upon the duty cycle the gain may increase. The energy accumulated in the inductor L_1 and capacitor C_1 is moving towards the capacitor C_2 as well as to the load R.

Table 3. Topology comparison of EPOSLL, TSCB, and ULL converters

Converter	Circuit diagram	Components	Voltage output (V)	Applications
EPOSLL		Switch=1 Diode=2 Capacitor=2 Inductor=1	$V_o = \dfrac{2-k}{1-k} V_{in}$	– LED lighting. – EV. – Loco – motives. – Battery charging. – Power supplies.
TSCB		Switch=1 Diode=3 Capacitor=2 Inductor=2	$V_o = \left(\dfrac{1}{1-k}\right)^2 V_{in}$	– Computer applications. – Satellite applications. – Mobile charging. – EV. – Voltage doubling application.
ULL		Switch=1 Diode=3 Capacitor=2 Inductor=2	$V_o = \dfrac{k(2-k)}{(1-k)^2} V_{in}$	– High gain application. – Fast charging. – Vehicle to grid. – EV. – Communication applications.

2.2. Two-stage cascaded boost DC-DC converter

The two-stage cascaded boost converter circuit consists of three diodes (D_1, D_2 and D_3) two capacitors (C_1 and C_2), two inductors (L_1 and L_2) and one MOSFET switch(S) as shown in Figure 5. The boost operation is carried out in two ways, one is through L_1, D_1, and S and the other way is through C_1, L_2, and S, in both ways the capacitor C_2 is charged and delivers the boosted voltage across the load [16], [17].

- Mode 1: switch S is in ON state, diode D_1, D_2, and D_3 is in conducting mode, the current flowing through the inductor is increased gradually. Current in diode D_2, D_3 starts to decrease until S is off.
- Mode 2: switch S and diode D_1 is ON state, D_2 and D_3 is OFF. The energy level in inductors L_1 and L_2 is increased and the load is energized through the capacitor C_2.
- Mode 3: switch and diodes are in ON state. So, capacitor C_2 has been charged from the reverse current.
- Mode 4: switch S and D_1 is in OFF state and D_2, D_3 is in ON state. The charged energy is given to the load through D_2 and D_3. The inductor current i_{L1} and i_{L2} decreases gradually. The reverse current is stored in the capacitor C_1 until switch S is ON and the process continues.

2.3. Ultra-lift Luo converter

The circuit diagram includes a MOSFET switch S, capacitors (C_1, C_2), diodes (D_1, D_2, D_3), and inductors (L_1, L_2) respectively as shown in Figure 6. The parameters of the ULL converter are the input

voltage V_1, input current I_1, output voltage V_2, output current I_2, duty cycle k, and the switching frequency fsw. Duty cycle kT and (1-k)T during switch-ON and switch-OFF respectively [18]:

- Continuous conduction mode (CCM): in this mode, the switch is ON, the inductor current iL_1 increases with the slope (V_1/L_1) and decreases with slope $-(V_3/L)$. In this condition, the values are equal either increasing or decreasing throughout the time period T. Similarly for the inductor current iL_2, the slope is increases $(V_1-V_3)/L_2$ and decreases of $-(V_3-V_2)/L_2$ during switch-ON and switch-OFF simultaneously.
- Discontinuous conduction mode (DCM): during switch ON and OFF, the inductor current iL_1 increases with the slope of V_1/L_1 and decreases with the slope of $-(V_3/L_1)$. The inductor current iL_1 is decreased to zero when the switch is turned ON during the next time. Similarly, inductor current iL_2 increases by $(V_1-V_3)/L_2$ and decreases by $-(V_3-V_2)/L_2$ during the switching ON and OFF process.
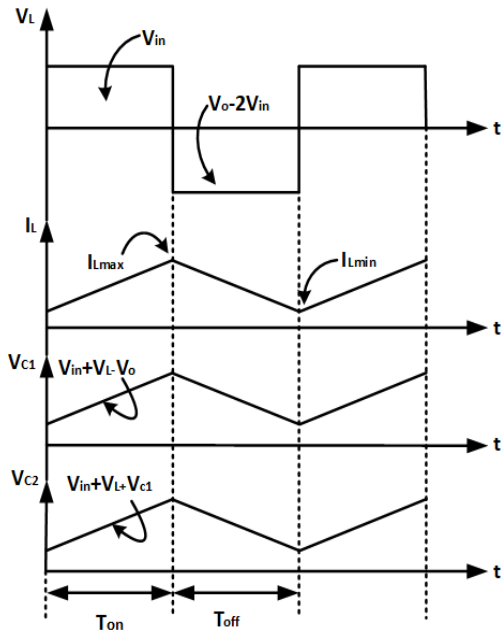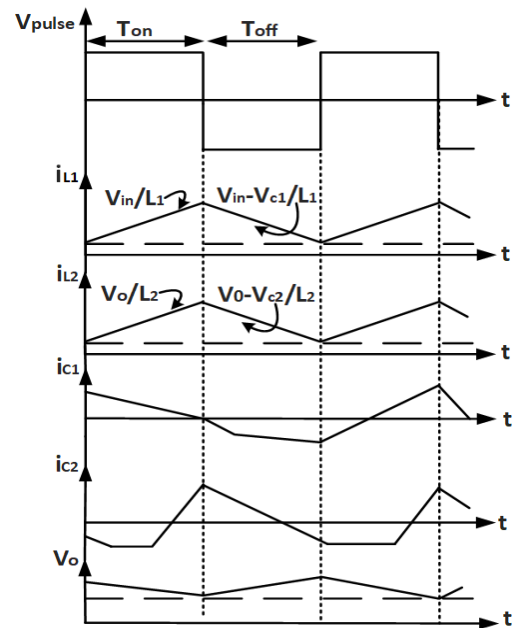

Figure 4. EPOSLL switching waveforms
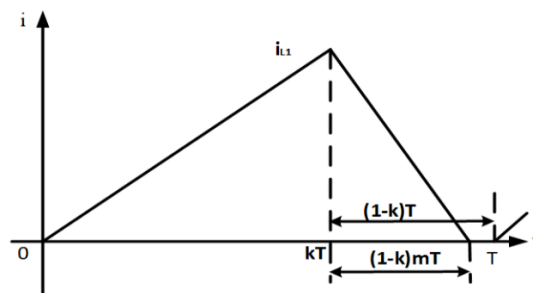

Figure 5. TSCB converter switching waveforms

Figure 6. Inductor current i_{L1} waveform in ULL converter

3. DIGITAL CHAOTIC PULSE WIDTH MODULATION TECHNIQUE

Spectrum spreading modulation is named chaotic modulation. By adding a disturbance to the PWM modulation controller with the help of an external peripheral device, a chaotic carrier wave signal has been generated. Gate terminals are triggered by chaotic pulses, the harmonics and energy peaks are flattened through the entire time period as shown in Figure 7 and the energy level is constantly maintained. The instant peak value of Fc is tuned to [Fc−Δfc, Fc+Δfc] and the peak of the harmonics and EMI has been reduced [19]-[21].

3.1. Randomized carrier frequency modulation with fixed duty

By varying the pulse position or width concerning carrier frequency, chaotic pulses are generated. In the PWM technique normal carried wave is implemented to generate PWM pulses. An abnormal carrier wave

is used to generate chaotic pulses with a fixed duty cycle. The switching frequency has been maintained at $\pm 1/3^{rd}$ of the central switching frequency 200 kHz i.e. (144 kHz to 266 kHz) for the better EMI mitigation process. The linear feedback shift register has been utilized to achieve the above said RCFMFD [22]. From Figure 8. T_k represents k^{th} cycle duration, α_k is the ON state interval, ε_k is the delay time, duty ratio (d_k) is given by α_k/T_k, k^{th} cycle starting time is ξ_k and the switching function is q(t). As mentioned in Figure 8, if the kth switching cycle starts at time ξ_k is given by (1),
Here,

$$\xi_k = \sum_{i=0}^{K-1} T_i \ \ k = 1,2,\dots\dots T_o = 0 \tag{1}$$

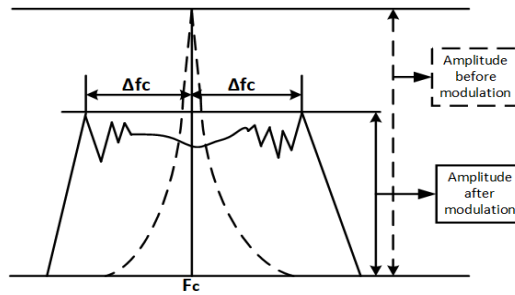where u_k $(t-\xi_k)$: single-pulse waveform.

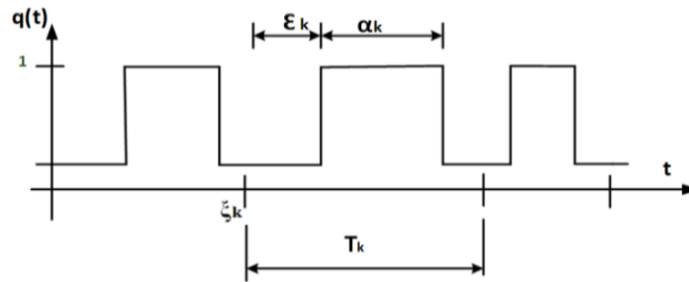

Figure 7. Basic concept of DCPWM

Figure 8. Randomization parameters in switching signal

The switching function is given in (2):

$$q(t) = \sum_{i=-\infty}^{\infty} T_i \ u_k \ (t - \xi_k) \tag{2}$$

where $u_k(t)$ value is given by (3):

$$u_k(t) = \begin{cases} 1, for \ \xi_k \ \le t \ \le \ \xi_k + \alpha_k \\ 0, otherwise \end{cases} \tag{3}$$

3.2. Pseudo-random number generation using FPGA based linear feedback shift register

A pseudo-random number has been generated for producing switching pulse with the help of linear feedback shift register (LFSR) which is embedded in the FPGA controller as shown in Figure 9. Combination of shift registers and XOR gates embedded in LFSR to do the linear operation for adjusting the clock pulse edges. 2n-1 random numbers are produced by LFSR, where n indicates flip flop counting and the positions of bits are seed and taps. The outputs are 0's and 1's and the LFSR is triggered continuously until the program execution ends by the programmer [23].

3.3. Module for generating DCPWM using FPGA controller

The following module explain the generation of DCPWM for 200 kHz switching frequency and the corresponding flow chart also shown in Figure 10. Xilinx design suit 14.7 software has been used to implement the generation of digital chaotic pulses. Verilog language is used to write coding for digital chaotic pulses generation through FPGA controller.
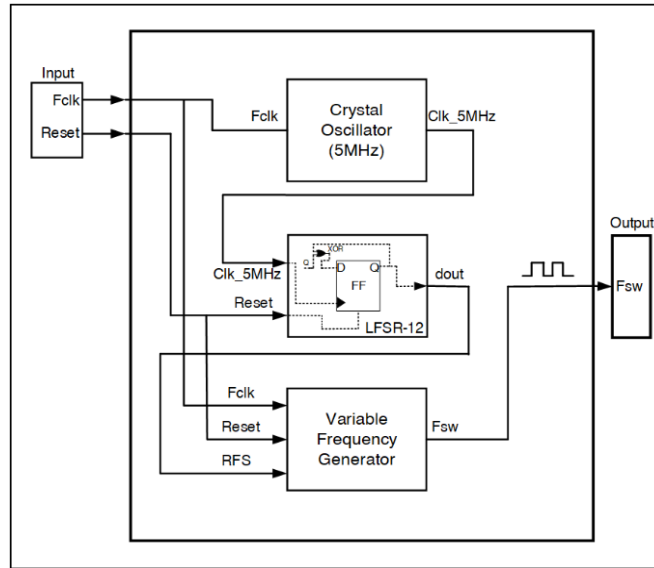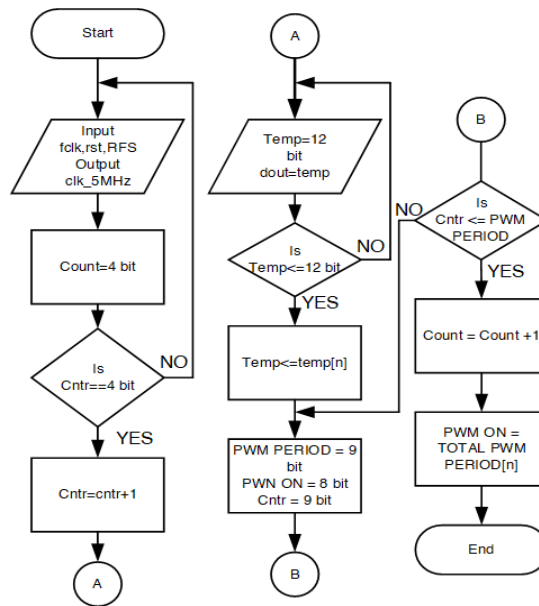
Figure 9. FPGA module for chaotic pulse generation

Figure 10. Flowchart for chaotic pulse generation

3.3.1. Main module
Step 1: Configure the inputs (fclk, rst, RFS) and output Fsw.
Step 2: Set RFS bit.
Step 3: Request sub-module from the output of clock frequency.
Step 4: Request LFSR module inputs and outputs to the main module.
Step 5: Request Variable_frequency generation outputs clk, dout, RFS, Fsw and rst.

3.3.2. Clock frequency generation (5 MHz)
Step 1: Configure the clock inputs fclk and output clk_5M.
Step 2: Set bits for clk=1 bit and counter cntr=4-bit.
Step 3: Set always positive edge pulses.
Step 4: Compare cntr with 4-bit values and clk_5M.
Step 5: increment the counter cntr=cntr+1.

Step 6: Stop module.

3.3.3. Feeding data to LFSR module
Step 1: Set input clk, rst and output dout.
Step 2: Set flip flops for 12-bit temp. register and give the 12-bit data value like 0's and 1's.
Step 3: Configure temp. is greater than or equal to 12- bit.
Step 4: Feed the temp 12-bit data.
Step 5: Stop module.

3.3.4. Variable frequency generation
Step 1: Initialize the inputs fclk, rst, RFS and output Fsw.
Step 2: Set PWM PERIOD=9-bit, PWM ON=8-bit and counter=9-bit.
Step 3: Set max. frequency value TN=8-bit data.
Step 4: Set always at positive edge of clock.
Step 5: Configure the load by enabling the counter.
Step 6: RFS is <=8-bit data, PWMON=PWMPERIOD value down to 8-bit values.
Step 7: Stop module.

4. PROPOSED EMI MITIGATION TECHNIQUE ON EPOSLL, TSCB, AND ULL CONVERTERS
The following division gives a picture of the EMI suppression method in periodic and digital chaotic on the various converter. Through line impedance stabilization network (LISN) the input voltage has been given to the converters from the DC source. Periodic and chaotic pulses are given to the MOSFET gate terminals of the above-mentioned converters and the desired output voltage has been calculated with EMI, in the form of power spectrum density through various input voltage levels respectively [24].

4.1. Line impedance stabilization network
LISN circuit diagram and its specifications are shown in Figure 11 and Table 4. LISN has been generally used to block the conducted EMI from an outside source through various components like wires, sockets, and display panels. The common-mode and differential-mode noises are measured through various outcomes from the vector sum of line-ground (L-G) and neutral-ground (N-G) voltages.
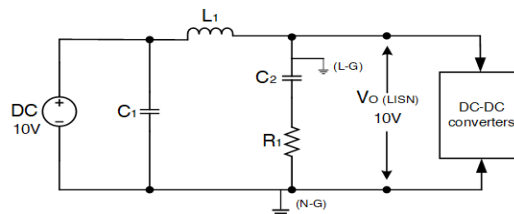

Figure 11. LISN circuit diagram

Table 4. LISN specifications

Parameter	Symbol	Value
Input voltage (V)	V_{in}	10
Output voltage (V)	$V_{o\ (LISN)}$	10
Inductor (µH)	L_1	5
Capacitor (µF)	C_1	10
Capacitor (nF)	C_2	100
Resistor (Ω)	R_1	50

4.2. Digital chaotic PWM based EMI mitigation technique
The proposed digital chaotic EMI mitigation process is as follows. The input of 10 V is given to the converters from a DC power supply (RPS) through LISN are shown in Figures 12(a)-(c). By using the voltage boosting technique, the input voltage is boosted to the desired voltage based upon the gain of the converters. To attain the gain quickly, the switching frequency has been increased and spikes are produced at the instant, in that way EMI has been generated in that circuit. The chaotic pulses have been generated with help of FPGA coding and those pulses are given to the MOSFET switch gate terminal and the generated EMI has been mitigated. The following section explains the EMI mitigation process in periodic and chaotic approach in simulation using MATLAB 2020a and hardware prototype model [25], [26].
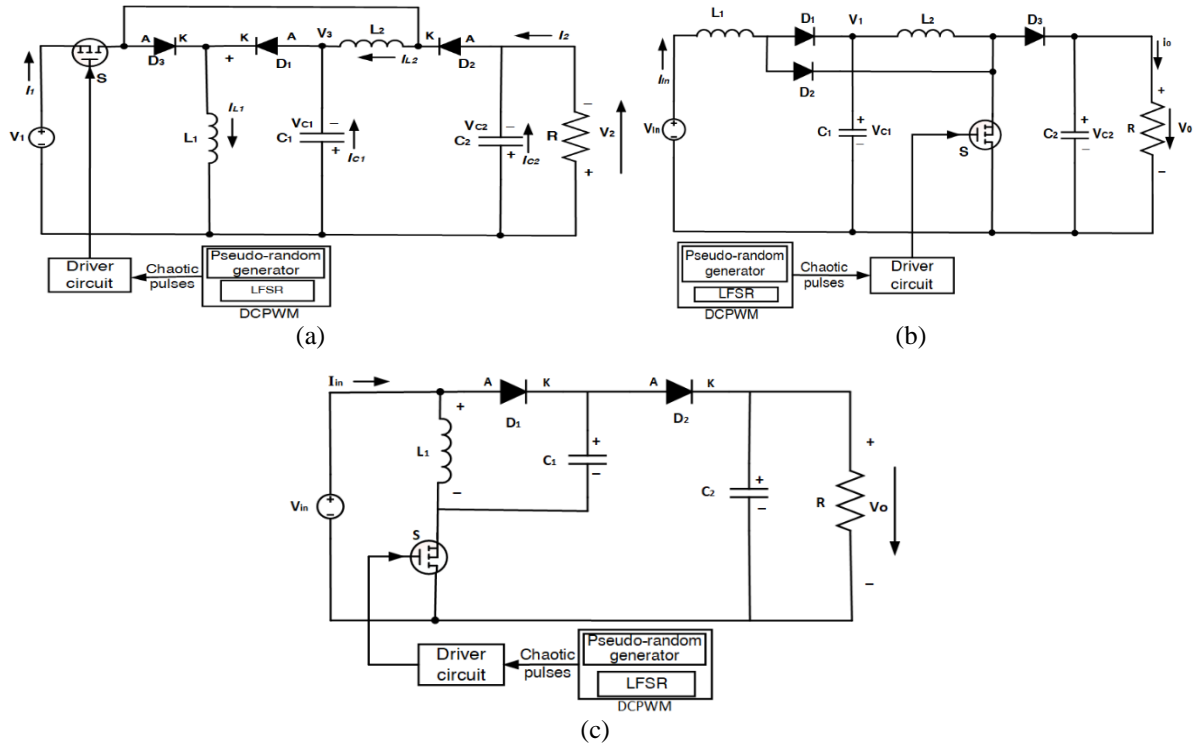
Figure 12. Schematic of the proposed DCPWM EMI mitigation technique (a) EPOSLL, (b) TSCB, and (c) ULL

5.   SIMULATION RESULTS AND DISCUSSION
The circuit diagrams of the above-said converters are simulated with the help of MATLAB 2020a. The parameters are mentioned in Table 5 for the respected converters. The following section explains the simulation comparison between the periodic PWM approach and DCPWM approach on EPOSLL, TSCB, and ULL converters.

Table 5. Specifications of EPOSLL, ULL, and TSCB converters

Parameters Name	Symbol	Values		
		EPOSLL	ULL	TSCB
Input voltage (V)	V_{in}	10	10	10
Output voltage (V)	V_o	30	80	40
Inductor (µH)	L_1	-	100	100
Inductor (µH)	L_2	200	200	200
Capacitors (µF)	C_1, C_2	10	10	10
Switching frequency (kHz)	F_s	200	200	200
Load resistance (Ω)	R	50	50	50
Output power (W)	P_o	40	80	40
Duty cycle	k	0.5	0.67	0.5

5.1. Periodic pulse width modulation technique
The simulated waveforms are shown in Figures 13(a)-(c), the input voltages are varied from 10 V to 12V and the duty cycle varies from 0.5 to 0.67. The periodic pulses are generated by conventional PWM technique with MATLAB 2020a simulink model. The respected inputs and the various outputs of EPOSLL, TSCB and ULL converters are tabulated in Tables 6-8.

Table 6. Simulation results of EPOSLL converter using periodic PWM technique

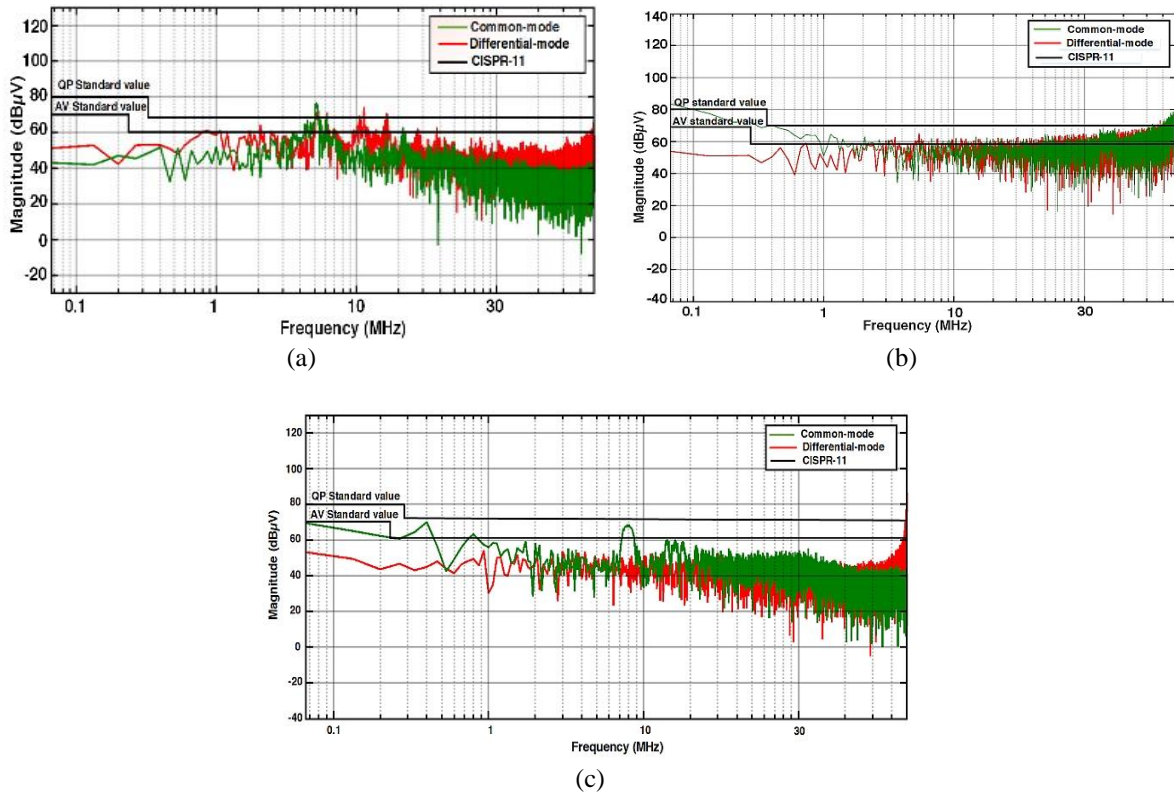| Input voltage (V)	Output voltage (V)	Output current (A)	PSD (dBV)	CM noise (dBµV)	DM noise (dBµV)
2	6	0.3	-10	80	40
4	12	0.5	-20	75	30
6	18	0.9	-40	60	25
8	24	1.1	-50	50	20
10	30	1.3	-60	40	15

(a)

(b)

(c)

Figure 13. CM/DM noise in periodic PWM technique (a) EPOSLL, (b) TSCB, and (c) ULL

Table 7. Simulation results of TSCB converter using periodic PWM technique

Input voltage (V)	Output voltage (V)	Output current (A)	PSD (dBV)	CM noise (dBµV)	DM noise (dBµV)
2	8	0.2	30	40	25
4	16	0.5	-5	45	30
6	24	0.7	-8	50	40
8	32	0.9	-10	60	50
10	40	1.1	-13	70	60

Table 8. Simulation results of ULL converter using periodic PWM technique

Input voltage (V)	Output voltage (V)	Output current (A)	PSD (dBV)	CM noise (dBµV)	DM noise (dBµV)
2	16	0.2	-5	80	40
4	32	0.4	-18	70	60
6	48	0.6	-20	50	70
8	64	0.8	-30	45	80
10	80	1.2	-42	30	90

5.2. Digital chaotic pulse width modulation technique

The chaotic pulses are generated by chaotic mapping technique with MATLAB 2020a Simulink model and applied to the above discussed converters. The input voltages are varied from 10 V-12 V and the duty cycle varies from 0.5 to 0.67 like periodic PWM technique as shown in Figures 14(a)-(c). The various parameter waveforms are captured and shown in Tables 9-11.

Table 9. Simulation results of EPOSLL converter using DCPWM technique

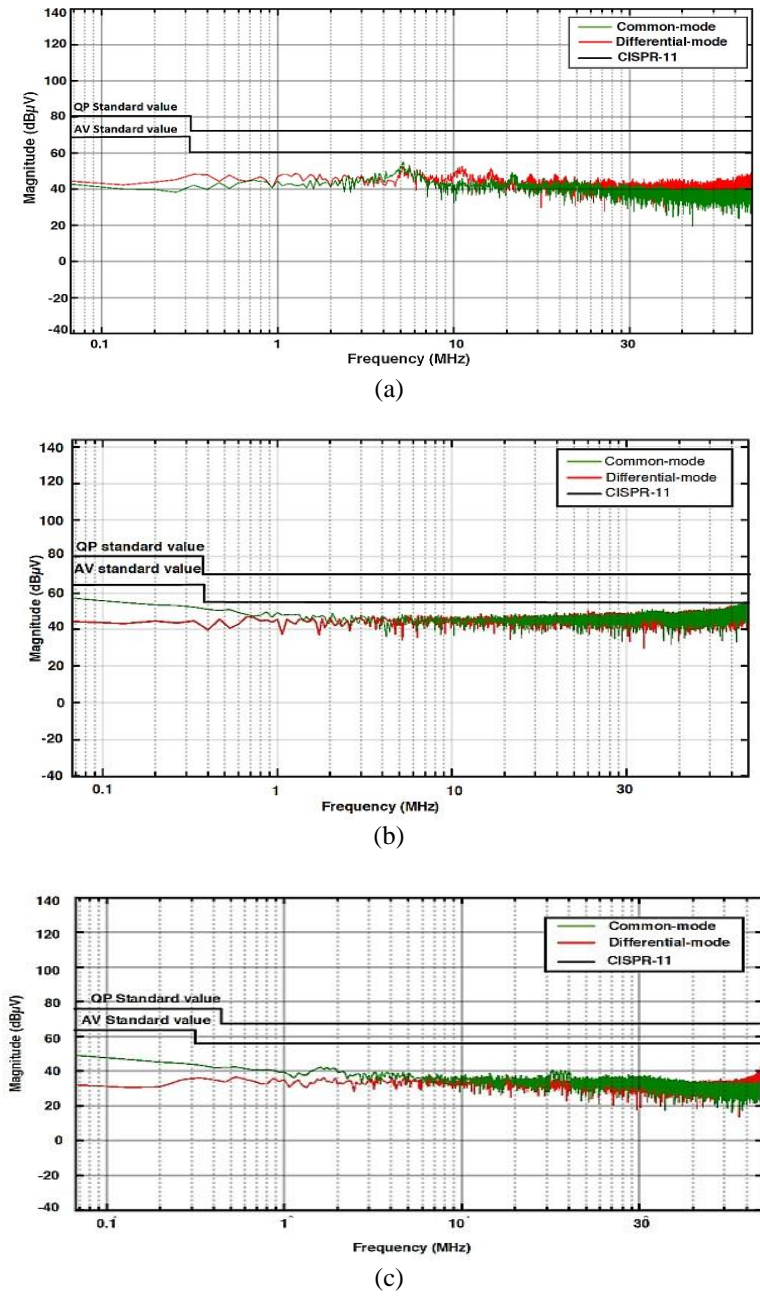| Input voltage (V)	Output voltage (V)	Output current (A)	PSD (dBV)	CM noise (dBµV)	DM noise (dBµV)
2	6	0.3	-10	60	60
4	12	0.5	-20	50	55
6	18	0.9	-40	40	50
8	24	1.1	-50	30	45
10	30	1.3	-70	25	40

(a)

(b)

(c)

Figure 14. CM/DM noise in DCPWM technique (a) EPOSLL, (b) TSCB, and (c) ULL

Table 10. Simulation results of TSCB converter using DCPWM technique

Input voltage (V)	Output voltage (V)	Output current (A)	PSD (dBV)	CM noise (dBµV)	DM noise (dBµV)
2	8	0.2	25	62	25
4	16	0.5	10	58	28
6	24	0.7	-10	55	35
8	32	0.9	-15	52	40
10	40	1	-20	60	48

Table 11. Simulation results of ULL converter using DCPWM technique

Input voltage (V)	Output voltage (V)	Output current (A)	PSD (dBV)	CM noise (dBµV)	DM noise (dBµV)
2	16	0.2	-2	45	20
4	32	0.4	-38	40	25
6	48	0.6	-40	35	30
8	64	0.8	-42	20	35
10	80	1.2	-44	10	40

5.3. Simulation comparison: periodic PWM Vs DCPWM techniques

During the fast-switching process, the frequency range of 150 kHz–200 kHz is applied to the gate terminals of MOSFET to increase the gain, due to that transient occurs in output voltage and output current at the initial stage, in that way EMI has been generated. In that comparison table, at the initial stage, the peak values of various parameters are shown in the periodic and chaotic PWM approach. In the DCPWM technique, the peak value has been spread over the time periodically, through this concept peak value at the initial stage has been minimized compared with the periodic PWM technique. In power spectrum density (PSD) waveform comparison, the density of power spectrum during periodic PWM and DCPWM are calculated. CM noise and DM noise were also compared for periodic PWM and DCPWM techniques. DCPWM technique generated less conducted EMI noise within CISPR 11 limits.

6. HARDWARE IMPLEMENTATION

From simulation design, the hardware prototype model has been embedded with commercially available components, apart from circuit FPGA spartan 3E controller board has been used to generate periodic and chaotic pulses through coding in Xilinx design suit 14.7 software, and the generated pulses are given to the gate terminal through TLP 350 gate driver circuit.

6.1. Periodic PWM and DCPWM approaches

In this approach, periodic and digital chaotic pulses are generated by using an FPGA board and applied to the gate terminals, and the respected FFT of output voltage waveforms are captured with the help of mixed signal oscilloscope (MSO) for EMI analysis as shown in Figures 15(a)-(c) and Figures 16(a)-(c).
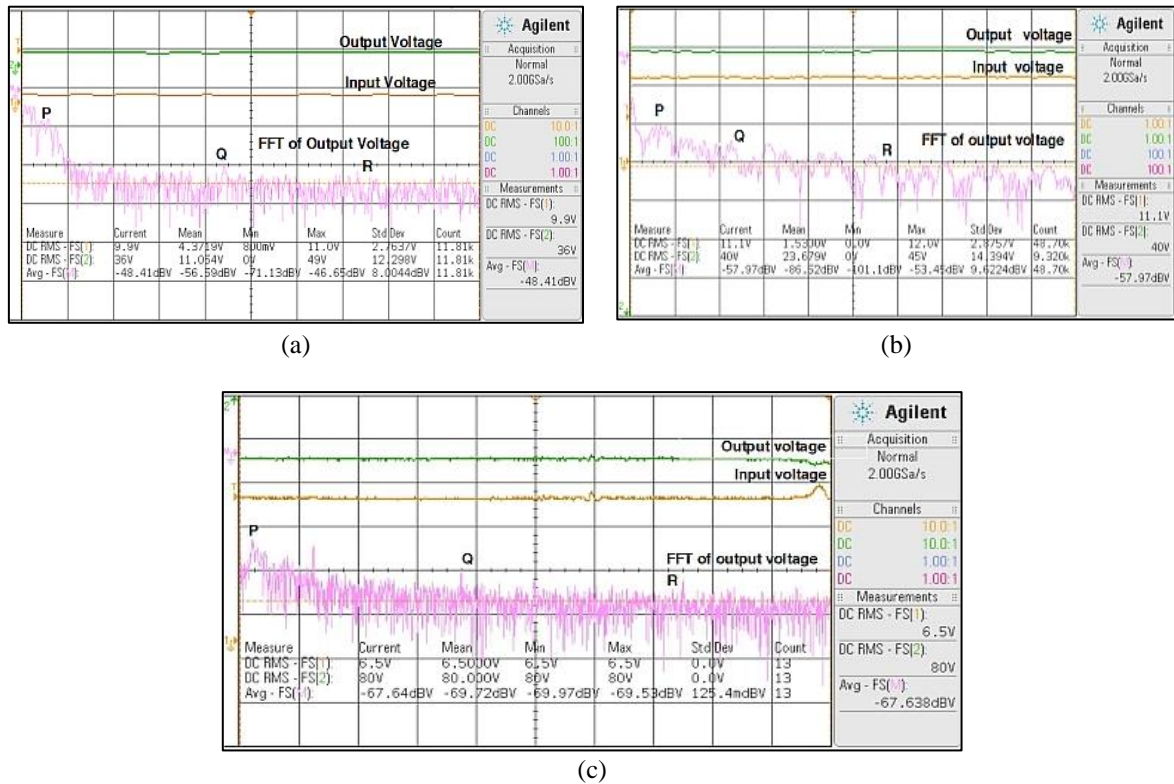

(a)   (b)

(c)

Figure 15. FFT of output voltage in periodic PWM technique (a) EPOSLL, (b) TSCB, and (c) ULL converters

6.2. Hardware comparison statement

From Figures 15(a)-(c) and Figures 16(a)-(c), the various peak levels of FFT output voltage magnitude have been taken as the parameter for analysis purposes. The total hardware setup is shown in Figure 17. There is a variation of 4 dBV to 15 dBV which is equal to 3 V to 10 V (RMS) of conducted EMI has been suppressed in DCPWM technique compared with periodic PWM technique as shown in Table 12 and Figure 18.
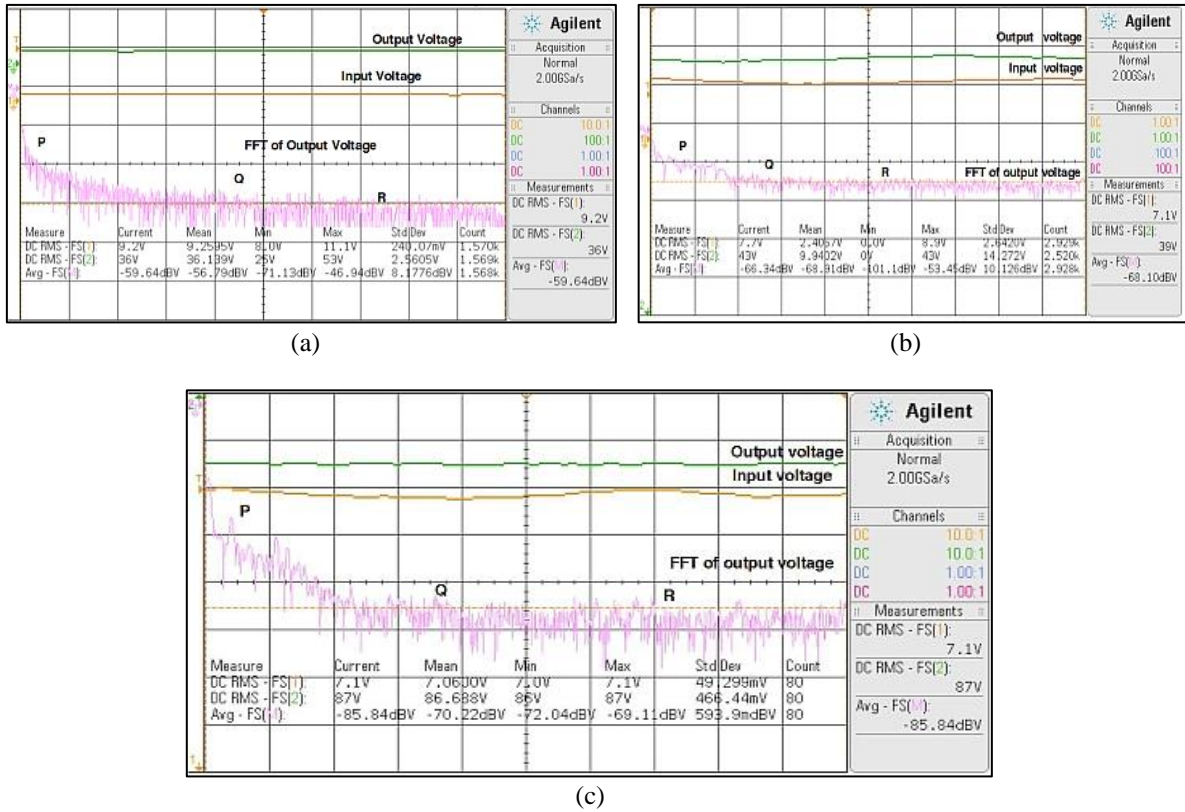
(a)

(b)

(c)

Figure 16. FFT of output voltage in DCPWM technique (a) EPOSLL, (b) TSCB, and (c) ULL converters

Table 12. FFT of output voltage from Figures 15 and 16

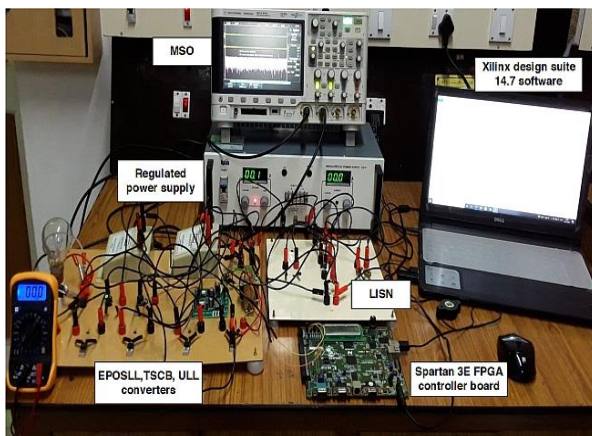|	Magnitude levels (dBV)					
	P		Q		R	
	Periodic PWM	DCPWM	Periodic PWM	DCPWM	Periodic PWM	DCPWM
EPOSLL	-46.65	-49.94	-48.41	-56.64	-56.59	-59.64
TSCB	-53.0	-57.24	-57.97	-61.09	-61.0	-68.10
ULL	-63.74	-69.11	-67.63	-72.04	-69.97	-85.84

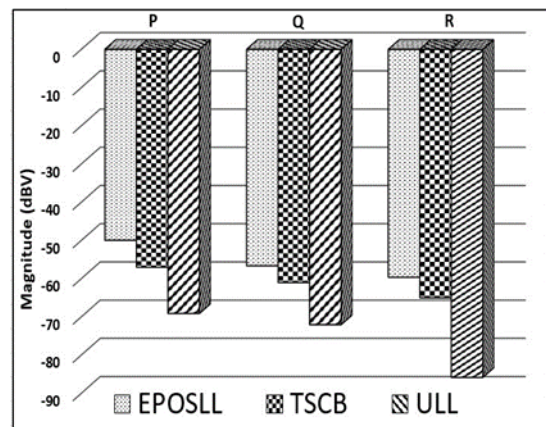Figure 17. Hardware setup for EMI testing

Figure 18. Spectral magnitude comparison

7. CONCLUSION

In this article, the EPOSLL, TSCB, and ULL high gain converter hardware prototype models have been built and tested with designed input and output values with a duty ratio of 0.5 to 0.67 for a power rating

of 40 W to 80 W. Calculation of conducted EMI noise has been done by measuring the peak value of PSD in simulation for both cases like periodic and digital chaotic PWM methods at randomly selected peak points. The FFT of the output voltages was also measured randomly throughout the conducted hardware experiment. From hardware results, 4 dBV (3 V) to 15 dBV (10 V) of conducted EMI noise has been reduced in the DCPWM technique on the above-tested converters. From the observations, it can be concluded that the selection of the ULL converter gives better results in simulation and hardware for the DCPWM based EMI mitigation process and satisfies EMC standards than EPOSLL and TSCB converters for EV applications.

REFERENCES

[1]   S. Natarajan, T. S. Babu, K. Balasubramanian, U. Subramaniam, and D. J. Almakhles, "A State-of-the-Art Review on Conducted Electromagnetic Interference in Non-Isolated DC to DC Converters," in *IEEE Access*, vol. 8, pp. 2564-2577, 2020, doi: 10.1109/ACCESS.2019.2961954.

[2]   T. Baba, N. A. C. Mustapha, and N. F. Hasbullah, "A review on techniques and modelling methodologies used for checking electromagnetic interference in integrated circuits," *Indonesian Journal of Electrical Engineering and Computer Science,* vol. 25, no. 2, pp.796-804, Feb. 2022, doi: 10.11591/ijeecs.v25.i2.pp796-804.

[3]   H. Li, Z. Li, B. Zhang, W. K. S. Tang, and W. A. Halang, "Suppressing electromagnetic interference in direct current converters," in *IEEE Circuits and Systems Magazine*, vol. 9, no. 4, pp. 10-28, 2009, doi: 10.1109/MCAS.2009.934705.

[4]   ''International Electrotechnical Commission,'' IEC everywhere for a safer and more efficient world, 2008. [Online]. Available: https://www.iec.ch.

[5]   G. A. Latheef, S. Karunakaran, and K. Sridhar, "Tuned band reject powerline EMI filter," *1995 International Conference on Electromagnetic Interference and Compatibility (INCEMIC)*, 1995, pp. 436-439, doi: 10.1109/ICEMIC.1995.501623.

[6]   A. Mariscotti, L. Sandrolini, and G. Pasini, "Variability Caused by Setup and Operating Conditions for Conducted EMI of Switched Mode Power Supplies Over the 2–1000 kHz Interval," in *IEEE Transactions on Instrumentation and Measurement*, vol. 71, pp. 1-9, 2022, Art no. 1501009, doi: 10.1109/TIM.2022.3162291.

[7]   Y. Zhou, W. Chen, and X. Yang, "Investigation of Cascade Connection Method to Improve the Insertion Loss of DM Active EMI Filters," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 1, pp. 1084-1094, Feb. 2022, doi: 10.1109/JESTPE.2021.3112576.

[8]   B. Narayanasamy and F. Luo, "A Survey of Active EMI Filters for Conducted EMI Noise Reduction in Power Electronic Converters," in *IEEE Transactions on Electromagnetic Compatibility*, vol. 61, no. 6, pp. 2040-2049, Dec. 2019, doi: 10.1109/TEMC.2019.2953055.

[9]   Z. Shen, M. Chen, H. Wang, X. Wang, and F. Blaabjerg, "EMI Filter Robustness in Three-Level Active Neutral-Point-Clamped Inverter," in *IEEE Transactions on Power Electronics*, vol. 37, no. 4, pp. 4641-4657, Apr. 2022, doi: 10.1109/TPEL.2021.3124282.

[10]   X. -F. Cheng, C. Liu, D. Wang, and Y. Zhang, "State-of-the-Art Review on Soft-Switching Technologies for Non-Isolated DC-DC Converters," in *IEEE Access*, vol. 9, pp. 119235-119249, 2021, doi: 10.1109/ACCESS.2021.3107861.

[11]   H. Li, Y. Ding, C. Zhang, Z. Yang, Z. Yang, and B. Zhang, "A Compact EMI Filter Design by Reducing the Common-Mode Inductance With Chaotic PWM Technique," in *IEEE Transactions on Power Electronics*, vol. 37, no. 1, pp. 473-484, Jan. 2022, doi: 10.1109/TPEL.2021.3100360.

[12]   H. Li, Z. Li, B. Zhang, F. Wang, N. Tan, and W. A. Halang, "Design of Analogue Chaotic PWM for EMI Suppression," in *IEEE Transactions on Electromagnetic Compatibility*, vol. 52, no. 4, pp. 1001-1007, Nov. 2010, doi: 10.1109/TEMC.2010.2071878.

[13]   J. Villa, A. Domínguez, L. A. Barragán, J. I. Artigas, J. Español, and D. Navarro, "Conductance Control for Electromagnetic-Compatible Induction Heating Appliances," in *IEEE Transactions on Power Electronics*, vol. 37, no. 3, pp. 2909-2920, Mar. 2022, doi: 10.1109/TPEL.2021.3118319.

[14]   F. L. Luo and H. Ye, *Advanced DC/DC converters 2nd edition*, CRC press, New York, 2017.

[15]   K. R. Kumar and S. Jeevananthan, "PI control for positive output elementary super lift luo converter," *International Journal of Electrical, Computer, Energetic, Electronic and Communication Engineering,* vol. 4, no. 3, pp. 544-549, Jan. 2010.

[16]   K. Sayed, M. Abdel-Salam, A. Ahmed, and M. Ahmed, "New high voltage gain dual-boost DC-DC converter for photovoltaic power systems," *Electric Power Components and Systems*, vol. 40, no. 7, pp. 711–728, Apr. 2012, doi: 10.1080/15325008.2012.658596.

[17]   S. H. Chincholkar, W. Jiang, and C. -Y. Chan, "A Normalized Output Error-Based Sliding-Mode Controller for the DC–DC Cascade Boost Converter," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 1, pp. 92-96, Jan. 2020, doi: 10.1109/TCSII.2019.2899388.

[18]   R Shenbagalakshmi, S Vijayalakshmi and K Geetha, "Design and analysis of discrete PID controller for Luo converter," *International Journal of Power Electronics*, vol. 11, no. 3, pp.283–298, Mar. 2020, doi: 10.1504/IJPELEC.2020.10027748.

[19]   G. M. Dousoky, M. Shoyama, and T. Ninomiya, "FPGA-Based Spread-Spectrum Schemes for Conducted-Noise Mitigation in DC–DC Power Converters: Design, Implementation, and Experimental Investigation," in *IEEE Transactions on Industrial Electronics*, vol. 58, no. 2, pp. 429-435, Feb. 2011, doi: 10.1109/TIE.2010.2049708.

[20]   S Natarajan and R. Natarajan, "An FPGA chaos-based PWM technique combined with simple passive filter for effective EMI spectral peak reduction in DC-DC converter," *Advances in Power Electronics*, vol. 2014, pp. 1-11, Feb. 2014, doi: 10.1155/2014/383089.

[21]   S. Natarajan, P. Padmavathi, J. R. Kalvakurthi, T. S. Babu, V. K. Ramachandaramurthy, and S. Padmanaban, "Conducted electromagnetic interference spectral peak mitigation in Luo-converter using FPGA-based chaotic PWM technique," *Electric Power Components and Systems, Taylor & Francis Group,* vol. 47, no. 9-10, pp. 838-848, Jul. 2019, doi: 10.1080/15325008.2019.1629510.

[22]   D. Shin, S. Jeong, Y. Baek, C. Park, G. Park, and J. Kim, "A Balanced Feedforward Current-Sense Current-Compensation Active EMI Filter for Common-Mode Noise Reduction," in *IEEE Transactions on Electromagnetic Compatibility*, vol. 62, no. 2, pp. 386-397, April 2020, doi: 10.1109/TEMC.2019.2906854.

[23]   F. A. Kharanaq, A. Emadi, and B. Bilgin, "Modeling of Conducted Emissions for EMI Analysis of Power Converters: State-of-the-Art Review," in *IEEE Access*, vol. 8, pp. 189313-189325, 2020, doi: 10.1109/ACCESS.2020.3031693.

[24]   N. Moonen, R. Vogt-Ardatjew, and F. Leferink, "Simulink-Based FPGA Control for EMI Investigations of Power Electronic Systems," in *IEEE Transactions on Electromagnetic Compatibility*, vol. 63, no. 4, pp. 1266-1273, Aug. 2021, doi: 10.1109/TEMC.2020.3042301.
[25]   T. L. Liao, P. Y. Wan, and J. -J. Yan, "Design and Synchronization of Chaos-Based True Random Number Generators and Its FPGA Implementation," in *IEEE Access*, vol. 10, pp. 8279-8286, 2022, doi: 10.1109/ACCESS.2022.3142536.
[26]   H. Bai, H. Luo, C. Liu, D. Paire, and F. Gao, "A Device-Level Transient Modeling Approach for the FPGA-Based Real-Time Simulation of Power Converters," in *IEEE Transactions on Power Electronics*, vol. 35, no. 2, pp. 1282-1292, Feb. 2020, doi: 10.1109/TPEL.2019.2918590.

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