A new approach to design Class C amplifier at nano scale with low power consumptions for mobile application

[1]Tripathi Arunendra Nath, [2]Tiwari Rajkumar, [3]Tiwari Monika

[1]Research scholar, [2]Prof. Department of Physics and electronics Dr ram Manohar Lohiya Awadh University Ayodhya Uttar Pradesh India. [3]Rajkiya Polytechnique college Gonda Uttar Pradesh India. [1]tripathiarun37@gmail.com, [2]rktiwari2323@gmail.com

Abstract- At present, saving energy is one of the important goals, keeping this in mind we present a new approach to design class c amplifier which works at very low power consumption in the range of micro watt and low noise in range nano watt and works in frequency range tera hertz 1.563THz to 6.930 THz with voltage gain 20dB. Present pair is combination of NMOS and PMOS in compound pair form and it is simulated on cadence virtuoso software at 180nm scale. It can be used in radio astronomy, satellite, communications.

Key words – Class C amplifier, Low noise, Low power Consumptions, NMOs and PMOS pair, Nano technology.

I. INTRODUCTION

In any transceiver power amplifier is always a last block for the transmission of wave. It amplifies an electrical signal to ample power level that secure a transmission signal to spread across some distance and received at the receiver end like mobile GSM application. Power amplifiers uses are different at different places which has so many applications.[1]

CMOS technology reduces fabrication cost: and therefor it is used in buildings of many IC systems. It is also Better than other available options when it comes at VLSI. However, CMOS having poor performance in radio frequency Circuits. CMOS has lousy current drive and large associated parasitic capacitance.[2] The suspense of integrated PA within CMOS stands up because of this technology have so many limitations that vastly limits the efficiency of power applications.[3] The primary difference among these PA classes is the passage of the radio frequency cycle for which the transistor conducts.[3] In class A PA, transistor conductus for the entire radio frequency cycle, while in class B amplifier PA it is on state for all half cycle, and is less than half of the RF cycles for class C PA, Class A Class B, AB may be used as linear amplifier in power applications, while the nature of class C is nonlinear.[4]

The class C amplifier is biased below down its turn-on voltage and the input drives the active device on for a small part, which is slightly less than the cycle of inputs. This is results of the pulsed current in the devices, these currents are filtered to excerption of the basic frequency component, and this is passes through the load resistance and the output wave is the basic frequency waveform. the efficiency of class C amplifier lies between 50 to 85 percent.[5]

In this paper we present a new approach to design the class C amplifier at nano scale by using COMS technology. This pair is simulated on cadence virtuoso at 180nm scale. This pair consume very low power and improve the battery life and efficiency of communications apparatus.

Working principal of complementary compound pair

This work we present new innovative pair, this pair is design with the help of two complementary pair, this pair is designed with the help of two PMOS and NMOS transistor. The working principal of this pair is, if a complimentary pair consist NMOS in deriver stage and PMOS work as output devices, then hole pair act as a simple NMOS transistor and its vice-versa[6-8]. It can be easily understood by below figure,

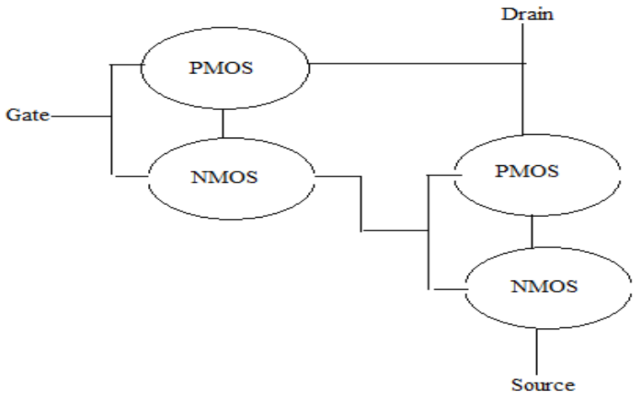

Figure 1- Model of complementary compound pair i.e. RKTG pair[6]

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This pair is very effective to increase the frequency bandwidth of signal, at very low power consumptions with very low input supply and temperature stability is high and this pair is provided high current gain[9].

II. EXPLORATORY CIRCUIT

In this part we take a transistor base class C amplifier circuit i.e., a NPN transistor whose operate at 15V Vcc and tuned circuit values L and C values are 2 µH &470pF respectively Cin be 0.1 µF R_B is 4.7KΩ, C_2 is 1000pF and load resistance is 1 KΩ.

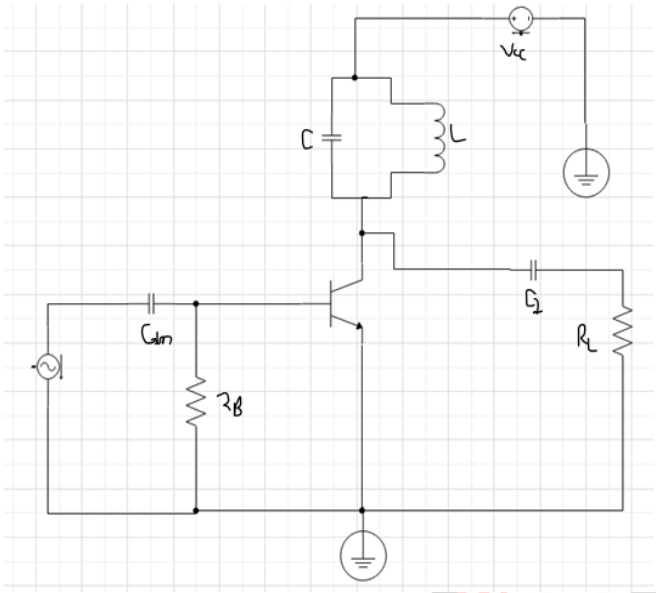

Fig 2- reference circuit model

in above circuit when we calculate some parameter like resonance frequency found 5.19MHz, inductive resistance 65.2 Ω parallel resistance values 65.2, AC load resistance 765 Ω bandwidth is 0.444KHz AC output compliance.

When all parameter are constant and one change in above circuit is NPN transistor is replace RKTG pair it is fond that lower cut off frequency **f_L = 473.42GHz** and Upper Cut off frequency **f_H = 721.96 ZHz.** Therefore, we get **bandwidth in ZHz,** but gain is slightly less than unity. When we increase the value of C_2 we get narrower bandwidths **(6.93-1.56) THz i.e., 5.37 THz with voltage gain 20db.** This circuits is simulated on Cadence virtuoso at 180nm. In above circuit when we vary the value of C_2 it is found that bandwidth and gain vary.

Table 1- variation of C_2 and bandwidth

C_{in}	L	C	C_2	f_L	f_H	bandwidth
1µ	2nH	470pF	1nF	473.42GHz	721ZHz	
			10nF	472.2 „	165.9 “	
			100nF	5.1’’	5.87’’	
			1µ	691’’	111.95EHz	
			1m	758.58’’	68.43PHz	
			1F	**1.56THz**	**6.93THz**	**5.37THz**

Simulations of circuits- this circuit is simulated on the Cadence Virtuoso software 180nm, and the firstly AC analysis are taken, the frequency response curve are given below. After this we analysis the transient analysis at MHz to GHz. This transient analysis is when the input frequency in MHz amplitude is 1mV.

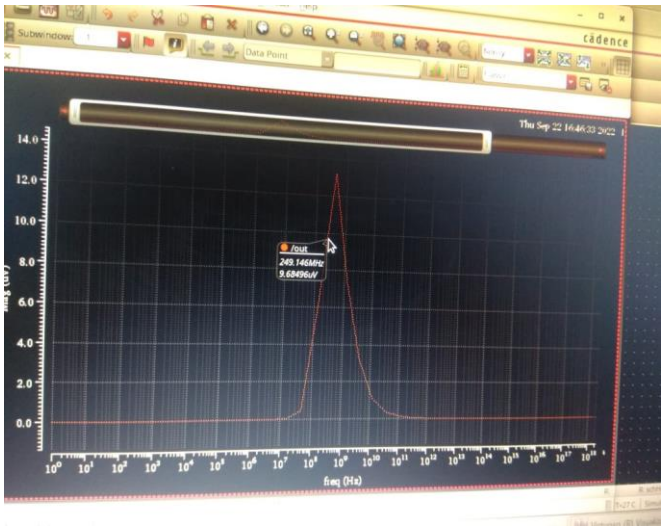

Fig- Frequency response of class c proposed amplifier

Figure- transient response of proposed class c amplifier

The power consumptions are this pair is very low in like as µW so this pair save a lot of power and increases the life of battery life use in communications devices.

S. N.	Year	Technologies	Topologies	Bandwidth	Gain	Noise figure	Power consumption
1	2001	0.35 CMOS		1.75 GHz	25dB		-
2	2004[14]	0.18CMOS	Gm Booster Common Gate	5.6GHz	-		
3	2004[15]	0.25µm CMOS	Cascade Based	900MHz		1.35 dB	
4	2005 [16]	0.18TSMC	Differential amplifier	3.1GHz - 4.8GHz	- 4.2 dB		25mW
5	2006 [17]	0.8 µm CMOS		1-5 KHz		291	24mW
6	2007 [18]	0.35 µm	Switched	8KHz			5.6µW

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7	2008 [19]		Current feed forword	20KHz			36 µW
8	2009 [20]	90nm	Current reused	7.6GHz	12.5	3dB	
9	2010 [21]	0.18 µm		3-8GHz	16.4	29dB	39mW
10	2011 [22]	65nm	Resistive shunt feedback	10GHz		0.8dB	13.7mW
11	2012 [23]	0.18 µm CMOS	Two stages		25	2.2dB	
12	2014 [24]	28nm CM OS				4.9dB	
13	2015 [25]						
14	2016 [26]	90nm	Cascade of two transistor	2.45 GHz	31.53		
15	2017 [27]	65 nm		39.35 GHz			19 µW
16	2018 [28]	55nm		10GHz	16		38.3nW
17	2019 [29]			24 GHz	31.53	0.7dB	0.03mW
18	2020 [30]						
19	This work	180nm	Complimentary compound pair (RKTG)	4.56 THz	20	-	0.36 µW

III. CONCLUSIONS

Studying above comparison table it is found that RKTG pair is more efficient than other pair like Darlington or szikli pair, and **20db voltage gain** is also achieved with the **highest bandwidth** in the range of **THz**, of class c amplifier known so far, which is better to the best of my knowledge, and **power consumptions also in order of micro** level.

IV. FUTURE WORK

In this section we work its mathematical verification of simulated result.

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