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Edge-TCT evaluation of high voltage-CMOS test structures with unprecedented breakdown voltage for high radiation tolerance

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Abstract: This paper presents the edge Transient Current Technique (eTCT) measurements of passive test-structures on the UKRI-MPW0 pixel chip, a 280 µm thick proof-of-concept High Voltage-CMOS (HV-CMOS) device designed and fabricated in the LFoundry 150 nm technology node with a nominal substrate resistivity of 1.9 kΩ cm. Samples were irradiated up to 1×10^{16} 1 MeV $n_{eq}\,cm^{-2}$ with neutrons to observe the change in depletion depth and effective doping concentration with irradiation. A depletion depth of the sensor was found to be ≈50 µm at ≈−400 V at 1×10^{16} 1 MeV $n_{eq}\,cm^{-2}$. A stable damage introduction rate (g_c) was also calculated to be $0.011 \pm 0.002\,cm^{-1}$.

Keywords: Particle tracking detectors (Solid-state detectors); Photon detectors for UV, visible and IR photons (solid-state) (PIN diodes, APDs, Si-PMTs, G-APDs, CCDs, EBCCDs, EMCCDs, CMOS imagers, etc.); Radiation-hard detectors; Solid state detectors

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Contents

1 Introduction

Trackers are an invaluable tool for high-energy physics experiments. Generally placed millimetres from the beampipe and collision centre, combined with a strong magnet they can determine the mass and charge of an ionising particle passing through the detector [1]. Due to this compact nature the sensing system has to be able to withstand high doses of radiation while also having a fine spatial and temporal resolution able to resolve multiple interactions per collision. Readout of events has to be done at a rate which, in some colliders, can reach the GHz range all while being as thin as possible so as not to disrupt the curved path of the particles [2]. To further fundamental knowledge on physics, experiments are probing higher energies and luminosities. This will mean an increase in the operational parameters of detectors. Silicon sensors are expected to endure fluences exceeding 10^{16} 1 MeV $n_{eq}\,cm^{-2}$ as part of the High Luminosity-LHC (HL-LHC), or 10^{17} 1 MeV $n_{eq}\,cm^{-2}$ as part of the Future Circular Collider for hadron-hadron collisions (FCC-hh) [3].

High Voltage-CMOS (HV-CMOS) sensors combine a high biasing voltage, for radiation tolerance and fast charge collection by drift; a fine granularity, not limited by expensive bump bonding, and a low material budget, from its integrated circuitry (IC), in a cost effective device as they are produced through an industrial standard manufacturing processes. Other options for silicon trackers do not, currently, offer the same specifications, because of this HV-CMOS is a prime candidate for reaching the requirements of future experiments. A challenge for silicon trackers is the change in doping profile after exposure to Non-Ionising Energy Loss (NIEL). NIEL decreases substrate resistivity through the introduction of acceptor states deep in the silicon, this also changes the breakdown voltage of the sensor and the depletion region around the pixel [4, 5].

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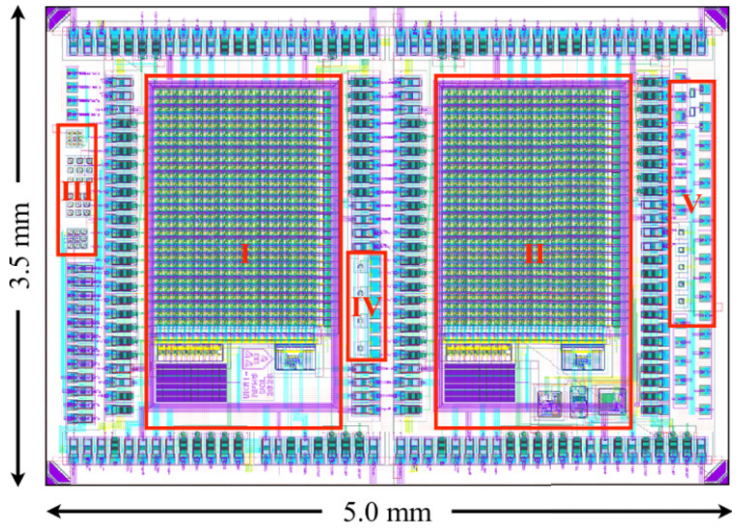
This paper presents edge Transient Current Technique (eTCT) [6] measurements of a proof-of-concept HV-CMOS sensor designed to increase the radiation tolerance through high biasing voltages.

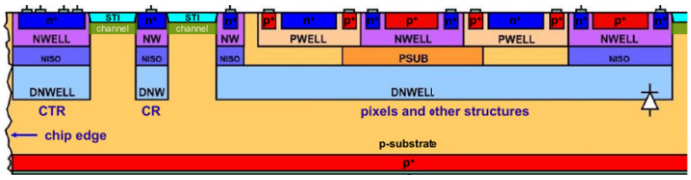
2 Samples and post-processing

2.1 UKRI-MPW0

The UKRI-MPW0 (depicted in figure 1) is a proof-of-concept HV-CMOS pixel chip crafted using the LFoundry 150 nm technology node. With a nominal substrate resistivity of 1.9 kΩ cm, the sensor has been thinned to 280 µm before being processed for backside biasing. On the chip there are two active matrices of 20 × 29 pixels with a pixel size 60 µm × 60 µm, and three sets of passive test structures for various measurements including passive pixels for eTCT, all of which are highlighted in figure 1(a). The eTCT test structures consist of four 3 × 3 passive pixels with the n-wells from the outer 8 pixels shorted together with the intent to measure the central pixel to replicate the conditions of a wider matrix. This paper focuses on the test structure which has the nominal 60 µm × 60 µm pixel size.



(a)



(b)

Figure 1. (a) The layout of the UKRI-MPW0 pixel chip. Areas I and II are the two matrices of active pixels; III is the location of the eTCT test structures, and IV, V are the locations of other passive test structures. (b) The cross-section of the UKRI-MPW0 pixel chip with the CR and CTR shown. Also highlighted is a parasitic transistor channel which can form at lower bias voltages [10].

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The chip is designed to increase the breakdown voltage beyond current capabilities of the technology by utilising backside biasing and a total lack of topside p-wells traditionally used for biasing or left floating if a backside biasing scheme is used. The topside p-well was omitted as TCAD simulations identified the area as a low resistivity current path which significantly lowered the breakdown voltage of the sensor. An n-well Cleanup Ring (CR), and an n-well Current Terminating Ring (CTR) was used instead of a conventional set of p-well rings to collect the leakage current from the edge of the chip and acts as a seal ring for the chip (see figure 1(b)) [7–9]. The reduced number of rings in this scheme increases the fill factor, but has proved to give a large leakage current (≈4 mA). The high current means the breakdown voltage of the sensor is limited by the current which can pass through the ring before thermal runaway occurs as opposed to the breakdown of the pixel itself. Although the n-well ring structure put in place has lead to a high current from the edge of the chip the scheme has achieved a breakdown voltage of ≈−600 V [10].

2.2 Backside processing

To add a backside p^+ region and metal contact for biasing, two wafers were sent to Ion Beam Services (IBS) for post-processing. Two methods were used for backside processing, BeamLine ion implantation with Rapid Thermal Annealing (BL + RTA), and Plasma Ion Implantation with Ultra Violet laser annealing (PIII + UV). BL + RTA is a well known process to the authors, however it involves heating the entire chip to high temperatures during the annealing process [11, 12]. Where as, PIII + UV is a more targeted process which better activates the implanted boron and is less likely to damage embedded electronics as it only heats the necessary parts of the chip in order to anneal the implantation damage [13, 14]. BL + RTA is the focus of this paper.

2.3 Irradiation campaign

Samples were irradiated with neutrons at the TRIGA reactor at the Jožef Stefan Institute (JSI) in Ljubljana [15]. 2 samples of each backside processing method were irradiated to varying fluences between 1×10^{13} and 1×10^{16} 1 MeV n_{eq} cm^{-2}.

3 Measurements

First the chip edge closest to the eTCT test structures was polished to remove scratches left from the dicing process which might impede the laser. 3 µm lapping was used to smooth large scratches from the edge before it was then polished with 1/10 µm grade diamond paste for the finer scratches. The chip was then glued using conducting paint to a metal contact, for backside biasing, on a custom circuit board with the eTCT test structures at the edge of the board. The pads for the test structures were wirebonded to the board so connectors could be used for reading the signal. The chip and board were placed on a Peltier cooling system inside a scanning-TCT setup provided by Particulars [16]. The chip and board were kept at −20 °C for all measurements.

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3.1 eTCT

eTCT measures the depletion region of a sensing diode by way of a pulsed Infrared (IR) laser of wavelength 1064 nm being placed incident to the edge of the chip. The focal point, or beam waist, penetrates into the silicon where it generates electron-hole pairs which drift to the collection electrodes due to the biasing field. By moving the beam waist in all three dimensions inside the silicon and recording the charge collected by the pixel at each location, the sensing region can be mapped. Current induced on the electrodes by the signal was then amplified by a discrete amplifier, and read by an oscilloscope. A 10 ns window around the current waveform was integrated to obtain an arbitrary charge collected per laser pulse. As samples were glued and polished by hand variations in pixel position from sample to sample were inevitable. To find the relevant pixel, and focus, a scan in the x and z direction (horizontal and vertical directions in figure 1(b) respectively) and a scan in the y and z directions (into the diagram and vertical directions in figure 1(b) respectively) were performed, using a knife edge technique. Once done the x and y positions were fixed. The sensor was then biased to −600 V with a compliance current in place. The z direction was then scanned over 400 µm in increments of 2 µm before the voltage was decreased and the z direction measured again, until 0 V was reached. The voltage was reduced by 25 V between −600 V and −450 V, then a finer step of 10 V was used from −450 V to 0 V. This was done to observe how the depletion region grows with voltage and how neutron irradiation damaged the sensor.

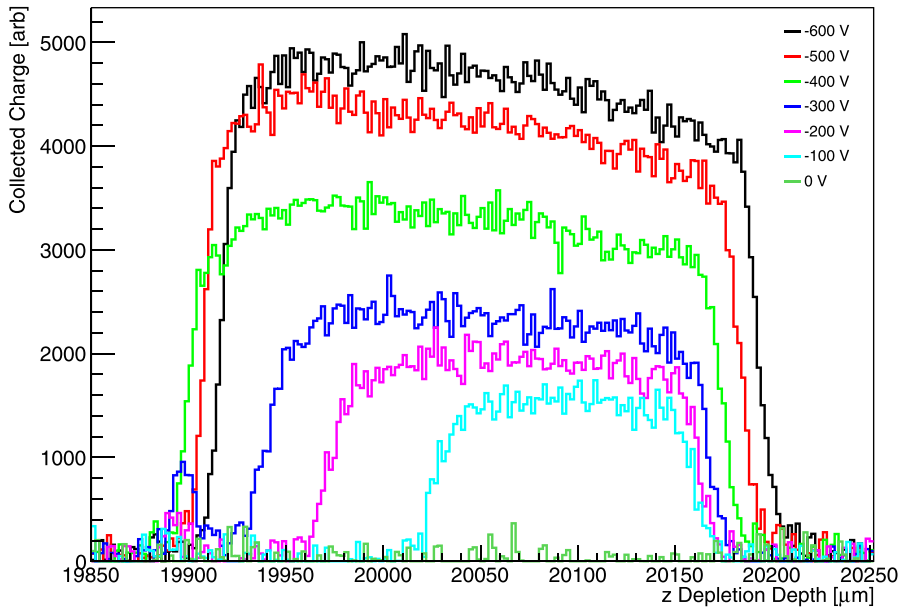

Figure 2. The arbitrary charge collected at varying bias voltages for an unirradiated BL + RTA sample. The top of the sensor sits around 20150 to 20200 µm, there is variation in the position due to oscillations in the movement stages.

4 Results and analysis

The depletion depth of a sensor was defined as a Full Width Half Maximum (FWHM) for the arbitrary charge collection profile in the z direction. This was done for every voltage measured to establish the depletion regions growth. Figure 2 shows the charge collected at varying voltages for an unirradiated BL + RTA sample. A secondary peak can be seen around 19900 µm for voltages before full depletion, this is due to backside processing. At higher voltages these peaks merge.

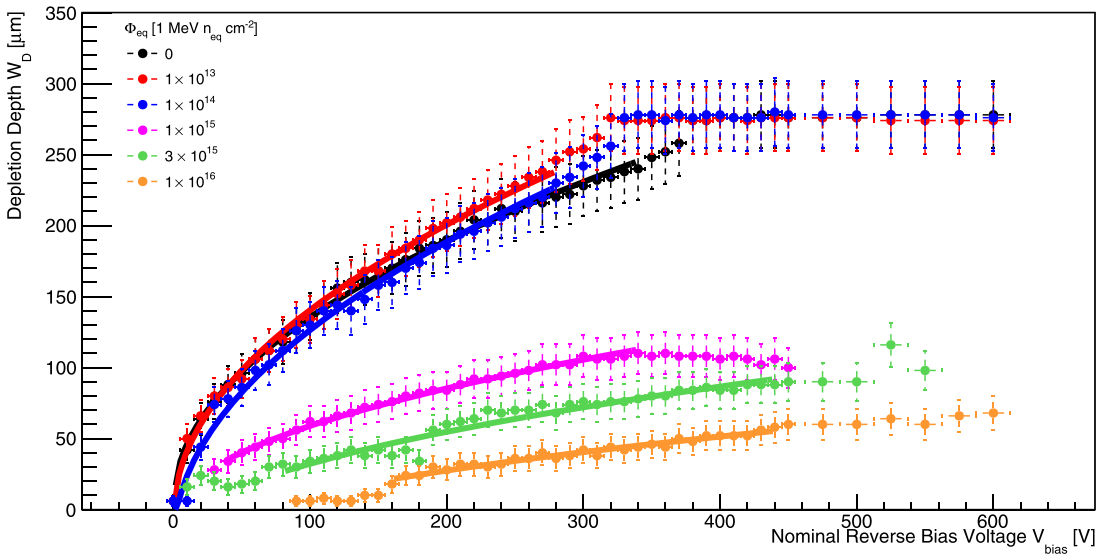

Figure 3. The depletion depth into the sensor with reverse bias voltage. With irradiation the depth to which the sensor could deplete was reduced.

The depletion depth was found by taking the maximum charge collected in the histogram and counting the number of adjacent bins above half this maximum then multiplying by the width of a single bin to find the depletion depth in micrometres. The uncertainty of the depletion depth was calculated using the square root of the number of counted bins multiplied by the bin width. The depletion growth with reverse bias can be fitted to find the effective doping concentration $N_{\text{eff},0}$ through:

$$W_{\text{D}} = W_0 + \sqrt{\frac{2\epsilon}{qN_{\text{eff}}} V_{\text{bias}}}, \tag{4.1}$$

where W_{D} is the depletion depth, W_0 is the depletion depth at 0 V, ϵ is the permittivity of silicon, q the charge of an electron, and V_{bias} the reverse bias voltage. Equation (4.1) was fit to the depletion depth with voltage for all measured samples, figure 3. The data points were fitted before full depletion or breakdown voltage was reached to accurately represent the growth of the depletion region. At low fluences the depletion depth growth follows equation (4.1) and the sensors are able to reach the full depletion. Full depletion can be seen in figure 3 as a discontinuity in between 300 V and 400 V for the unirradiated and lower fluence samples; this can be attributed to the

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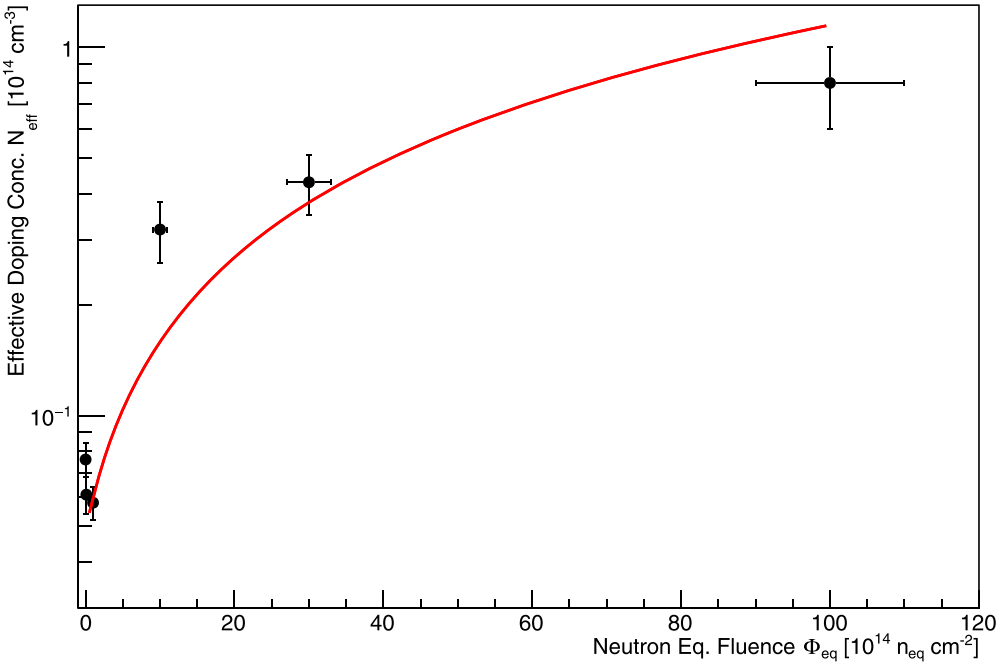

Figure 4. The doping concentration of each sample against irradiated fluence. At lower fluences there is a decrease in doping concentration before it increases again.

backside processing. Backside processed samples produce two depletion peaks for the topside n-well pixel, and the backside p^+ region as mentioned when discussing figure 2. As the voltage increases the depletion region around the topside well grows down into the substrate where the two meet [17]. With further irradiation the depletion depth grows at a slower rate and the discontinuity disappears due to the sensor not being able to fully deplete. At the highest fluence of 1×10^{16} 1 MeV $n_{eq}\,cm^{-2}$ a depletion depth of ≈50 µm is achieved at −400 V.

The effective doping profile extracted from the fit was also used to find the resistivity of the chip [18]. The nominal resistivity of the substrate is 1.9 kΩ cm, however the actual resistivity was found to be 1.19 ± 0.14 kΩ cm which is in agreement with measurements of similar sensors crafted in the same technology, process, and nominal resistivity [19, 20]. The effective doping concentration is plotted against the fluence and fitted using:

$$N_{\text{eff}} = N_{\text{eff},0} - N_c(1 - e^{-c\phi_{\text{eq}}}) + g_c\phi_{\text{eq}}, \tag{4.2}$$

where $N_{\text{eff},0}$ is the effective doping concentration before irradiation, N_c is the concentration of acceptors which have been deactivated, with c being the acceptor deactivation constant, g_c is the stable damage introduction rate, and ϕ_{eq} corresponds to the irradiated fluence. Equation (4.2) describes the initial acceptor deactivation and continual increase in effective doping of a silicon semiconductor. Figure 4 shows a decrease in doping concentration between 0 and 1×10^{14} 1 MeV $n_{eq}\,cm^{-2}$, which is consistent with initial acceptor deactivation, before the doping concentration increases again with radiation damage. At higher fluences the linear terms of the equation can be seen to dominate. The fitting parameters from equation (4.2), shown in table 1,

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have large uncertainties, however the data was sufficient to establish the stable damage introduction rate (g_c) as $0.011 \pm 0.002\,\mathrm{cm}^{-1}$, which was lower than other measurements of chips produced with the same and different technologies, but was in agreement with the literature, as were the other variables of the fit, table 1 [17, 19, 21, 22].

Table 1. Extracted parameter values from equation (4.2) and figure 4.

		UKRI-MPW0
N_{eff0}	$[10^{14}\ \mathrm{cm}^{-3}]$	0.076 ± 0.008
N_c	$[10^{14}\ \mathrm{cm}^{-3}]$	0.027 ± 0.010
c	$[10^{-14}\ \mathrm{cm}^{2}]$	9 ± 8
g_c	$[\mathrm{cm}^{-1}]$	0.011 ± 0.002

5 Conclusion

A proof-of-concept, backside bias only, prototype HV-CMOS pixel chip was irradiated to varying fluences up to 1×10^{16} 1 MeV $\mathrm{n_{eq}\,cm^{-2}}$ and a passive test structure was measured by eTCT between nominal biases of 0 V and −600 V to observe changes in doping concentration, resistivity, and depletion region growth with NIEL damage. It was shown that at there is a depletion of ≈50 µm at ≈−400 V after 1×10^{16} 1 MeV $\mathrm{n_{eq}\,cm^{-2}}$ of irradiation. The decrease in depletion region was also fit. Although there were large uncertainties in the fitting parameters, it was found that the stable damage introduction rate (g_c) was $0.011 \pm 0.002\,\mathrm{cm}^{-1}$, which is in agreement with literature.

Acknowledgments

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