Non-Volatile Resistive Switching in $PtSe_2$-Based Crosspoint Memristors

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Introduction: Two-dimensional (2D) materials such as transition metal dichalcogenides (TMDCs) have gained attention for neuromorphic computing applications due to their resistive switching (RS) behavior [1, 2]. Among TMDCs, platinum diselenide ($PtSe_2$) stands out because it can be grown at complementary metal-oxide-semiconductor (CMOS) back-end-of-line (BEOL) compatible temperatures [3, 4] and it has shown excellent long-term stability [5]. However, its potential for RS remains largely unexplored with only preliminary proof-of-concept characteristics presented in a multilayer $PtSe_2$ device with Au electrodes [6]. Here, we present the first detailed study on forming free RS in $PtSe_2$-based crosspoint (CP) memristors using CMOS-compatible electrodes. We find remarkably low switching fields (0.08 V/nm) likely related to our choice of electrode materials and excellent retention for at least several days.

Fabrication: CP memristors with ~32 μm^2 area have been fabricated by sandwiching multilayer $PtSe_2$ between Pd and Ni electrodes. A device schematic and an optical micrograph are depicted in **Fig. 1a-b**. The Pd back electrode (BE) was embedded into a SiO_2/Si substrate via subsequent reactive-ion etching (RIE), electron-beam evaporation of 10 nm Ti and 50 nm Pd and lift-off, leading to an electrode height of 23.5 nm from the substrate surface as confirmed by atomic force microscopy (AFM) (**Fig. 1c**). Nanocrystalline, 12.5 nm thick $PtSe_2$ was grown via thermally assisted conversion (TAC) [4] of a 4.1 nm Pt film on SiO_2/Si substrates and analyzed by AFM (**Fig. 1d**). **Fig. 1e** shows the characteristic Raman peaks of the as-grown material (August 2020) and after transfer and etching (April 2021). The identical peak positions indicate no significant quality change in $PtSe_2$ after long-time exposure to air (~9 months) and processing. $PtSe_2$ was transferred onto the BE substrate by using a KOH-based wet transfer technique. It was then successfully patterned by RIE as confirmed by the Raman maps of the characteristic peaks (**Fig. 1f-i**). Finally, the top electrode was defined by DC-sputtering of 55 nm Ni and lift-off.

Results: We performed current-voltage (I-V) sweeps on four devices with a total of 45 bipolar switching cycles (**Fig. 2a**). The SET transition from the high resistive state (HRS) to the low resistive state (LRS) occurred at voltages between -1.1 V and -1.5 V. The RESET transition (LRS to HRS) was observed for voltages between 1.1 V and 1.7 V. Despite a noticeable device-to-device and cycle-to-cycle variability, we found a stable switching window of at least 139 kΩ ($R_{HRS}/R_{LRS} = 9$) as shown in the box plots of the resistances (**Fig. 2b**). Excellent retention characteristics confirm the non-volatility of the RS for at least 3 days and 22 hours (**Fig. 2c**). After the respective DC SET/RESET sweeps, the current was read at V_{read} = 100 mV for 14 hours continuously followed by an additional 10 min measurement after waiting for 3 days and 7 hours, while the device was kept in ambient. Pulsed voltage stress (PVS) is the realistic mode of operation for RS devices [7]. **Fig. 2d** shows the transients of a voltage pulse (width 5 ms, rise and fall times 0.5 ms) that was applied to a device to obtain the corresponding I-V curves shown in **Fig. 2e**. A device from a second fabrication run showed particularly low switching voltages ($|V| <= 1$ V). Seven initial I-V curves of that device are depicted in **Fig. 2f**. Comparing the switching fields (V/thickness), we find that our $PtSe_2$ requires lower electric fields (0.116 V/nm average run 1, 0.08 V/nm best run 2) compared to other forming-free 2D materials or previous $PtSe_2$ with Au electrodes while maintaining its non-volatility (**Table 1**). The low switching field indicates the potential for reduced switching voltage and power consumption and could be related to the diffusivity of Ni in $PtSe_2$ subject to future investigations. Benchmarking of our $PtSe_2$ RS devices vs. other 2D materials highlights also the lower, BEOL-friendly growth temperature and use of CMOS compatible materials in the device stack (**Table 1**).

Conclusion: We presented the first detailed study on $PtSe_2$ RS showing excellent retention, consistent switching windows, long-term material stability under ambient conditions, and comparatively low switching fields. This, in combination with the materials CMOS BEOL compatibility, shows the great potential of $PtSe_2$ for RS devices.

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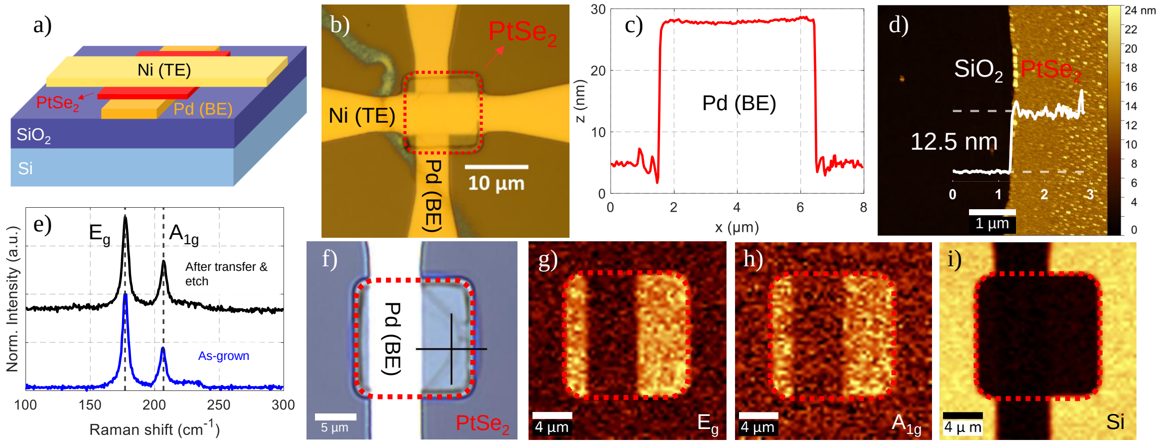

Fig. 1: (a) Schematic of a $PtSe_2$ crosspoint (CP) memristor. (b) Optical micrograph of a CP. (c) AFM electrode height profile of the embedded back electrode (BE) that shows that 23.5 nm of the total 60 nm protrude from the substrate surface. (d) AFM scan of the as-grown $PtSe_2$. The inset height profile shows a thickness of about 12.5 nm. (e) Raman spectra of $PtSe_2$. The transferred spectrum was taken at the spot marked by the black cross in f). (f) Micrograph of etched $PtSe_2$ on top of BE and Raman scan peak intensities (brighter – higher) of the (g) E_g, (h) A_{1g}, and (i) Si peak.

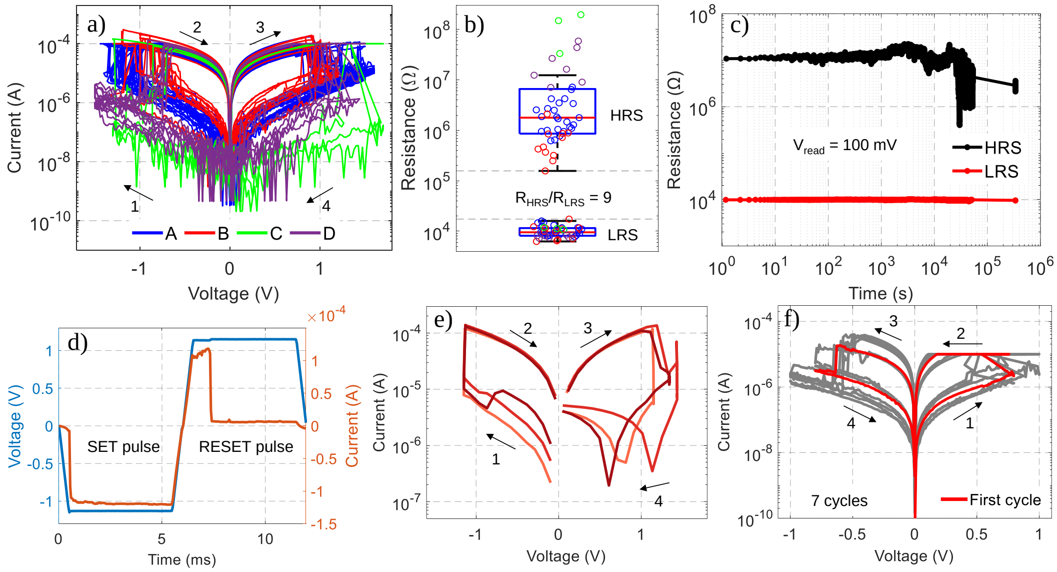

Fig. 2: (a) Bipolar I-V curves of 4 devices (A-D) with a total of 45 switching cycles. The numbers 1-4 show the sequence of the voltage sweeps (1: 0 V to SET, 2: SET to 0 V, 3: 0 V to RESET, 4: RESET to 0 V) (b) Boxplot of high (HRS) and low resistive states (LRS) from (a). (c) Stable state retention for at least 3 days and 22 hours. (d) Pulse waveform corresponding to (e). (e) Pulsed I-V curves. (f) I-V curves of a device from a second fabrication run.

Material	Growth T (°C)	Thickness (nm)	Switching field (V/nm)	Electrode Material	Ref.
$PtSe_2$	**400 (TAC)**	12.5	0.116	**Pd/Ni**	This work average
$PtSe_2$	**400 (TAC)**	12.5	**0.080**	**Pd/Ni**	**This work best**
$PtSe_2$	**400 (TAC)**	3	0.233	Au	[6]
MoS_2	500 (MOCVD)	2.1	0.333	Au	[1]
MoS_2	500 (MOCVD)	2.8	0.357	Au	[1]
h-BN	1000 (CVD)	2	0.200	Ti/Cu	[8]
h-BN	1000 (CVD)	5.8	0.121	Ti/Cu	[8]

Table 1: Benchmarking of our $PtSe_2$ devices with forming-free multilayer 2D material memristors from literature.