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A 1 MHz soft-switching boost DC-DC converter with matching network

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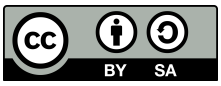
ABSTRACT

This paper introduces a high-performance zero-voltage-switching (ZVS) boost converter, which is capable to operate under different load currents. By utilizing matching network, the proposed topology can achieve ZVS over a wide range of input voltages. Due to the switching loss is minimized, the proposed circuit is suitable for operation at switching frequencies on the order of several MHz. Steady-state analysis and detailed description of the proposed circuit are discussed. The power-loss and design procedure are introduced. The proposed converter has been simulated to verify the presented analytical approach at 1 MHz and deliver 80 W output. The peak power efficiency achieves 94.2%.



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1. INTRODUCTION

Increasing the frequency leads to improve power density, fast response, and state-of-the-art DC-DC power converters with high efficiency. Due to high frequencies, power converters have become lighter and small in size [1]-[5]. However, high frequencies cause increasing in switching losses. As a result, the efficiency of the whole system is decreased. Among various topologies, many schemes have been previously presented ZVS converters using resonance to perform soft-switching technique [6]-[11]. Some resonant converters utilize auxiliary circuit to enable soft-switching for the main switch of the converters while the switch of auxiliary circuit operates with hard switching [12]. Moreover, the auxiliary circuit increases the complexity of the circuit. Thus, the whole efficiency of system decreases due to switching losses.

Various converters were demonstrated to achieve zero-voltage switching (ZVS) operation by adjusting the impedance of resonant network or using matching network [13]-[17]. This paper proposes a soft-switching boost DC-DC power converter with matching network circuit. The matching network consists of two capacitors and one inductor. It modifies the drain-source voltage of the main switch of the converter to perform soft-switching under ZVS condition.

Moreover, the matching network can bring benefit, such as maximize the transferred power between the supply and load, decrease the reflection and prevent the returns for the load of the converter [18]-[21]. The steady-state operational principle and power loss of the proposed converter are analyzed in detail. In order to fully characterize the proposed topology, a design procedure has been provided. Then, simulation results are presented to confirm ZVS condition for the main switch of the converter at 1 MHz.

2. TOPOLOGY ANALYSIS AND DESCRIPTION OF THE PROPOSED CONVERTER

A schematic of the proposed boost dc-dc power converter is depicted in Figure 1. It comprises of an inductor L, a main switch M, a capacitor C_T, a matching network, an output capacitor C_O and a load R_L. The matching network comprises of two capacitors (C_{S1} and C_{S2}) and an inductor L_F. The main switch M of the converter operates with soft-switching technique by tuning the elements of matching network. The converter has two operating modes: when the power transistor M is closed, the majority of main inductor current i_L flows through the switch current i_S. When the switch M is opened, the switch voltage will ring up at the half of switching period then back to zero.

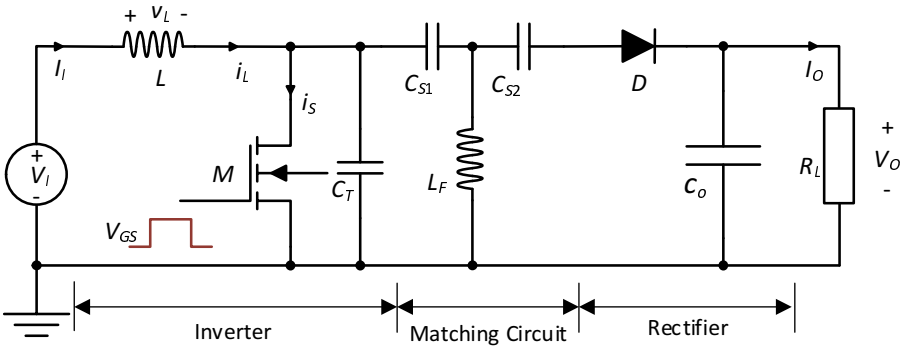

Figure 1. Proposed topology of boost DC-DC power converter

2.1. Configuration of the proposed boost converter

A T-shaped matching network is connected between the inverter and the rectifier of the power boost DC-DC converter as depicted in Figure 1. The proposed converter enables soft-switching through matching network by modifying the switch voltage drain-source voltage (V_{DS}). The idealized voltage and current waveforms are shaped in Figure 2 to explain the principle operation of the proposed topology.

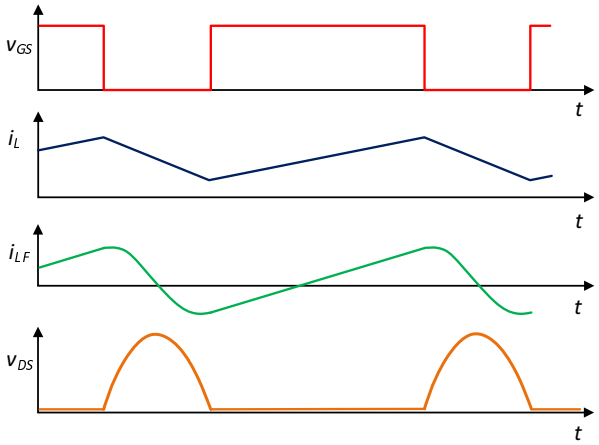

Figure 2. Idealized waveforms of the proposed boost DC-DC power converter

During time interval $0 < t \leq$ dT, the voltage across the inductor L equals the DC input voltage V_I. Hence, the inductor current starts from an initial value and increases linearly. At the same time, the diode D is switched from forward to reverse biased and the voltage across the diode D is $V_D = -V_O$. During the interval dT $< t \leq$ T, the power transistor M is opened by the gate-source voltage V_{GS}. Thus, the voltage across the inductor is $v_L = V_I - V_O$ and the main inductor current i_L waveform decreases linearly. At the end of period T, the power transistor M is closed again. In this topology, the current waveform i_L of inductance L operates

in continuous current mode (CCM). Therefore, the change in inductor current during [0, dT] is expressed as:

$$\Delta i_L = \frac{V_I}{L} dT, \tag{1}$$

where d is the duty cycle of the power transistor M and T is the switching period. During the interval time [dT, T], the estimated inductor ripple current is:

$$\Delta i_L = \frac{V_O - V_I}{L} dT. \tag{2}$$

from (1) and (2), the output voltage of the proposed boost dc-dc converter can be given as:

$$V_O = \frac{V_I}{d_1}, \tag{3}$$

where d_1 is the interval time when the power transistor is opened under condition ($d + d_1 = 1$).

2.2. Impedance analyze

A T-shaped matching network, which is considered high-pass and combined of two capacitors and one inductor, transforms the resistance of the inverter to the rectifier. Figure 3 shows the equivalent circuits of the matching network, which provides DC blocking and allows for fast transient response of the converter. Moreover, the matching network transforms maximum power to the output stage of the proposed DC-DC converter. In order to make the converter achieves soft-switching technique, the matching network is analyzed using s-domain to obtain the frequency response of the equivalent circuit.

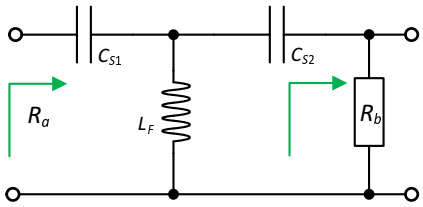

Figure 3. Equivalent impedance of network matching circuit

The output resistance R_a of the inverter can be expressed as:

$$R_a = \frac{s^3 L_F C_{S1} C_{S2} R_b + s^2 (L_F C_{S1} + L_F C_{S2}) + s C_{S2} R_b + 1}{s^3 L_F C_{S1} C_{S2} + s^2 C_{S1} C_{S2} R_b + s C_{S1}}, \tag{4}$$

where R_b is the input resistance of the rectifier. The coefficients of the real and imaginary components of the above equation are equivalent. The input resistance of the inverter is given as (5).

$$R_a = \frac{1 - \omega^2 (L_F C_{S1} + L_F C_{S2})}{-\omega^2 C_{S1} C_{S2} R_b}. \tag{5}$$

The relationship between the capacitance C_{S1} and the capacitance C_{S2} is:

$$C_{S1} = A C_{S2}. \tag{6}$$

where A is a constant. Based on equation (5), (6), the equation (7) can be expressed as (7).

$$R_a R_b = \frac{\omega^2 L_F C_{S2} (A + 1) - 1}{A \omega^2 C_{S2}^2}. \tag{7}$$

The components of matching network can be obtained as:

$$C_{S2} = \frac{1}{A\omega} \sqrt{\frac{R_a A^2 - R_b}{R_a R_b (R_a - R_b)}}, \tag{8}$$

$$C_{S1} = \frac{1}{\omega}\sqrt{\frac{R_a A^2 - R_b}{R_a R_b (R_a - R_b)}}, \tag{9}$$

and the inductance L_F is defined as (10).

$$L_F = \frac{1}{\omega^2 C_{S2}} \frac{R_b A R_b}{A(R_b - R_a)}. \tag{10}$$

According to [22], the output resistance of the inverter can express as:

$$R_a = \frac{\left(\frac{4}{\pi} V_I\right)^2}{2P_I}, \tag{11}$$

and the input capacitance of the rectifier expressed as (12).

$$R_b = \frac{\left(\frac{4}{\pi} V_O\right)^2}{2P_O}. \tag{12}$$

The bode plot and phase margin of the matching network is depicted in Figure 4. It can be noticed that maximum value of the input resistance is -70 when the frequency is changed from 1 Hz to 10 MHz.

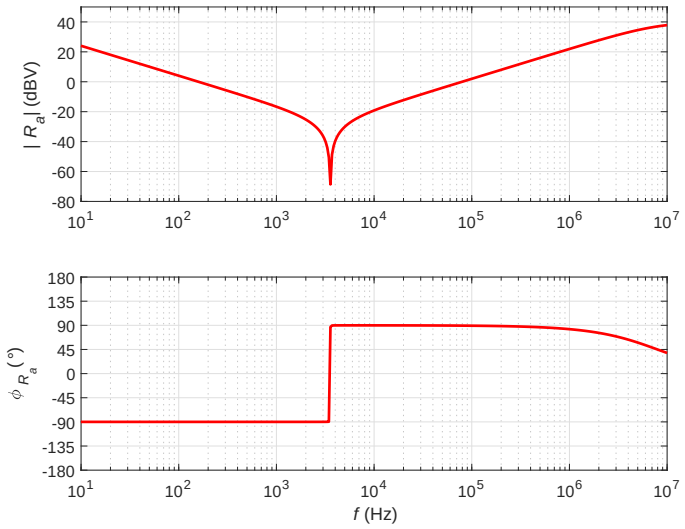

Figure 4. Bode plot of matching network circuit

2.3. Power losses

The power dissipation of the proposed boost DC-DC power converter is presented. The switching losses are significant in the megahertz range of power converters [23]-[25]. Since the main switch M of the proposed converter operates in ZVS operation, the switching losses are eliminated in the converter. To estimate the losses of the converter, it is considered that the ripple of the main inductor current is free. Thus, the inductor current i_L equals to the input current I_I. During the interval $0 < t \leq$ dT, the current that flows through the main power switch is approximated as (13).

$$i_S = I_I = \frac{I_O}{1-d}. \tag{13}$$

The rms current value of the power switch M can be expressed as (14).

$$i_{S(rms)} = \sqrt{\frac{1}{T}\int_0^{dT} i_S^2 \, dt} = \frac{I_O}{1-d}\sqrt{\frac{1}{T}\int_0^{dT} dt} = \frac{I_O\sqrt{d}}{1-d}. \tag{14}$$

Hence, the power conduction of the switch is given by (15).

$$P_{FET} = i^2_{S(rms)} r_{on} = \frac{I_O^2 r_{on} d}{(1-d)^2} = \frac{r_{on} d P_O}{R_L (1-d)^2}. \tag{15}$$

During the interval time dT $< t \leq$ T, the current flows through the diode is expressed as (16).

$$i_D = I_I = \frac{I_O}{1-d}. \tag{16}$$

Thus, the rms value can be given as (17).

$$i_{D(rms)} = \sqrt{\frac{1}{T} \int_{dT}^{T} i_D^2 \, dt} = \frac{I_O}{1-d} \sqrt{\frac{1}{T} \int_{dT}^{T} dt} = \frac{I_O \sqrt{d}}{1-d}. \tag{17}$$

Therefore, the dissipated power in the diode D is approximated as (18).

$$P_D = i^2_{D(rms)} R_F = \frac{I_O^2 R_F d}{(1-d)} = \frac{R_F P_O}{R_L (1-d)}. \tag{18}$$

The inductor current is approximated as (19).

$$i_L = i_{L(rms)} \approx I_I = \frac{I_O}{1-d}. \tag{19}$$

Then, the dissipated power by conduction in the inductors of the proposed topology is given by (20).

$$P_L = i^2_{L(rms)} (r_L + r_{LF}) = \frac{I_O^2 (r_L + r_{LF})}{(1-d)^2} = \frac{(r_L + r_{LF}) P_O}{R_L (1-d)^2}. \tag{20}$$

The conduction current that flows through the output capacitor C_O is approximated as (21).

$$i_C = I_I - I_O = \frac{d I_O}{1-d}. \tag{21}$$

Therefore, the rms current value of the capacitor is determined as (22).

$$i_{C(rms)} = \sqrt{\frac{1}{T} \int_{0}^{T} i_C^2 \, dt} = I_O \frac{d}{1-d}. \tag{22}$$

The conduction power loss, which is dissipated in the capacitors of the power converter, is expressed as (23).

$$P_C = i^2_{C(rms)} (r_{CO} + r_{CS1} + r_{CS2}) = \frac{d I_O^2 (r_{CO} + r_{CS1} + r_{CS2})}{(1-d)} = \frac{d (r_{CO} + r_{CS1} + r_{CS2}) P_O}{R_L (1-d)}. \tag{23}$$

The overall dissipated power of the proposed boost dc-dc power converter can be approximated by (24).

$$P_{LOSS} = P_{FET} + P_D + P_L + P_C. \tag{24}$$

Thus, the efficiency η of the proposed topology is given by (25).

$$\eta = \frac{P_O}{P_O + P_{Loss}}. \tag{25}$$

2.4. Design procedure

A design procedure for the proposed boost DC-DC power converter is presented at operating switching frequency $f_s = 1$ MHz. The design is applied to calculate the values of the components for the proposed boost converter and matching network (C_{S1}, C_{S2}, and L_F). The output power P_O and the duty cycle d were selected to be 80 W and 62%, respectively. The input voltage of the converter is V_I= 150 V. From (3), the output voltage of the converter is $V_O = 400$ V. According to (11) and (12), the values of $R_a = 228$ Ω and R_b= 1622 Ω. It is assumed that the value of constant A = 1. Based on (9) and (8), the value of C_{S1} and C_{S2} are 26 nF and 26 nF, respectively. From (10), the inductance L_F of matching network is 258 μH. According to subsection (2.3.), the dissipated power by conduction of the proposed boost dc-dc power converter is determined. From (15), the conduction power loss, which is dissipated in the MOSFET (IXFH34N65X3), is $P_{FET} = 1.21$ W. According to (18), the dissipated power in the diode (MUR1560) is $P_D = 1.71$ W. Based on (20) and (23), the power loss due to the inductance and the capacitance are $P_L = 1.15$ W and $P_C = 0.85$ W. As a result, the total power loss of the proposed topology is calculated $P_{Loss} = 4.92$ W. Figure 5 shows the relationship between the efficiency η and the output power P_O for the proposed topology and the conventional converter. The specification of components for the proposed converter are shown in Table 1.

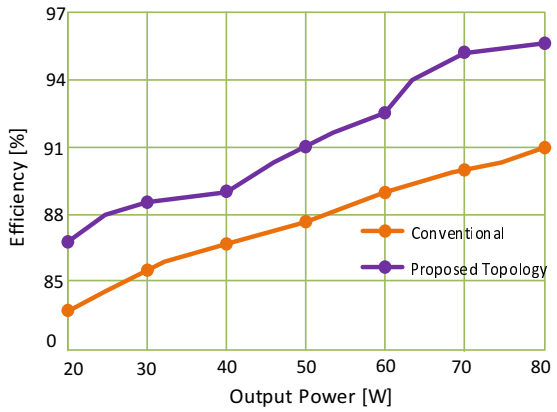

Figure 5. Output power and efficiency of conventional boost and proposed topology

Table 1. Performance parameters of proposed DC-DC power converter

Components	Value
Supply voltage V_I	150 V
Output voltage V_O	400 V
Load resistance R_L	2 KΩ
Output power P_O	80 W
Inductors L, L_F	90 μH (L), 258 μH (L_F)
Capacitors C_T, C_{S1}, C_{S2}, C_O	25 μF (C_T), 26 nF (C_{S1}), 26 nF (C_{S2}), 35 μF (C_O)

3. RESULTS AND DISCUSSIONS

Figure 8 shows the switch signal V_{GS}, the inductor current i_L, the output current of the converter i_O, and the output voltage V_O waveforms. It is clear that the output voltage of the proposed topology is constant at 1 MHz operating switching frequency. Thus, the proposed circuit is eligible to operate at high frequencies with low switching losses. The proposed circuit was also tested at full power with the input voltage $V_I = 170$ V. Under this condition, the efficiency of the converter is $\eta = 94\%$.

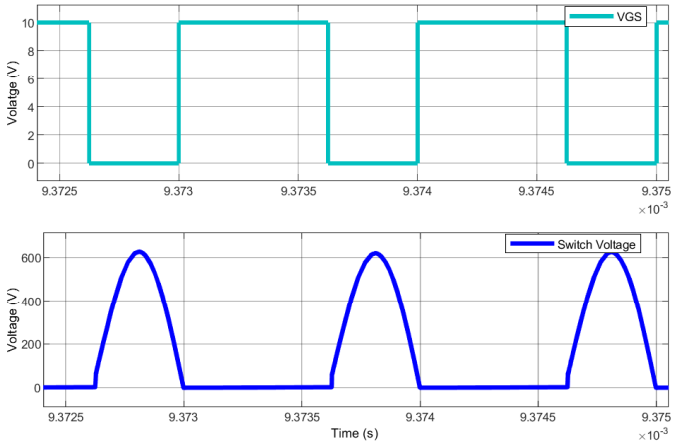

Figure 6. Gate-source voltage and switch voltages with ZVS technique

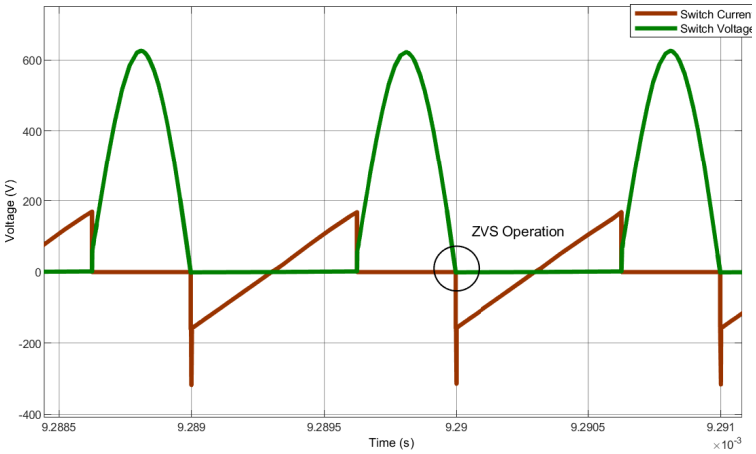

Figure 7. Voltage and current waveforms for the main switch M of the proposed converter

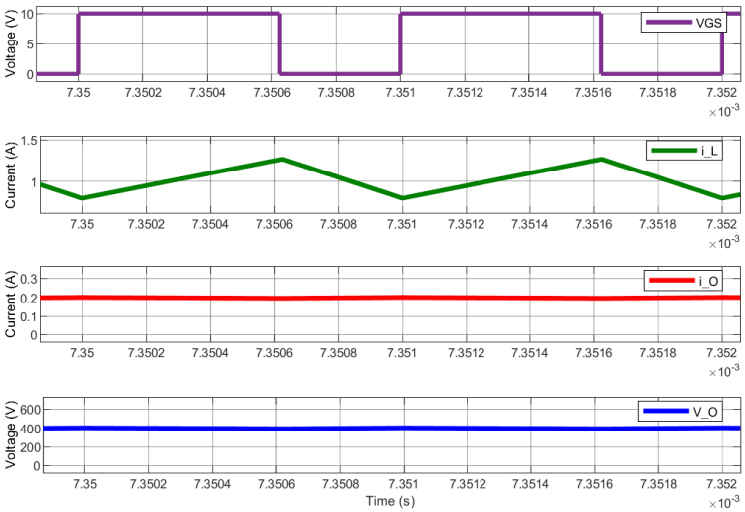

Figure 8. Inductor current, output current, and output voltage waveforms of the proposed converter

4. CONCLUSION

A soft-switching boost DC-DC converter has been introduced in this paper that uses a matching network as interface circuit between the rectifier and the inverter. The main switch of the converter performs ZVS condition by using the matching network to modify the switch voltage of the converter. The proposed topology has been analyzed and designed in details. It has high flexibility of design and low number of passive elements. A 1 MHz prototype has been confirmed by simulation to demonstrate ZVS operation. It is shown that the performance of the proposed boost dc-dc power converter is better than the conventional boost converter. The proposed converter is suitable for applications, such as, high-frequency converters, battery chargers, and photovoltaic DC-DC power converters.

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