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Hysteresis control of the new split-packed-U-cell inverter

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ABSTRACT

The authors provide a novel hysteresis control method for the SPUC inverter in this paper. The suggested system, which consist of the SPUC inverter and the balancing algorithm can offer eleven levels at output voltage using only seven switches, a closed loop is applied to maintain capacitors voltage at desired values, another hysteresis control that ensures capacitors voltage self-balancing is implemented in open loop which result in the proposed SPUC9 inverter .No voltage sensor or filtering is needed, as a consequence the inverter and installation expenses are kept to a minimum. The authors utilized MATLAB/Simulink environment to simulate the proposed converters. Simulation results prove all the concepts given in this paper. Total harmonic distortion remains reduced and depends on the hysteresis bandwidth.

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1. INTRODUCTION

In recent years, multilevel inverters have recieved a lot of attention because of their benifits including, low electromagnetic interference (EMI), decreased voltage stress (dv/dt), minimal total harmonics distortion (THD) and high power conversion. Three basic topologies are considered, namely, Neutral Point Clamped (NPC) [1], cascaded H-Bridge (CHB) [2] and the flying capacitor (FC) [3]. Many topologies have borne, such as packed-U-cell (PUC) [4], and split-packed-U-cell (SPUC) [5], and they become very competitive due to their capacity for producing high levels of voltage while utilizing a minimal amount of power components.

However, the major problem in multilevel converter topologies is balancing capacitors voltages, in fact, their imbalance can seriously harm semiconductors and passive components. As solutions, three ideas are proposed, the first option consist of applying a closed loop regulation [6]–[20] using proportional integral (PI) regulators and sensors but this solution is incompatible with several industrial uses.Some electronics circuits are includes in the second option,resulting in hefty converters [21], [22]. However,in the third option redundant states are used to provide capacitors voltage self-balancing ,as a result, a very simple implementation is obtained [23]–[25].

In this paper, the authors provide a novel hysteresis control method for the SPUC inverter, the later which is designed using two converters which are PUC and NPC may provide a high number of levels with few device components. Firstly, a closed loop control is used to maintain capacitors voltages at desired values, as a result, the inverter offers eleven levels using only seven switches, another hysteresis controller is applied on the SPUC inverter, this method insures capacitors voltage self-balancing without the need of filters or a voltage feed-back sensor.

2. RESEARCH METHOD

In this section, a closed loop regulation is applied on the SPUC inverter. This method which is based on hysteresis control provides eleven levels at the output voltage, another multilevel hysteresis technique that assures self balancing of capacitors voltages is related to the proposed inverter. By taking advantage of redundant states, it can offer nine levels in open loop operation without the usage of any regulators or filters.

2.1. Eleven level SPUC inverter structure, switching states and closed loop capacitors voltage balancing method

The SPUC inverter is inspired by the original seven-level PUC converter. As indicated in Figure 1, an extra four quadrant power device is placed and linked to the lower capacitor mid-point. When Vc1=Vc2=E/5, the topology provides a maximum of eleven voltage levels.

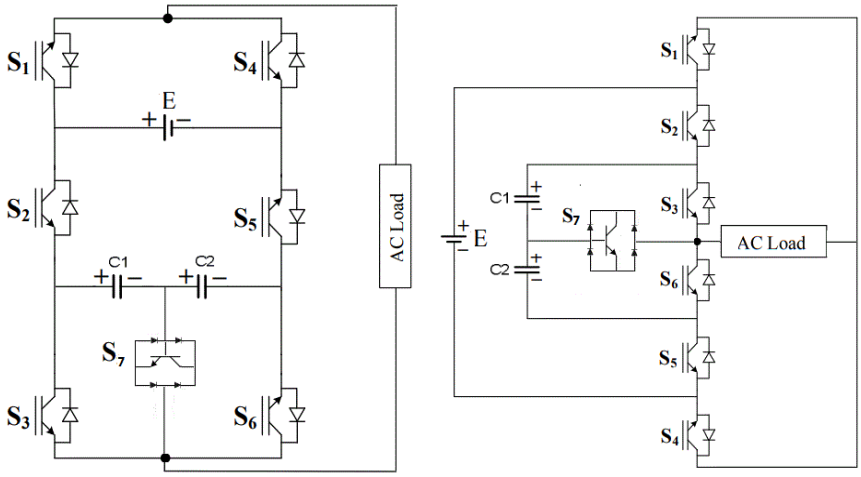


Figure 1. SPUC Inverter Circuit diagram

Table 1 presents the eleven required levels operations. The third column gives an example when direct current (DC) source is equal to 300 V. All possible situations are presented in the second column. One can remark the two redundant states 6 and 6'.

Table 1. Switching sequence for the eleven level SPUC inverter.

State	Interconnection	Voltage (V)	S1	S2	S3	S4	S5	S6	S7
11	E	300	1	0	0	0	1	1	0
10	E-Vc2	240	1	0	0	0	1	0	1
9	E-(Vc1+Vc2)	180	1	0	1	0	1	0	0
8	Vc1+Vc2	120	1	1	0	0	0	1	0
7	Vc1	60	1	1	0	0	0	0	1
6	0	0	1	1	1	0	0	0	0
6'	0	0	0	0	0	1	1	1	0
5	-Vc2	-60	0	0	0	1	1	0	1
4	-Vc1-Vc2	-120	0	0	1	1	1	0	0
3	(Vc1+Vc2)-E	-180	0	1	0	1	0	1	0
2	Vc1-E	-240	0	1	0	1	0	0	1
1	-E	-300	0	1	1	1	0	0	0

The following equation can be used to presente the reference of the AC load voltage:

$$V_L=K_p\tilde{i_L} + K_i \int \tilde{i_L} dt \quad (1)$$

When:

$$\tilde{i_L} = i_L{}^* - i_L \quad (2)$$

The load current reference is represented by i_L*. A PI controller adjusts the capacitor voltage in such a way that:

$$i_L{}^* = (K_{p1}\widetilde{v_1} + K_{i1}\int \widetilde{v_1}\, dt) + (K_{p2}\widetilde{v_2} + K_{i2}\int \widetilde{v_2}\, dt) \quad (3)$$

$$\widetilde{v_1} = v_{c1}{}^* - v_{c1}\,,\ \widetilde{v_2} = v_{c2}{}^* - v_{c2} \quad (4)$$

where v_{c1}* , v_{c2}* are the capacitors voltages references.

Table 1 is thus used to obtain the eleven voltage levels. The suggested control technique is depends on the ten band hysteresis method, when Δi which is the current error is negative. Positive voltages are applied (part A in Figure 2). Inversely,when the Δi is positive, negative voltages are used (part B in Figure 2). Δi presents the real load current minus the current reference. Figure 3 depicts the eleven states and their transition conditions.

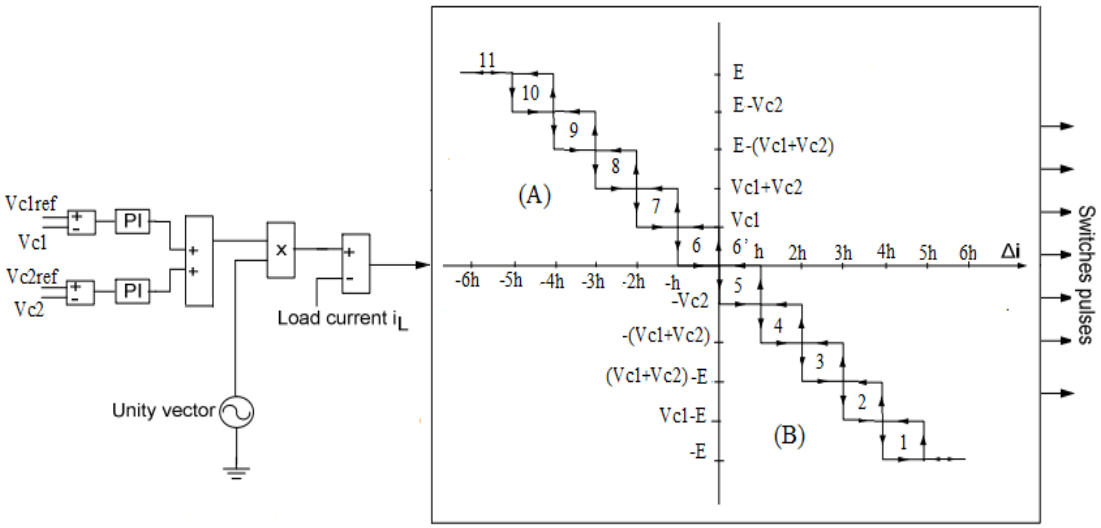


Figure 2. Proposed capacitors voltages balancing technique

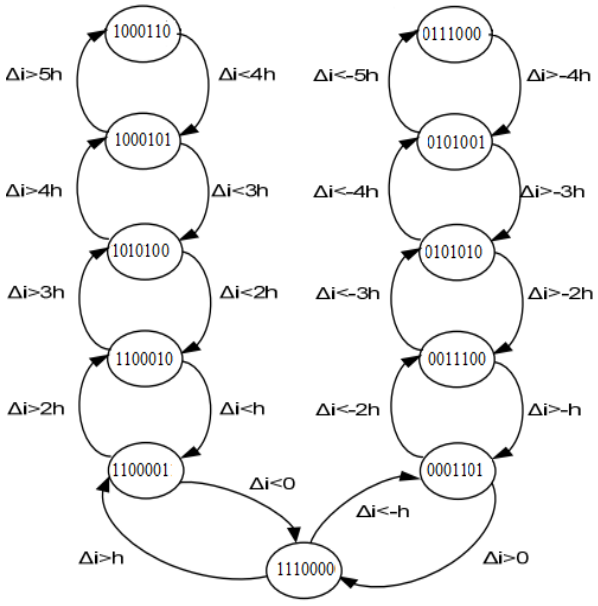


Figure 3. Proposed hysteresis controller

2.2. Nine level SPUC inverter structure, switching states and voltage balancing method

The proposed 9-level inverter was derived from the eleven-level SPUC inverter presented above. However, using closed loop regulation is incompatible with several industrial uses.So, the idea is to decrease voltage levels number, allowing for additional redundant states. These latter are used to guarantee that capacitors voltages self balance without any regulation operation.Assuming that Vc1=Vc2=E/4.Three redundant states which are states 3', 5' 7' are created in addition to the nine required levels operations as is indicated in the Table 2.The three redundant states were produced in the following manner.

- (7):E-(Vc1+Vc2) positive output (first E/2): (S1 is ON), and linked to the positive terminal of the load, while (S3 is ON)+(S5 is ON), and linked to the negative terminal of the load. Capacitor 1 and 2 are charging.
- (7'):Vc1+Vc2 positive output (second E/2): (S1 is ON)+(S2 is ON), and linked to the positive terminal of the load, while (S6 is ON), and linked to the negative terminal of the load. Capacitor 1 and 2 are discharging.
- (5):Zero output (0): (S1 is ON)+(S2 is ON)+(S3 is ON).No effect on capacitor 1 or capacitor 2.
- (5'):Zero output (0): (S4 is ON)+(S5 is ON)+(S6 is ON).No effect on capacitor 1 or capacitor 2.
- (3):–Vc1-Vc2 negative output (first -E/2): (S4 is ON) + (S5 is ON and linked to the positive terminal of the load, while (S3 is ON), and linked to the negative terminal of the load. Capacitor 1 and 2 are discharging.
- (3'):(Vc1+Vc2)-E negative output (second -E/2): (S4 is ON) + (S2 is ON), and linked to the positive terminal of the load, while (S6 is ON), and linked to the negative terminal of the load. Capacitor 1 and 2 are charging.

Table 2 shows the levels that where kept, that decision is based on different situations of capacitors and takes states that according to proposed capacitors voltages balancing technique (Figure 4) they provide nine levels with capacitors voltages self-balancing.

The suggested control strategy is depends on the eight band hysteresis method, when Δi which is the current error is negative, positive voltages are applied (part A in Figure 4).Vice versa, when the Δi is positive, negative voltages are used (part B in Figure 4), Δi presents the real load current minus the current reference. Figure 5 depicts the nine different states and their transition conditions.

Table 2. Switching sequence for the nine-level SPUC inverter

State	Interconnection	Voltage (V)	S1	S2	S3	S4	S5	S6	S7
9	E	400	1	0	0	0	1	1	0
8	E-Vc2	300	1	0	0	0	1	0	1
7'	E-(Vc1+Vc2)	200	1	0	1	0	1	0	0
7	Vc1+Vc2	200	1	1	0	0	0	1	0
6	Vc1	100	1	1	0	0	0	0	1
5	0	0	1	1	1	0	0	0	0
5'	0	0	0	0	0	1	1	1	0
4	-Vc2	-100	0	0	0	1	1	0	1
3	-Vc1-Vc2	-200	0	0	1	1	1	0	0
3'	(Vc1+Vc2)-E	-200	0	1	0	1	0	1	0
2	Vc1-E	-300	0	1	0	1	0	0	1
1	-E	-400	0	1	1	1	0	0	0

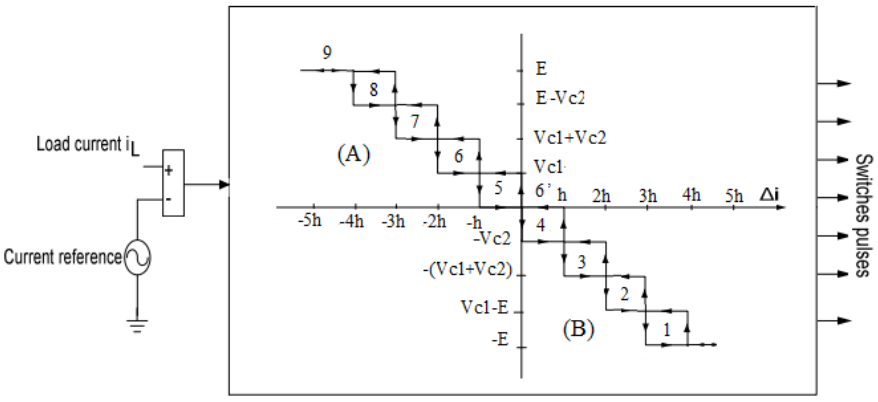


Figure 4. Proposed capacitors voltages balancing technique

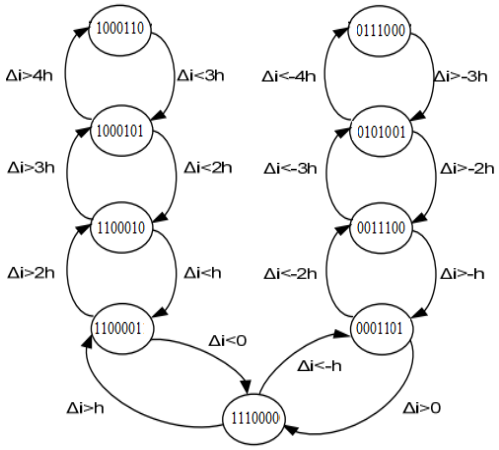


Figure 5. Proposed hysteresis controller

3. RESULTS AND DISCUSSION

Simulation of the proposed eleven level and nine level SPUC inverters was obtained utlizing the MATLAB/Simulink environment. The eleven level SPUC inverter was simulated with constant DC source and load operation. Whereas, simulation of the nine level SPUC inverter was performed in constant and changing load operations, other parameters, including hysteresis bandwidth, remain unchanged.

3.1. Eleven level SPUC inverter

As shown in the Figure 6, the capacitors appear to have attained the appropriate voltage values, thus, Vc1 and Vc2 are maintained exactly on the fifth of the DC source. Figure 7 depicts the voltage and current load waveforms, output voltage of the SPUC inverter proposed is constituted from eleven voltage levels as is presented in Figure 7(a), parameters utilized in the simulation are shown in Table 3.

As presented in Figure 7(b), a nearly sinusoidal load current is achived, it depends on Hysteresis bandwidth. The THD level is very low. Figure 8 displays the load voltage and current harmonics content, it is about 12.21% for the load voltage (Figure 8(a)) and 1.79% for the load current waveform (Figure 8(b)). Reducing the hysteresis bandwidth help to reduce the load current THD.

3.2. Nine level SPUC inverter

The simulation is run under constant and variable load operations to validate the proposed inverter and its balancing algorithm. As well as to demonstrate the high dynamics of the proposed concept, no PI regulators, filters or voltage feed-back are used. All other parameters, including hysteresis bandwidth, stay constant during simulation, capacitors voltages are self-balanced around the desired values.

3.2.1. Constant load and DC source operation

As shown in Figure 9, the capacitors voltages are attained their desired values, thus, Vc1 and Vc2 are maintained around the fourth of DC source, no voltage sensor or closed loop is needed. Figure 10 depicts the voltage and current load waveforms, the output voltage of the inverter proposed, it is constituted from nine voltage levels as is presented in Figure 10(a). A nearly sinusoidal load current is detected as represented in Figure 10(b), parameters utilized in the simulation are shown in Table 4.

The THD level which is very low is obtained without any voltage sensor or regulation loop. Figure 11 displays the load voltage and current harmonics content; we observe a 16.43% for output load voltage (Figure 11(a)) and 1.71% for load current (Figure 11(b)). Reducing the hysteresis bandwidth help to reduce the load current THD.

3.2.2. Changing load operation

To demonstrate the high dynamics of the nine-level SPUC inverter, another simulation is realized. Hence, at t=5 s load resistor value is changed from 60 Ω to 30 Ω ,other parameters keep the same values which are 400 V for DC source voltage and 15 mH for load inductance. As illustrated in Figure 12 capacitors voltages values are balanced after t=5 s. A fast response is detected, (Vc1 and Vc2) are fixed around the fourth of DC source. The voltage load waveform is depicted in Figure 13, it maintains nine levels before (Figure 13(a)) and after (Figure 13(b)) load change. However, Figure 14 displays the current load which appears almost sinusoidal before (Figure 14(a)) and after (Figure 14(b)) load change.

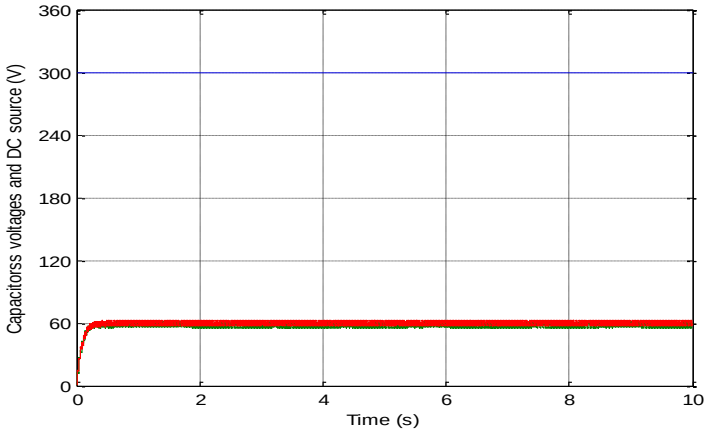
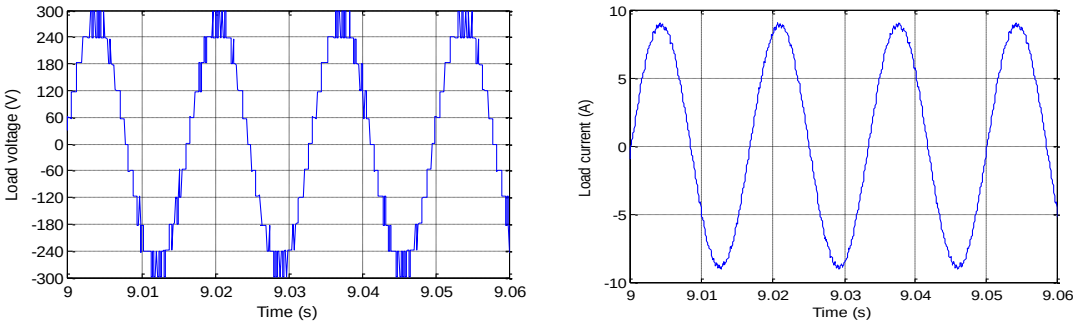


Figure 6. DC source and capacitors voltages

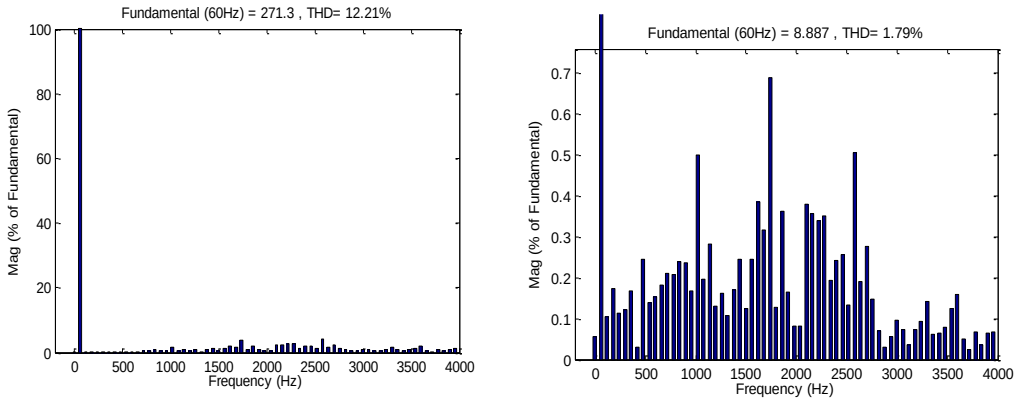


(a) (b)

Figure 7. Load waveforms (a) voltage and (b) current

Table 3. Parameters utilized in the simulation

Parameters	Value
Hysteresis bandwidth	0.25
Voltage source DC	300V
Load resistor	30 Ω
Load inductance	15 mH
SPUC11 capacitors	4 000 µF



(a) (b)

Figure 8. Harmonics content of load (a) voltage and (b) current

Table 4. Parameters for simulation

Parameters	Value
Hysteresis bandwidth	0.25
E (DC source voltage)	400V
Load resistor	30 Ω
Load inductance	15 mH
Auxiliary DC bus capacitor	4 000 µF

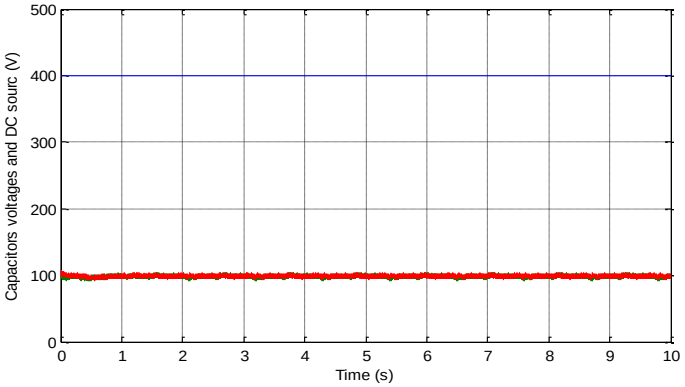
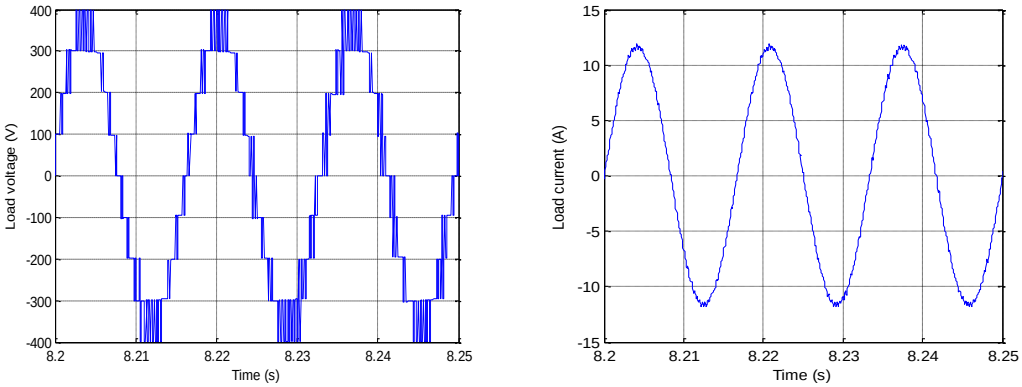
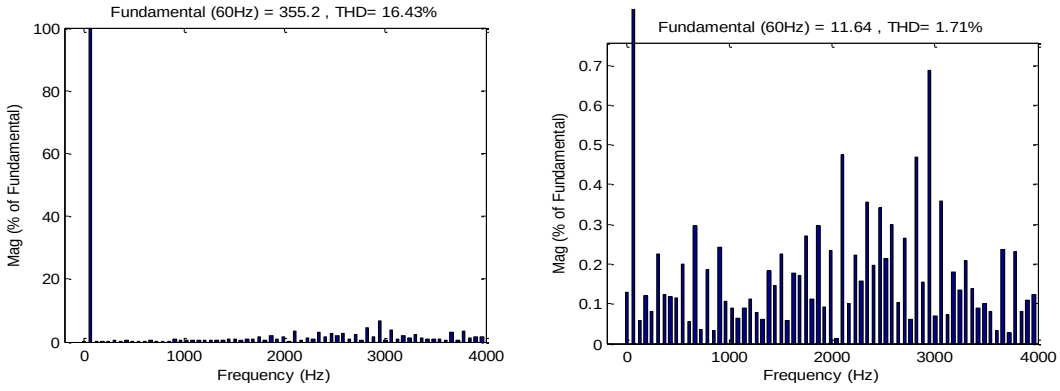


Figure 9. DC source and capacitors voltages



(a) (b)

Figure 10. Load waveforms (a) voltage and (b) current



(a) (b)

Figure 11. Harmonics content of load (a) voltage and (b) current

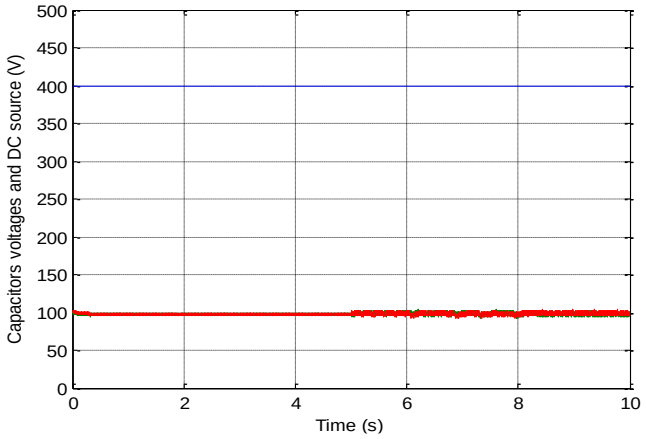


Figure 12. DC source and capacitors voltages

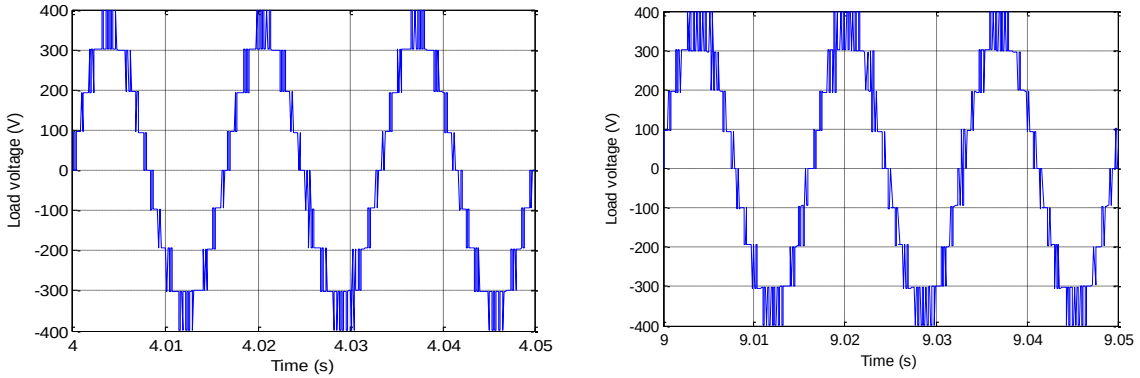


Figure 13. Load voltage waveform (a) before and (b) after load change

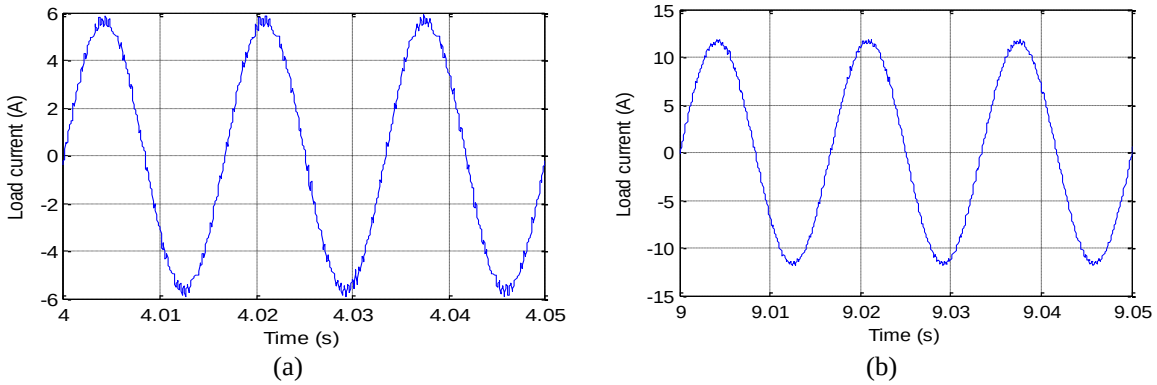


Figure 14. Load current waveform (a) before and (b) after load change

4. CONCLUSION

A novel hysteresis control is applied on the SPUC inverter. The SPUC inverter can offer eleven levels at output voltage, however, a closed loop is used to maintain capacitors voltage at desired values. Another method of control is presented, the later helps to achieve capacitors voltage balancing in open loop operation without using any sensors or regulators, output current is nearly sinusoidal and it can be ameliorated by reducing the hysteresis bandwidth. The high dynamics of the proposed inverter was verified by simulation.

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