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INTERNATIONAL JOURNAL OF ADVANCED RESEARCH (IJAR)

Article DOI:10.21474/IJAR01/15539
DOI URL: http://dx.doi.org/10.21474/IJAR01/15539

RESEARCH ARTICLE

SYNTHESIS AND FPGA VALIDATION OF PARALLEL PREFIX ADDERS

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Manuscript Info

Manuscript History
Received: 19 August 2022
Final Accepted: 23 September 2022
Published: October 2022

Key words:-
KSA, CSKA, CLA, RCA, HDL, Xilinx Vivado, Cadence Genus

Abstract

In this work, the design implementation, functionality testing, design synthesis and bitstream generation of various n-bit adder architecture of RCA, CLA, CSkA and KSA. And addresses various forms of adders which include Ripple-carry (RCA), Carry-lookahead (CLA), Carry-skip (CSkA), and Kogge-stone (KSA) adders. Certain design restrictions for digital VLSI circuits, such speed and area, can be satisfied using these adders. All the mentioned adder are designed using Verilog HDL, implemented the same on Xilinx Vivado 2018.2, functionality test is carried out by writing testbench, bitstream generated for the same and synthesized using Cadence genus.

Introduction:-

In any Digital circuit adders are the basic building blocks. In processor, ALU (arithmetic logic unit) is the component uses the adder as its building block, since addition, subtraction, multiplication and division all these operations require adders only. Adding to the list of its application, decoders such as binary to octal, binary to decimal and binary hexa-decimal, encoders such as octal to binary, decimal to binary, hexa-decimal to binary, complemented number representation and multiplexers uses adders in one or the other way.The following constraints are majorly concerned in the digital design:

1. Low power design.
2. Portability.
3. Delay.
4. Cost or combination of all.

All above mentioned constraints cannot be fulfilled by the single adder implementation, most of the time adder selected based on user's requirement. The comparative analysis of 4-bit, 8-bit, 16-bit, and 32-bit of adder has done which helps in selection of adder for the user design constraints. The work is inspired by [2], where they implemented different full adder technology and cascaded for higher bit adder using schematic in cadence virtuoso. Authors also have done the pre-layout and post-layout simulation. This work includes, the comparative analysis of KSA with different adders, which includes designing using Verilog, functionality testing by wring test benchfor thedesign, generating bit stream for FPGA validation and synthesizing the design, for constraints comparative analysis. Below is the list are the adders considered for work:

1. Ripple – Carry Adder
2. Carry - Lookahead Adder

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3. Carry - Skip Adder
4. Kogge Stone Adder

Theflow of work is divided as follows: II Adders: explained the adders which used in this work, III Simulation and Results, IV Conclusion: outcome of the work.

Adders

a. RCA

Ripple Carry Adder (RCA) is designed by cascading the full adders. Full adder design in Verilog uses two half adders and OR gate, half adder consists of one XOR gate and AND gate. Ripple carry adder uses n - full adders for n- bit adder. Fig 1 shows the 4 - bit Ripple carry adder Design, A3-A2-A1-A0 (first operand) and B3-B2-B1-B0 (second operand) as inputs and produces outputs as S3-S2-S1-S0 (sum) and C4(carry). The carry in (c0) can be taken as either 1 or 0 depending on previous stage carry output. Carry output of first stage (full adder) is give as carry in to next stage (full adder). Since the last stage (full adder) carry out is evaluated only when its preceding stages completes its operation, so delay is more.

$$SUM = A \oplus B \oplus Cin \quad (1)$$

$$Cout = (A.B) + (B.Cin) + (C.inA) \quad (2)$$

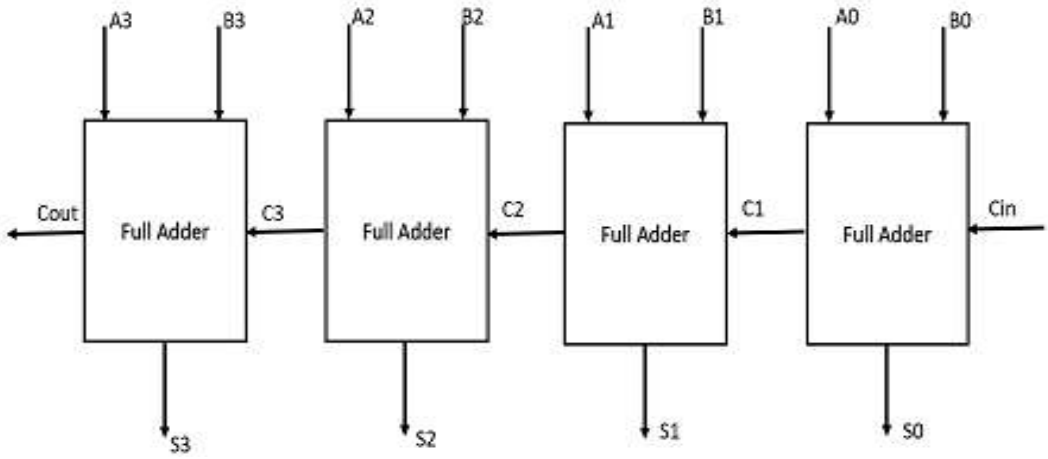

Fig.1:- Design of 4-bit RCA.

b. CLA

Carry Look Ahead (CLA) is having less delay compared to the RCA. The analogy used in CLA to increase speed is that this adder having additional block called look ahead logic. Here generation bit and propagation bit generated parallelly with respect to the full adder sum generation, which are used to evaluate the carry out of the circuit. So no need to wait for preceding full adder to completes its evaluation for carry out. .

Fig 2 shows the design of CLA. Here sum is generated using the Full Adder and Carry out is generated using look ahead logic which contain the circuit to generate the propagation and generation bit by following the below equations.

$$Gi = Ai.\ Bi \quad (3)$$

$$Pi = Ai \oplus Bi \quad (4)$$

$$Si = Pi \oplus Ci \quad (5)$$

$$C+1 = Gi + (Pi.\ Ci) \quad (6)$$

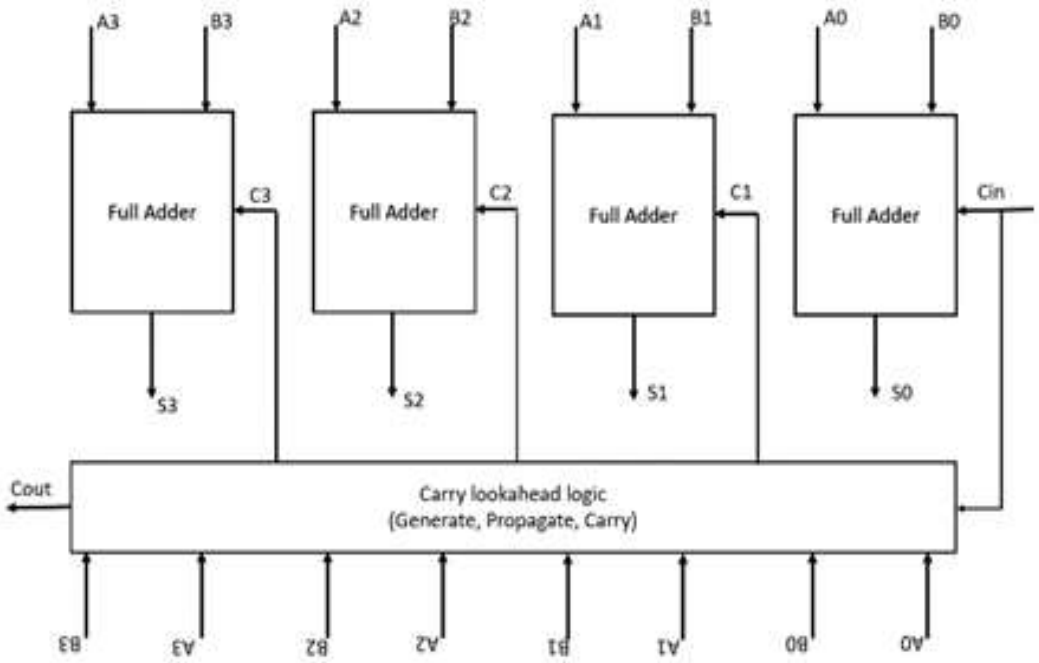

Fig.2:- Designof 4-bit CLA.

c. CSkA

Carry Skip Adder (CSkA) is also known as the bypass adder because it uses the bypass block in its design. Bypass circuit is nothing but the 2:1 multiplexer and 4-input AND gate. When propagation term is high for all the bits, Cout = Cin, otherwise Cout = Cn (last bit carry out). For higher bits, cascading of 4-bit CSkA is done.

Fig 3 show the design of 4-bit CSkA. Similar to RCA here sum and carry evaluation will done but parallelly generating the propagation bit for every bit. Propagation bit is generated parallelly with sum evaluation. When the sum evaluation is completed, mux will decide should is bypass Cin as Cout or not with the help of select-line which is output of AND gate. It will not provide the speed of CLA but definitely higher speed or lesser delay than RCA. Consume the less area and power compared to the CLA, more hardware compared the RCA. CSkA used as 4-bit cascading blocks for higher bit adder implementation.CSkA speed is high but area utilization is more comparatively other adder.

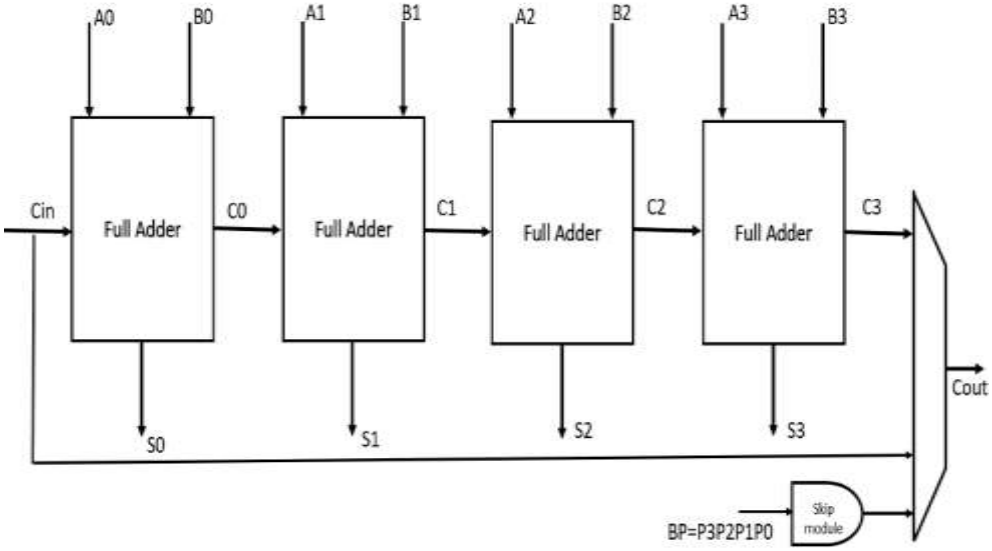

Fig.3:- Design of4-bit CSkA.

d. **KSA**

Kogge Stone Adder (KSA) is one of fastest adder and parallel prefix adder. KSA does not uses the full adder for its addition evaluation. KSA require more power and area but gives the higher speed compared to other adders. And also, at higher bit addition it compensates the it's area and power consumption compared to other adders. Fig 5, shows the design of 4-bit KSA. KSA do its evaluation in three stages namely pre-processing stage, carry generation stage and final processing stage. In the pre-processing stage generation and propagation bits. In the carry generation stage, it generates intermediate generation and propagation bits by using previous stage outputs. In the final processing stage sum and carry is generated. All three stages formula is listed below:

A. Pre-processing stage:

$$Pi = Ai \oplus Bi \quad (7)$$
$$Gi = Ai.\ Bi \quad (8)$$

B. Generation of carry:

$$Gi = (Pi\ .Gi^*) + Gi \quad (9)$$
$$Pi = (Pi.\ Pi^*) \quad (10)$$

C. Final processing stage:

$$Ci = Gi \quad (11)$$
$$Si = Pi \oplus Ci\text{-}1 \quad (12)$$

Where '*' represents the previous value

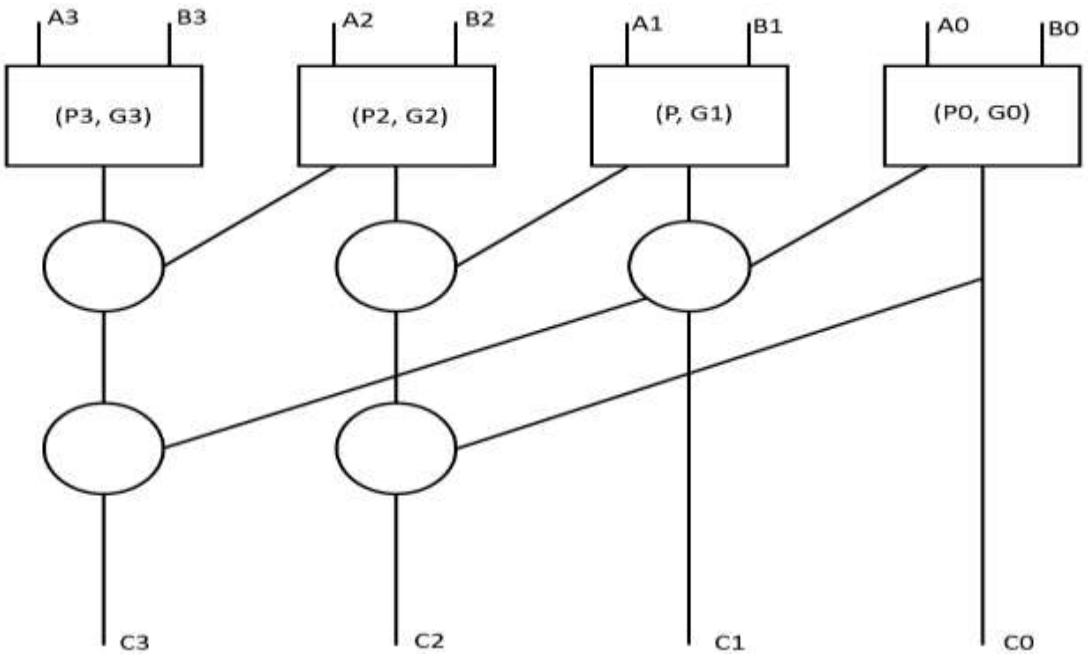

Fig. 4:- Design of 4-bit KSA.

Simulation and results

Functional Verification has been done by using Xilinx Vivado 18.3 using Verilog and bit stream generated for the same. Synthesize the design using Cadence genus.

e. Ripple Carry Adder

The RCA has been designed using full adder for 4-bit and, 8-bit, 16-bit and 32-bit design by instantiating the 4-bit design.

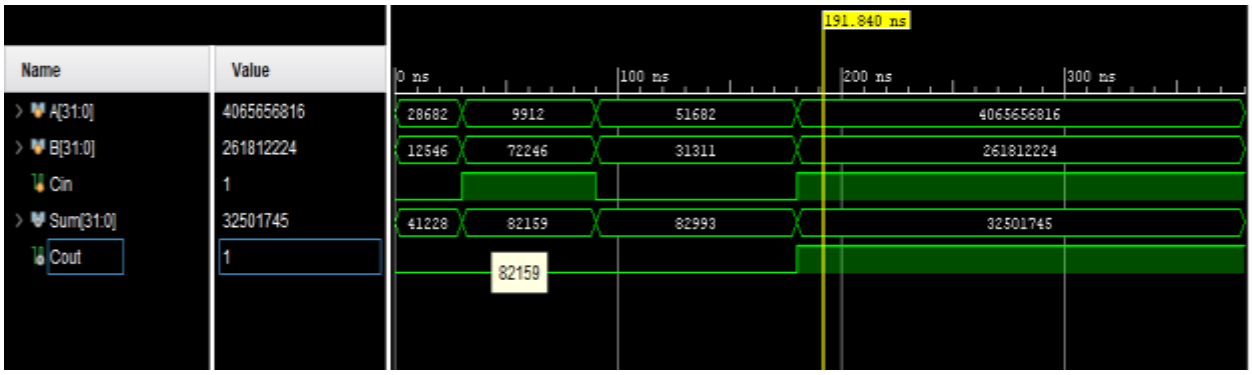

Fig 5:- Simulation of 32-bit RCA.

The Fig 5 shows the simulation of 32-bit Ripple carry adder with the A, B, Cin, Sum and Cout value shown in the table 1. Results are viewed in decimal number system.

Table 1:- Input and output values of 32-RCA.

A	B	Cin	Sum	Cout
4065656816	261812224	1	32501745	1

Fig 6 shows the synthesized schematic of 32-bit RCA which is instantiated using 4-bit RCA, using cadence genus tool.

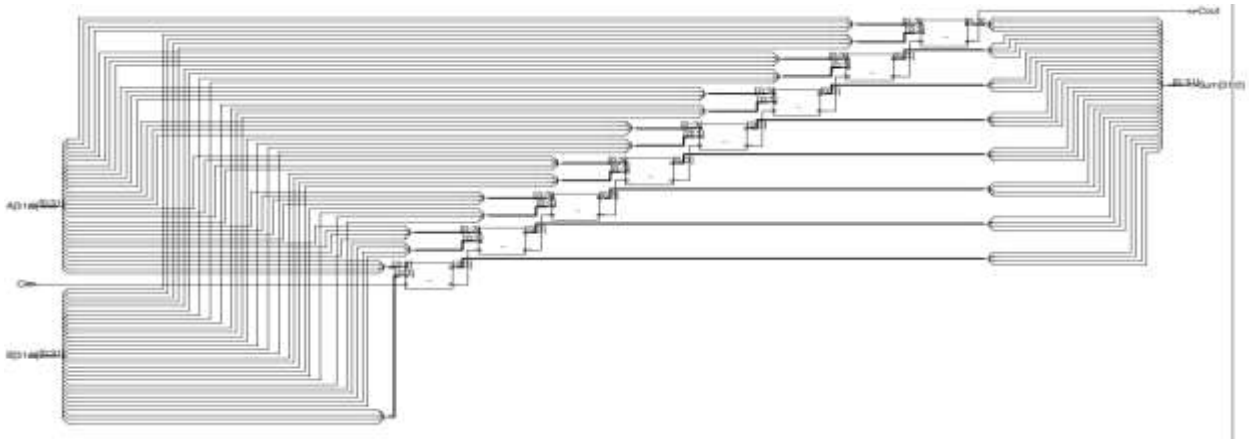

Fig 6:- Schematic of 32-bit RCA.

f. Carry Lookahead Adder

The CLA has been designed using full adder and lookahead block for 4-bit and, 8-bit, 16-bit and 32-bit design by instantiating the 4-bit design.

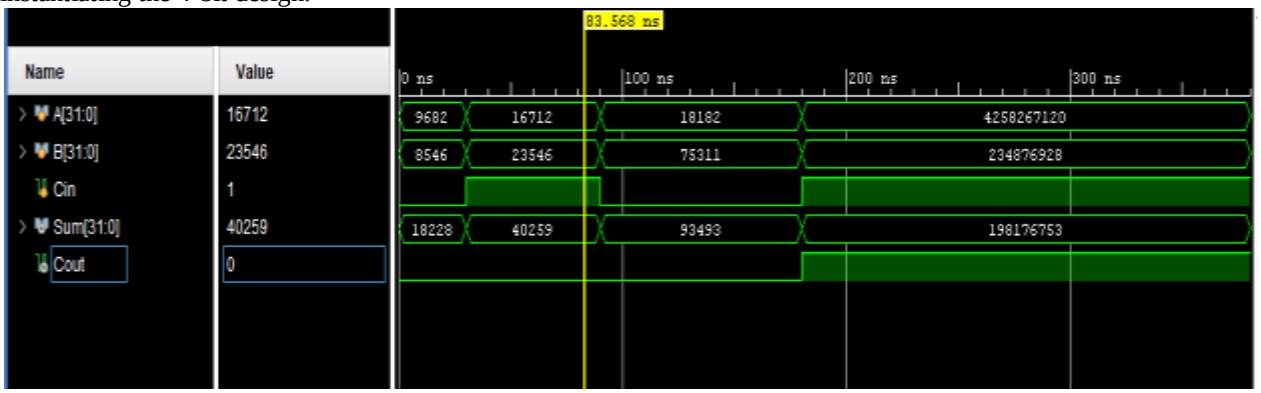

Fig 7:- Simulation of 32-bit CLA.

The Fig 7 shows the simulation of 32-bit Carry lookahead adder with the A, B, Cin, Sum and Cout value shown in the table 2. Results are viewed in decimal number system.

Table 2:- Input and output values of 32-CLA.

A	B	Cin	Sum	Cout
16712	23546	1	40259	0

Fig 8 shows the synthesized schematic of 32-bit CLA which is instantiated using 4-bit CLA, using cadence genus tool.

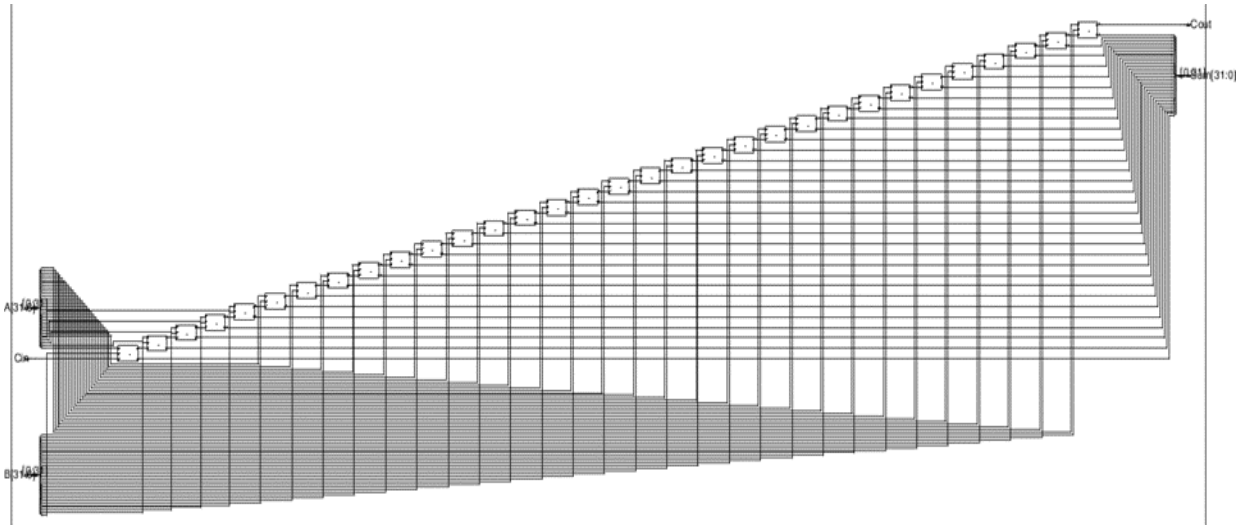

Fig 8:- Schematic of 32-bit CLA.

g. Carry Skip Adder

The CSkAhas been designed using full adder, multiplexer and skip module for 4-bit and, 8-bit, 16-bit and 32-bitdesign by instantiating the 4-bit design

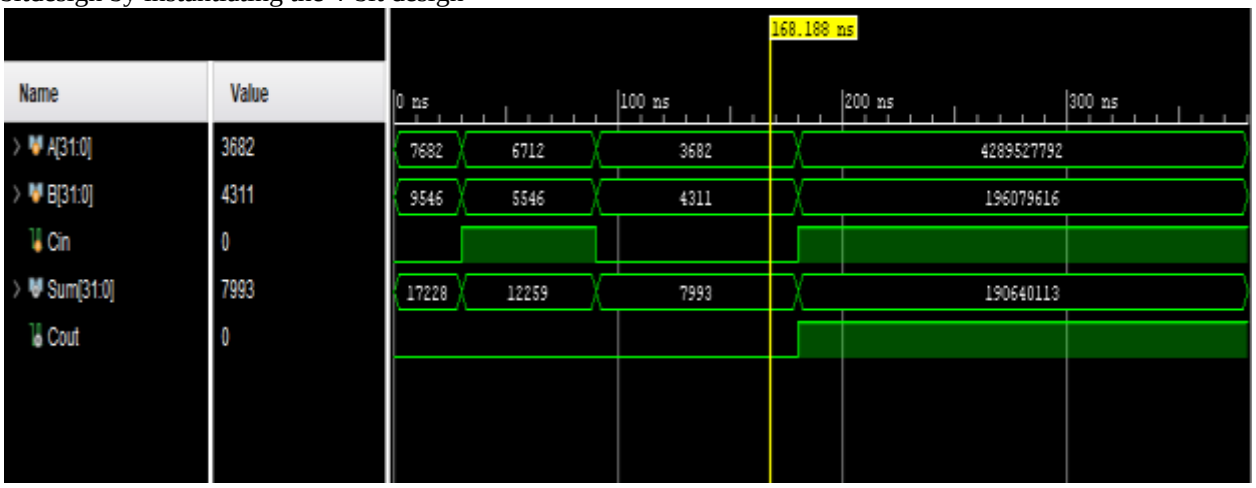

Fig 9:- Simulation of 32-bit CSkA.

The Fig 9 shows the simulation of 32-bit Carry skip adder with the A, B, Cin, Sum and Cout value shown in the table 3. Results are viewed in decimal number system

Table 3:- Input and output values of 32-CSkA.

A	B	Cin	Sum	Cout
3682	4311	0	7993	0

Fig 10 shows the synthesized schematic of 32-bit CLA which is instantiated using 4-bit CLA, using cadence genus tool.

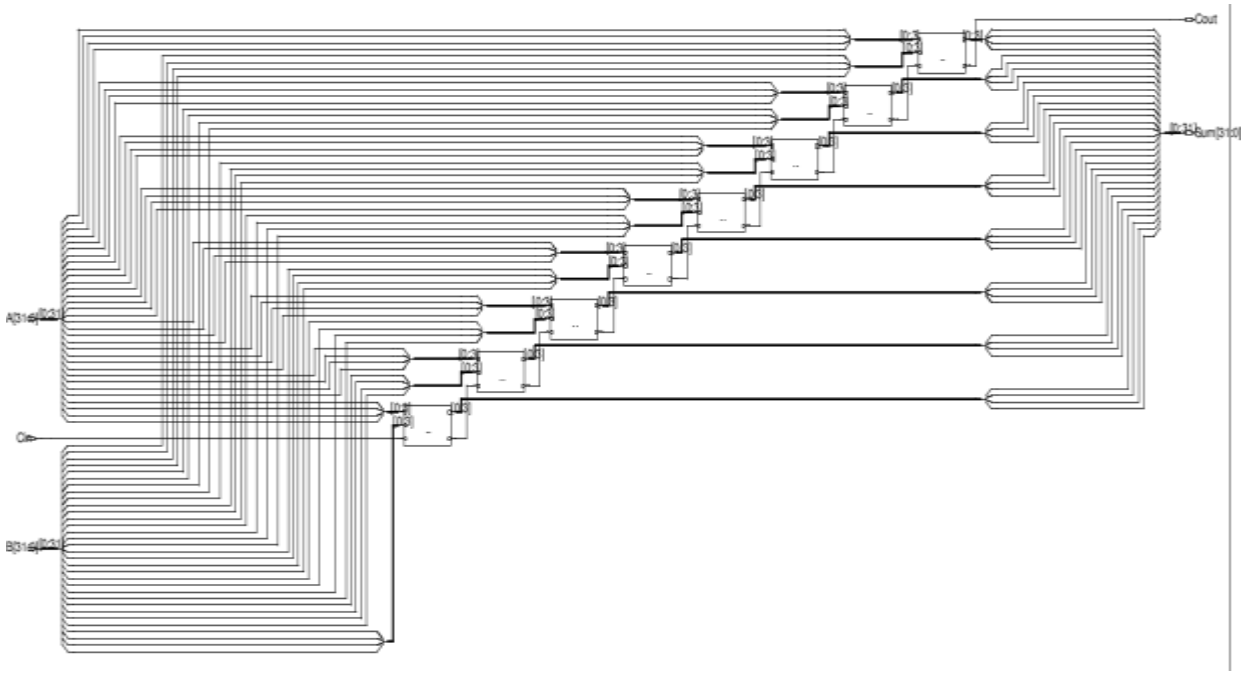

Fig 10:- Schematic of 32-bit CSkA.

h. Kogge Stone Adder

The KSA has been designed using propagate-generate module and basic gates with the help of KSA equations for 4-bit, 8-bit, 16-bit and 32-bit design.

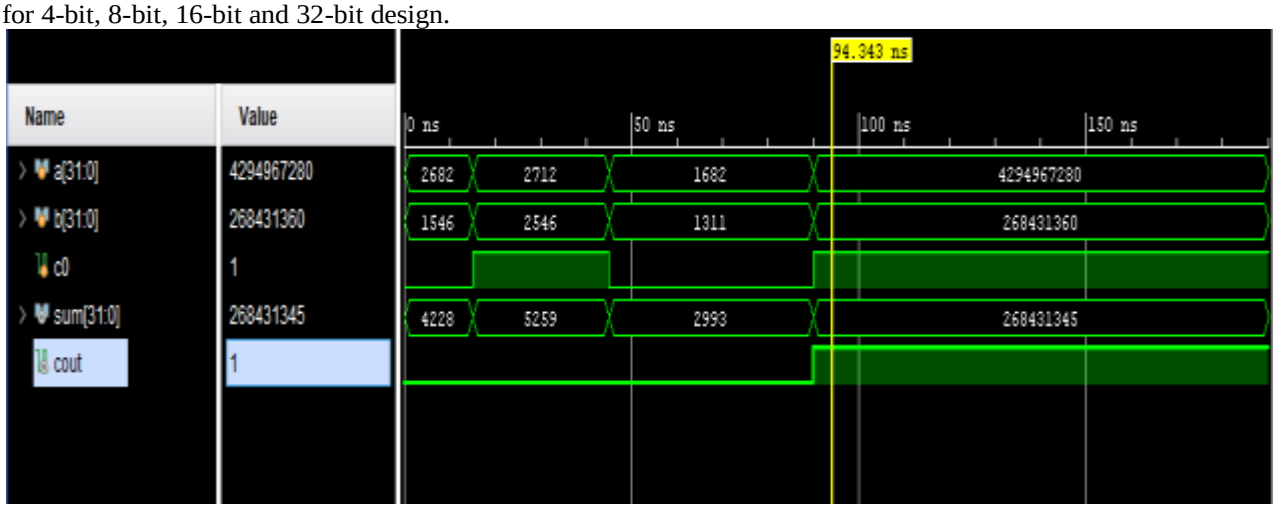

Fig 11:- Simulation of 32-bit KSA.

The Fig 11 shows the simulation of 32-bit Carry skip adder with the A, B, Cin, Sum and Cout value shown in the table 4. Results are viewed in decimal number system.

Table 4:- Input and output values of 32-KSA.

A	B	Cin	Sum	Cout
4294967280	26431360	1	268431345	1

Fig 12 shows the synthesized schematic of 32-bit KSA which is designed without using full adder module, in cadence genus tool

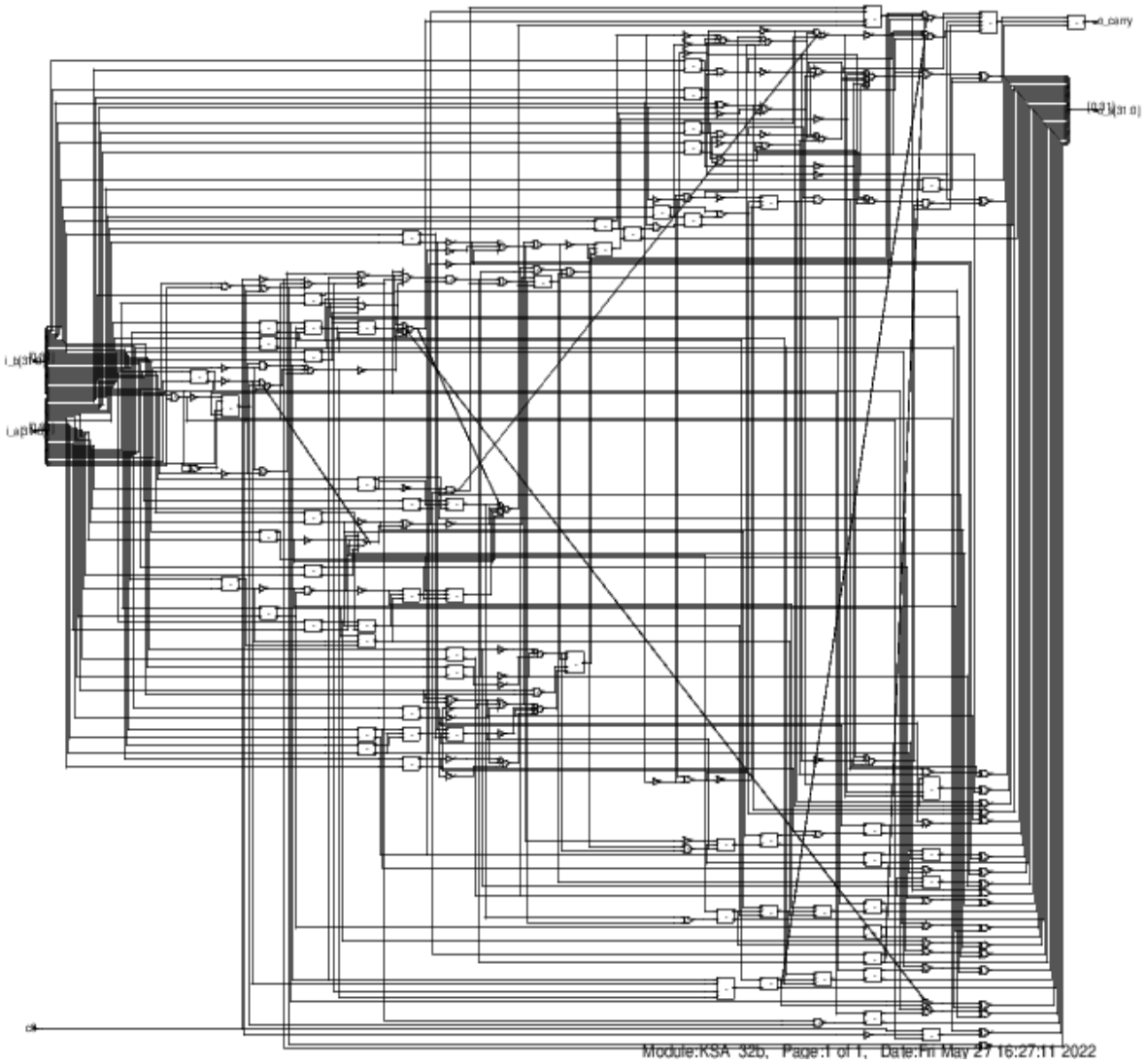

Fig 12:- Schematic of 32-bit KSA.

Table 5 shows the comparison of different adder with respect to power and number of logic cell utilization.

The evaluation was made using Cadence genus 45nm technology. From the table, we can be seen that RCA consume less power but when the higher bit application KSA gives higher speed with almost same power consumption.

Table 5:- Comparison of Adders with respect to number of inputs.

Logic Design	Number of cells	Total power(nw)
RCA (4-bit)	4	2370.9
RCA (32-bit)	32	23006.5
CLA (4-bit)	4	1056.4
CLA (32-bit)	32	10142.04
CSKA (4-bit)	4	1370.9
CSKA (32-bit)	72	8580.5
KSA (4-bit)	5	2005.1
KSA (32-bit)	196	29413.4

Table 6 shows the comparison of different adder with respect to Area vs Performance vs Power consumption of adders (for higher bits)

Table 6:- Comparison of Adders.

Logic Design	Area	Speed	Power consumption
RCA	Moderate	Less	Moderate
CLA	High	Moderate	Less
CSKA	High	Moderate	Less
KSA	Moderate	Good	Moderate

Fig 13 shows the comparison of different adder with respect to power delay product and number of input bits. At lower bits RCA look good, but for higher bits KSA yields good result

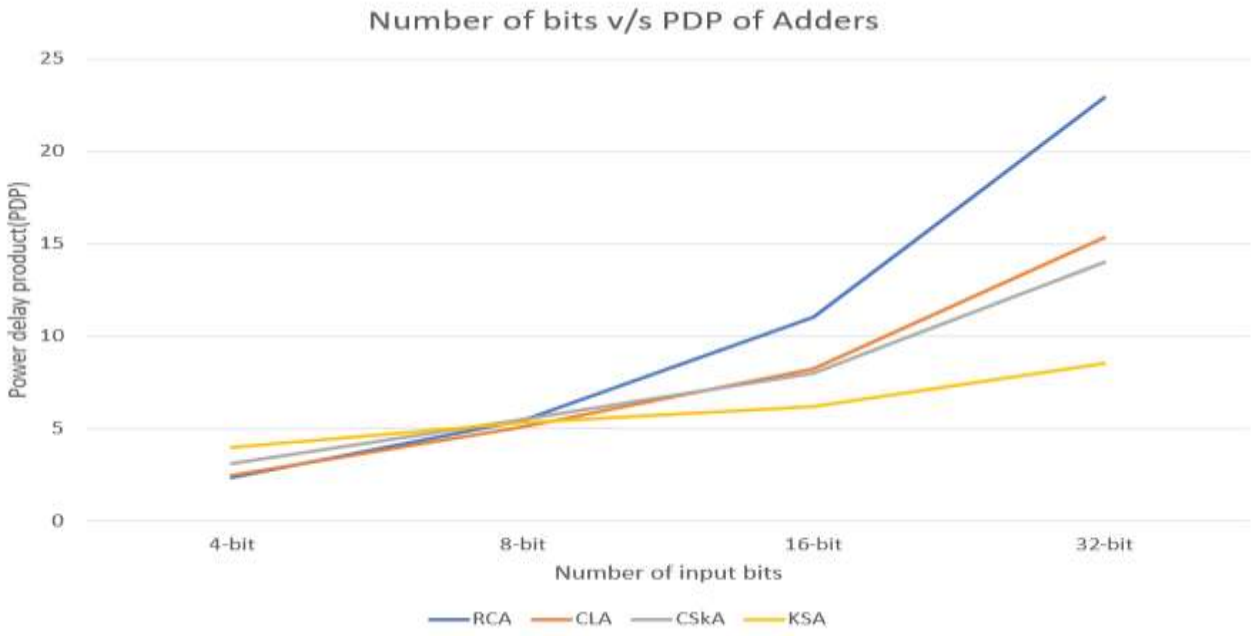

Fig 13:- Comparison graph of different adder.

Conclusion:-

In thiswork, The Adder's design has been done using Verilog HDL are independent of technology, very easy for designing and debugging and are normally more useful than schematics particularly for large circuits.Every adder design is done for 4-bit, 8-bit, 16-bit and 32-bit, and the functionality verification is done for the same.The bitstream has been generated for all Parallel Adder designs using Xilinx vivado 2018.2 design suite and the same bitstream can be loaded onto any FPGA board to verify its functionality.The RTL schematic and synthesis reports has been generated using Genus with 45nm Technology for various n-bit Parallel adders such as RCA, CLA, CSkA and KSA are done. Kogge Stone Adder is a high-speed adder with moderate power consumption

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