Grant Agreement No: 101004761

AIDAinnova

Advancement and Innovation for Detectors at Accelerators

Horizon 2020 Research Infrastructures project AIDAINNOVA

MILESTONE REPORT

Completion of planar sensor production for ACF

MILESTONE: MS24

Document identifier:	AIDAinnova-MS24
Due date of milestone:	End of Month 18 (September 2022)
Report release date:	30/10/2022
Work package:	WP6: [Hybrid pixels sensors for 4D Tracking and Interconnection Technologies]
Lead beneficiary:	[CNRS]
Document status:	Final

Abstract:

Planar sensors and dedicated test structures are necessary for a precise characterisation of the ACF bonding developed in the framework of the Task 6.4 (WP6) of AIDAInnova. This document reports on the production and availability of such devices and the completion of MS24 in Month 18.

The Advancement and Innovation for Detectors at Accelerators (AIDAinnova) project has received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement no. 101004761. AIDAinnova began in April 2021 and will run for 4 years.

Delivery Slip

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Executive summary

Anisotropic Conductive Films (ACF) represent a flexible and cost-effective industrial solution for die-to-die electrical interconnection. Task 6.4 includes the development and validation of ACF bonding for pixel detector at future colliders, including the production of dedicated sensors and daisy-chain devices which have been produced by FBK Trento. The devices are implemented using a single patterned metal layer on top of the 6-inch quartz substrate of 625μm thickness.

The layout and thickness of the metal and passivation layer mimics the matrix size, pitch and topology of various target ASICs and sensors (Timepix3, CLICpix2, RD53). Devices with larger pads and low pad density are also implemented to test ACF module integration. The routing between the pads allows for electrical measurements of the connectivity and contact resistance in various configurations.

A lot of eight wafers have been produced.

1. INTRODUCTION

Small-pitch hybrid pixel detectors produced with a number of traditional bump-bonding technologies such as solder or indium, or in some cases even more advanced techniques (for instance transient liquid or metal direct bonding), are widely used in current HEP experiments and planned in future ones. The cost of the complex metallization and interconnect processing, performed in highly specialized foundries, dominates the production cost per unit area, and the need to process whole readout wafers dominates the prototyping costs. New cheaper technologies are being developed to mitigate this constraint. Recent progress was made in industrial applications of Anisotropic Conductive Films (ACF) for multiple interconnect solutions. The resulting process flow will constitute a large simplification of the bonding process, reducing cost per flip-chip placement and removing the constraint of having to process full readout wafers. Prototyping and production of hybrid assemblies with ACF can therefore be performed with standard flip-chip equipment available in many institutes within the HEP community.

ACF are composed of microscopic conductive particles suspended in an adhesive matrix. Thermocompression of the ACF between two conductors results in a permanent attachment and a reliable electrical connection only in the direction of the compression. Today, ACF is the dominating interconnect technology for displays (LCD and OLED) and is widely used also in many other applications such as camera modules and RFID manufacturing. For the application in HEP pixel detectors, critical parameters such as bonding force, adhesive film thickness, conductive particle (CP) material and diameter and density of CPs need to be developed for the specific layout and topology of the respective sensors and readout ASICs.

Task 6.4 of AIDAInnova includes the study and development of interconnections by means of ACF and is a synergy between research institutions and industry. A few different readout chips are available in the community and have already started to be tested in this Task, using different coverage areas and pixel pitch. A few prototypes have been built, and the interconnection quality has been tested with radioactive sources and at test-beam facilities. The objective is now a more quantitative and systematic evaluation of the interconnection yield, as a function of the area, the pitch size and other parameters such as the post-process technology or the pressure used during the assembly. This will include reliability tests, for example after thermal cycles or irradiation. The systematic characterisation study is based on two classes of objects: dedicated sensor productions and conductive chain devices.

2. VALIDATION OF INTERCONNECTION PERFORMANCE

2.1. DEDICATED SENSOR PRODUCTIONS

A first possibility to have a quantitative and precise assessment of the ACF interconnection yield is to use specific sensor productions matched to the available readout chips. In Task 6.4, dedicated sensors have been made available by participating institutes through synergies with parallel or previous productions. In particular, several sensor types featuring a pitch ranging from 25µm to 55µm and corresponding to some available readout chips (TimePix, ClicPix, RD53) have been shared. Sensors built in a previous submission made by one of the participating institutes (CNRS-LPNHE Paris) in the framework of AIDA-2020 have been collected. The production, in collaboration with FBK Trento [1], used wafers of 50µm, 100µm and 130µm active thickness, thus allowing to probe also the behaviour of ACF for different sensor thicknesses.

2.2. PRODUCTION OF SPECIFIC CONDUCTIVE CHAIN DEVICES

Even if the sensor typologies described in 2.1 are realistic examples of the possible application of ACF for interconnection of sensors to readout chips used in HEP detectors, they are not the best suitable devices to measure precisely the quality of the interconnection and the obtained yield. Dedicated devices featuring conductive chains represent a more powerful tool to obtain a higher precision and a better understanding of the general behaviour of the interconnection film. A production of such devices has been organised in Task 6.4 in collaboration with FBK Trento.

The principle of conductive chains is shown in Fig. 1. A long metal connection is subdivided in conductive segments which are deposited following an alternate pattern on the surface of the two facing dies. When the two dies are flip-chip bonded, the sequence of segments reconstructs the full long line. If one of the electrical connections between the two dies fails, the line is interrupted and a conductivity test can spot the failure. Additional test-pads along the line allow to test partial portions in case of multiple failures.

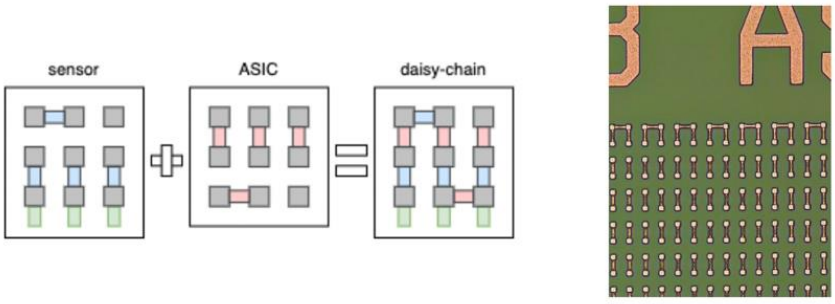

Fig. 1 The principle of Conductive Chains: a single long connection is subdivided in segments which are alternated on the surface of the two facing dies. When the two dies are flip-chip bonded, the sequence of segments reconstructs the full long line. A picture of one of the produced dies is shown on the right.

The testing chains are realised as a single metal layer deposited at FBK on silicon or quartz wafers. In this production, eight 6'' quartz wafers of 625 µm thickness were used. The layout includes one

or several pairs of matching devices per wafer so that after dicing even a single wafer has enough dies to test each device type.
The layout and a picture of one of the produced wafers are shown in Fig. 2.

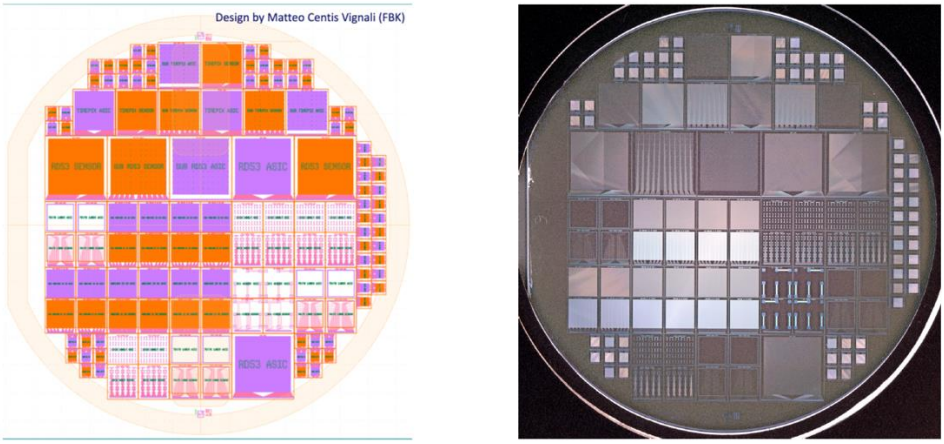

Fig. 2. Layout and photo of one wafer of the conductive chains production

The choice of devices has been made to represent the topologies of some of the most common ASICs presently in operation: CLICpix2, Timepix3, RD53, in addition to a number of larger pitch devices for tests of chip-to-flex interconnections for module integration. For most designs, more than one pair of devices are present in the layout. A summary of the different flavours is summarised in Table 1.

	pitch	size in mm	connections	per wafer	type
160x160 20um	20 um	3.2 x 3.2	25600	36	grid
CLICpix2	25 um	3.2 x 3.2	16384	34	grid
400x400 25um	25 um	20 x 20	640000	5	grid
Timepix3	55 um	14 x 14	65536	4	grid
Timepix3 islands	55 um	14 x 14	65536	4	grid
RD53	50 um	20 x 20	160000	4	grid
RD53 islands	50 um	20 x 20	160000	2	grid
70x70 140um	140 um	20 x 20	2112	3	peripheral
10x10 1000um	1000 um	20 x 20	400	3	grid
3x3 4500um	4500 um	20 x 20	36	1	grid

Table 1. Content of the conductive chains wafer layout

Different typologies of test structures are used, to probe different aspects of the interconnectivity. The baseline design is represented by the classic conductive chain, featuring a serpentine across the die, connecting the very first readout pad (input) with the very last (output). To improve the sensitivity, each column can be probed independently through intermediate readout pads. In order to be sensitive to different ranges of failure rates in the interconnection, an improvement in the design was introduced in the standard conductive chains. Blocks of columns feature an increasing density of openings across the dies (see Fig. 3). The first few blocks present very few openings and are thus suitable to estimate the failure rate in presence of a high number of expected defects. The number of openings increases in neighbouring blocks, thus allowing to probe more reliable interconnection

conditions, where the probability of intercepting a defect in at least one of the openings becomes lower.

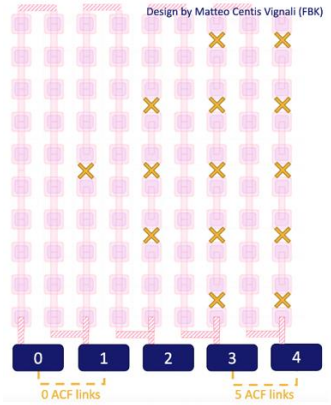

Fig. 3. Classical design used for probing the interconnection yield. The first (input) readout pad and the last (output) one, at the other side of the device and not included in the picture, can be tested for connectivity to compute the probability that a defect is present and breaks the continuity of the line. In addition, an intermediate readout pad is connected to each bottom-of-column, thus allowing to probe different portions of the full chain. The density of openings increases across the devices to allow the probing of different ranges in terms of interconnection failure rates.

The bottom-of-column points are fan-out with metal lines to a set of readout pads, organised in a double-row. They reach an inter-pitch larger than the one of the pixels in the device, thus allowing the readout via wire-bonds or micro-probes, which would be challenging to achieve with smaller pitches.

In the flip-chip of sensors and FE electronics, especially for large surfaces, the interconnectivity yield is not uniform across the die, and more critical regions present defects or delamination, often along the borders or in the corners. To address the possibility of studying such effects, a second class of structures has been designed. In this case, instead of a unique serpentine across the different columns, different macro-regions of the die are probed with dedicated serpentine blocks, see Fig. 4.

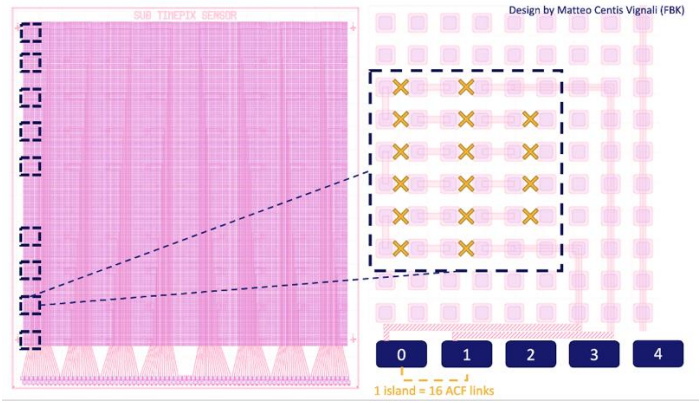

Fig. 4. Test structure dedicated to the study of defects in specific regions of the flip-chip die.

Each ‘island’ features an independent serpentine connected to the bottom readout pads by direct metal lines. In this way it is possible to map the interconnection failure rate in different regions of the die.

Some of the devices also feature very large pitch size mimicking readout and powering pads on ASICs. They will be used to test chip-to-flex interconnection for module integration with ACF or other interconnection technologies, such as conductive glue dots.

Some of these test devices have a peripheral structure where the serpentine runs at the perimeter of the die, realizing the connections only in this region. These structures might be used to test interconnection with ACF or other technologies, which could be used as an alternative to the wirebonding.

It is also worthwhile to mention that special studies have been done during the design phase of these conductive chains, to tune the thickness and the height of the metal in the pixel regions in order to present realistic conditions able to mimic the typical metal structure of pads of sensors (after post-processing such as under-bump-metallization, UBM) and of readout electronics. A thickness of 2.5μm has been used for the metal, and 950 nm for the passivation.

Eight quartz wafers have been produced by FBK Trento during the first year of the AIDAInnova project. Two of them are already at CERN for preliminary studies. Two more will be diced to be used in tests with ACF to progress with die-to-die connection. Some will be kept un-diced for studies of technologies which require wafer-level processing, such as the deposition of standard UBM.

3. REFERENCES

[1] Fondazione Bruno Kessler, Trento, Italy

ANNEX: GLOSSARY

Acronym	Definition
ACF	Anisotropic Conductive Film
UNM	Under Bump Metallization