Design of an efficient binary phase-shift keying based IEEE 802.15.4 transceiver architecture and its performance analysis

Vivek Raj Kempanna[1], Dinesha Puttaraje Gowda[2]
[1]Department of Electronics and Telecommunication Engineering, Dayananda Sagar College of Engineering, Bengaluru, India
[2]Department of Electronics and Communication Engineering, Dayananda Sagar College of Engineering, Bengaluru, India

Article Info

ABSTRACT

The IEEE 802.15.4 physical layer (PHY) standard is one of the communication standards with wireless features by providing low-power and low-data rates in wireless personal area network (WPAN) applications. In this paper, an efficient IEEE 802.15.4 digital transceiver hardware architecture is designed using the binary phase-shift keying (BPSK) technique. The transceiver mainly has transmitter and receiver modules along with the error calculation unit. The BPSK modulation and demodulation are designed using a digital frequency synthesizer (DFS). The DFS is used to generate the in-phase (I) and quadrature-phase (Q) signals and also provides better system performance than the conventional voltage-controlled oscillator (VCO) and look up table (LUT) based memory methods. The differential encoding-decoding mechanism is incorporated to recover the bits effectively and to reduce the hardware complexity. The simulation results are illustrated and used to find the error bits. The design utilizes less chip area, works at 268.2 MHz, and consumes 108 mW of total power. The IEEE 802.15.4 transceiver provides a latency of 3.5 clock cycles and works with a throughput of 76.62 Mbps. The bit error rate (BER) of 2×10^{-5} is achieved by the proposed digital transceiver and is suitable for real-time applications. The work is compared with existing similar approaches with better improvement in performance parameters.

Corresponding Author:

Vivek Raj Kempanna
Electronics and Telecommunication Engineering, Dayananda Sagar College of Engineering
Bengaluru, Karnataka, India-560078
Email: vivekgowda1990@gmail.com

1. INTRODUCTION

IEEE 802.15.4 physical layer (PHY) is a prominent wireless communication protocol used to provide connectivity between nearby devices in wireless personal area network (WPAN) applications such as healthcare, smart grid, industry automation, and control appliances [1]. PHY and medium access control (MAC) layers are used in the IEEE 802.15.4 standard for low cost, low-data-rate and low-power short range communication. In terms of power consumption, device size, and battery life, WPAN applications implementing 802.15.4 encounter numerous obstacles. The 802.15.4 standard uses two frequency bands for operation: 868/915 MHz and 2.4 GHz. These two bands allow for less data transmission between nodes in the WPAN. The 868/915 MHz frequency band PHY transceiver is suitable and enables a longer range within the time restriction and control link [2].

IEEE 802.15.4, ZigBee module, the International Society of Automation (ISA) 100 protocol, and WirelessHART are the key sources for WPAN applications that enable distinct intrinsic solutions with time and frequency variations. With a few technologies such as direct sequence spread spectrum (DSSS),

frequency division multiple access (FDMA), carrier sense multiple access (CSMA), and time-division multiple access (TDMA), IEEE 802.15.4 provides coexistence capabilities. These solutions regulate network access and give a reasonable data rate [3], [4].

Many IEEE 802.15.4 transmitters with 2.4 GHz are available in current research, including direct conversion, dual conversion, phase-locked loop (PLL) based direct modulation, half-sine shaping (HS) based offset quadrature phase-shift keying (OQPSK), and sub-harmonic and injection-locked (SHIL) based quadrature voltage-controlled oscillators (QVCO). The linear outputs of these transmitter are employed mostly in healthcare control and monitoring applications [5]. The multi-mode-based digital 802.15.4 transceiver using 868/915 MHz and 2.14 GHz frequency bands on a single chip for WPAN applications is described [6]. This module provides an option to choose the convenient baseband for the application requirements. The IEEE 802.15.4 based transceiver is designed using OQPSK with half-sine pulse shaping features to reduce the inter symbol interference (ISI) and provides better system performance [7]–[9]. The 2.4 GHz ZigBee receiver using OQPSK demodulator offers better performance with less resource utilization on a single chip than the conventional DSSS approaches [10].

An efficient BPSK-based IEEE 802.15.4 digital transceiver architecture is designed on field programmable gate arrays (FPGA) platform. The transceiver supports both the 868 MHz and 915 MHz frequency bands. The proposed design uses less chip area, consumes less power, and improves latency and throughput. The digital transceiver presented in the work has a lower bit error rate (BER) and complies with IEEE 802.15.4 PHY standards, making it suitable for usage in communication systems. The BPSK modulator and demodulator in the proposed work are designed using a digital frequency synthesizer (DFS) module for In-phase (I) and quadrature (Q) phase creation. For the IQ generation, most approaches use a voltage-controlled oscillator (VCO) or a look up table (LUT) based memory, which consumes more chip area and power, lowering overall system performance.

The manuscript is organized: section 1 provides the recent existing approaches towards IEEE 802.15.4 based system and its gaps. The proposed BPSK based IEEE 802.15.4 digital transceiver hardware architecture is elaborated in detail in section 2. The results and discussion of the digital transceiver are analyzed in section 3 with a performance comparison. The overall work is concluded in section 4 with future scope.

This section discusses the existing IEEE 802.15.4 transceiver modules for different applications on hardware and software platforms. The numerous physical layers (PHYs) of IEEE 802.15.4 transceiver hardware architectures for software-defined radio (SDR) applications are presented by Massouri and Risset [11]. The transceiver is designed to work on three separate frequency bands using different modulation techniques. The construction of a transceiver for the 2400 MHz frequency band employing OQPSK modulation is elaborated. Further the chip regions of the three designs are explored in depth. Espinoza-Rhoton et al. [12] present the 802.11b and 802.15.4 receiver architectures for SDR applications on the FPGA platform. The combination of 802.11b and 802.15.4 receiver designs is thoroughly discussed. The chip area and frequency characteristics are realized on the Cyclone FPGA. The performance analysis was done by including processing gain (PG), signal to noise ratio (SNR), and BER. For the 4 dB SNR ratio, the system achieves a BER of 10-5. The wireless electrocardiogram (ECG) acquisition SoC module for Zigbee applications is described by Wang et al. [13]. The study examines the detection of human body ECG using a 0.18 m complementary metal–oxide–semiconductor (CMOS) standard.

On both ASIC and FPGA platforms, Olonbayar et al. [14] introduce the IEEE 801.15.4a based Infrared-ultra-wideband (IR-UWB) baseband transceiver module. On the ASIC platform, the transceiver operates at 27.24 Mbps while consuming 74 mW of power at 2.85 V supply voltage. The IEEE 802.15.4g compatible multi-regional frequency shift keying (MR-FSK) based transceiver module for smart metering utility network (SUN) applications on ASIC platform is discussed by Oliveira et al. [15]. On a 65 nm CMOS process, the design utilizes 22,309 cells and consumes 0.197 mW of power. Supare et al. [16] present the M-ary quadrature amplitude modulation (MQAM) based Zigbee transceiver module on the FPGA platform. The transmitter and receiver use a 2.4 GHz frequency band for MQAM modulation operation. The Zigbee transceiver design utilizes 2526 LUT's on the Virtex-7 FPGA device and verifies the simulation results with theoretical calculations. Elmiligi et al. [17] discuss the binary phase shift keying (BPSK) modem for IEEE 802.15.4 Devices. The work discusses more on BPSK modulation and demodulation architectures. The demodulation module has a carrier recovery module with phase detection to identify the originally received signals. The work analyzes the chip area and timing utilization on AMIRIX (AP1000) development board. Zubair et al. [18] present the dual-mode IEEE 802.15.4 receiver architecture with reconfigurable features for diverse internet of things (IoT) applications. The work introduces hybrid (MSK and OQPSK) demodulation in the receiver to realize the SNR indication and complexity analysis. Deep and Elarabi [19] discuss the IEEE 802.15.4 hardware architecture for IoT applications. The simulation results are highlighted for IEEE 802.15.4 transmitter submodules. Gomes et al. [20], [21] discuss the low-power wireless personal area network (6LoWPAN) accelerator module for IoT devices on the FPGA platform. The work analyzes PAN accelerator,

which includes MAC layer filter, transmission control protocol/user-defined protocol (TCP/UDP) filter, denial of service (DoS) security, and data handling. The complete design is evaluated in a real-time environment with an application programming interface (API) setting. The work extended to use further for heterogeneous wireless sensor nodes (WSNs).

Alves-Tamagno et al. [22] present the IEEE 802.15.4g based multi-regional orthogonal frequency division multiplexing (MR-OFDM) with estimator and compensator. The design uses integer carrier frequency offset (ICFO) estimation and compensation mechanisms for IEEE 802.15.4g PHY standards. Liu et al. [23] present the MAC controller architecture for Wi-Fi and ZigBee-based hybrid network systems. The design uses both Wi-Fi and ZigBee data path units which are integrated with processor and control units. The MAC controller simulation results are highlighted along with resource utilization using Zynq FPGA. Charan et al. [24] present the Cache management technique for IEEE 802.15.4 based WSN's. The work analyzes the performance metrics like energy consumption, latency and byte hit ratio for different cache sizes. Kadhum and Haitham [25] present the IEEE 802.15.4 transceiver system using Simulink modeling. The design analyzes step-by-step simulation results for all the sub-modules. BER performance with additive white gaussian noise (AWGN) channel is investigated with and without direct sequence spread spectrum (DS-SS) techniques. Adappa et al. [26] present the slotted and unslotted carrier sense multiple access/collision avoidance (CSMA/CA) for Wi-Fi and ZigBee protocols. The design analyzes the simulation results along with performance realization on Artix-7 FPGA. Guruprasad and Chandrasekar [27] present the 802.15.4 transceiver module for WPANs applications on the FPGA platform. The synthesis results include area, frequency, and power consumption parameters are analyzed on Artix-7 FPGA. The comparative results of the transceiver are highlighted with existing work with chip area improvements. Beula and Rathika [28] discuss the ZigBee transceiver model for smart grid home area networks using MATLAB Simulink (HAN). This research examines the simulation findings as well as the BER calculation. On the system on chip (SoC) platform, Kim [29] offer a dual-mode Bluetooth low energy (BLE) 5.0 and IEEE 802.15.4 transceiver architecture. Using IEEE 802.15.4 mode, the authors achieved a BER of 10-3 on a 28-nm CMOS technology. The DS based code division multiple-access (CDMA) system offers better average channel capacity under Rayleigh fading environment [30]. The OFDM transceiver is integrating with both WLAN and optical technologies to improve the data rate up to 5 Gbps using advanced modulation method [31]. The human body digital transceiver is introduced for wireless Body area network (WBAN) applications using frequency selective digital transmission approach [32].

2. BPSK BASED IEEEE 802.15.4 TRANSCEIVER DESIGN

The digital transceiver architecture is designed as per IEEE 802.15.4 physical layer standards using BPSK modulation and demodulation. The overview of the IEEE 802.15.4 digital transceiver module is represented in Figure 1. In the design AWGN channel is used between transmitter and receiver modules. The differential encoding-decoding, symbol to the chip (S2C) and chip to symbol (C2S) generation units, BPSK modulation, and demodulation units are incorporated in the transceiver module. The BER calculation module is designed to calculate the error rate using input and received data bits. The individual submodules of the IEEE 802.15.4 digital transceiver module are discussed in the following subsections.
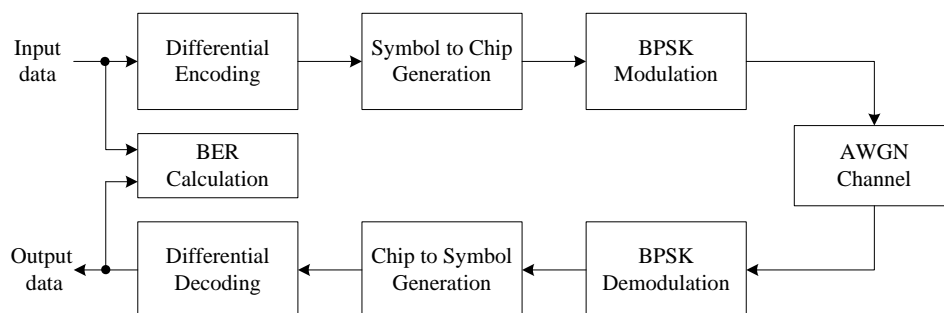

Figure 1. Overview of the IEEE 802.15.4 transceiver module

2.1. IEEE 802.15.4 transmitter module

The IEEE 802.15.4 transmitter hardware architecture using BPSK is represented in Figure 2. The transmitter mainly contains differential encoding (DE), symbol to chip (S2C) generation unit, and BPSK

modulation using a DFS module. The MAC layer provides the data sequence continuously to the differential encoder via the first in-first out (FIFO) interface module. The differential encoder receives the data bits and is processed further for symbol encoding. The differential encoding is used to avoid the signal and symbols inversion from MAC in BPSK modulation. Consider the signal x_i bit for data transmission and s_{i-1} is transmitted symbol, then the Symbol to be transmitted for input signal x_i is represented in (1):

$$s_i = s_{i-1} \oplus x_i \tag{1}$$

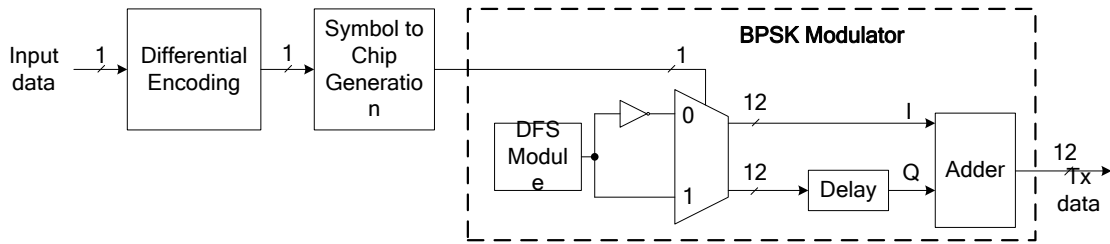where $\oplus$ denotes modulo-2 or binary addition operation.

Figure 2. Hardware architecture of BPSK based IEEE 802.15.4 transmitter module

The symbol to chip generation unit received the encoded data in terms of symbols and mapped it into the 15-bit chip values with the same sample rate. The chip generation is in the form of a pseudo-random sequence, tabulated in Table 1. Suppose the input symbol is '0', then $(09AF)_H$ value else $(7650)_H$ are mapped for chip generation. The generated 1-bit chip sequences are used in BPSK modulation as a select line.

Table 1. Symbol to chip generation values

Input symbols	15-bit Chip Outputs
0	$(09AF)_H$
1	$(7650)_H$

The BPSK is a two-phase modulation technique, where the binary messages like zeros and ones are represented using two different phases in carrier signal: If the binary value is '0' then carrier signal $\theta=180°$ is selected; otherwise, for binary '1', then the carrier signal $\theta=0^0$ is selected. The BPSK modulation is designed using a DFS unit and multiplexor. The multiplexor provides the two forms of output values: in-phase (I) and quadrature-phase (Q) values. The 1-bit chip value acts as the select line to the multiplexor unit. Suppose it is '0', the inverted DFS output else the DFS output value is selected. The I value receives DFS output directly, whereas, The Q value receives the inverted DFS output with a 1-clock cycle delay. These In-phase and quadrature-phase outputs values are added to produce the transmitter output (*Tx_data*). The transmitted bits are corrupted by AWGN to generate the noise signal.

The DFS generates a sinusoidal carrier wave for the BPSK modulation scheme. The DFS provides the accurate frequency, phase, and amplitude results based on the frequency control world (*f_{cw}*) values. The DFS mainly contains a phase accumulator with 1's Complement unit, multiplexor tree, adder unit, and format converter. The phase accumulator provides a saw-tooth wave based on the frequency control word (*f_{cw}*) value. The 1's complement unit provides the triangular wave using Phase accumulator MSB bits. The multiplexor tree with the adder unit generates the half-sine wave. The half-sine wave is converted to the full sine wave using a standard converter unit. The *f_{clk}* is the input clock frequency, and 'n' represents the adder length is set to generate the frequency of DFS output signal (*f_o*), and it is described in (2):

$$f_o = \frac{f_{clk}}{2^n} \times f_{cw} \tag{2}$$

2.2. IEEE 802.15.4 receiver module

The IEEE 802.15.4 receiver hardware architecture using BPSK is represented in Figure 3. The receiver contains BPSK demodulation using the DFS module, C2S generation unit, and differential decoding (DD) unit. The BPSK demodulated receives the corrupted noise signal data, which AWGN on the receiver side causes. The BPSK demodulator uses two D-FF units to synchronize the clock signal with receiver input.

The same DFS module is used to generate the sinusoidal carrier signal. The comparator is used to compare the receiver input (*Rx_in*) with delayed DFS output. If both the values are equal, then one else zero is considered as a BPSK demodulator output.
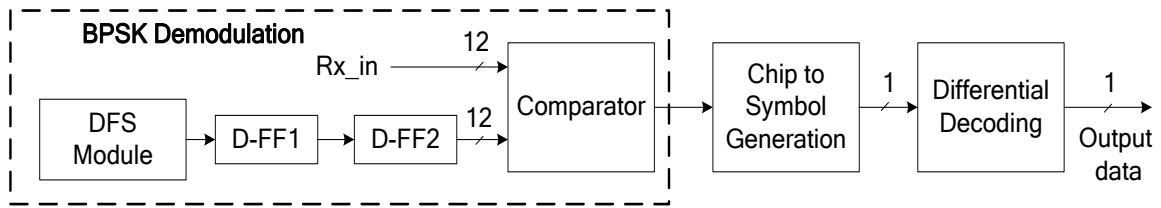

Figure 3. Hardware architecture of BPSK based IEEE 802.15.4 receiver module

The chip to symbol (C2S) generation unit received the 1-bit BPSK demodulated output in a sequence and converted it to symbol using the same 15-bit chip values. The differential decoding module receives the symbol data in a sequence and recovers the original data (y_i) using (3):

$$y_i = S_i \oplus S_{i-1} \tag{3}$$

The difference between received symbol data (S_i) and previous symbol data (S_{i-1}) depends only on the recovered original data (y_i). These recovered data are not influenced by any of the inversion from symbol data.

2.3. Bit error rate calculation module

The hardware architecture of the BER calculation module is represented in Figure 4. The signal-to-noise ratio (SNR) values are used to calculate the BER. The ratio of energy per bits by spectral noise density (E_b/N_o) is called SNR. The zero mean (m=0) and unity variance ($\delta^2=1$) generate the AWGN value. The square of the scaling factor (s) and its inverse is used to determine the new variance value ($\delta^2=1/s^2$). The SNR is calculated based on scaling factor: $s^2/4$.
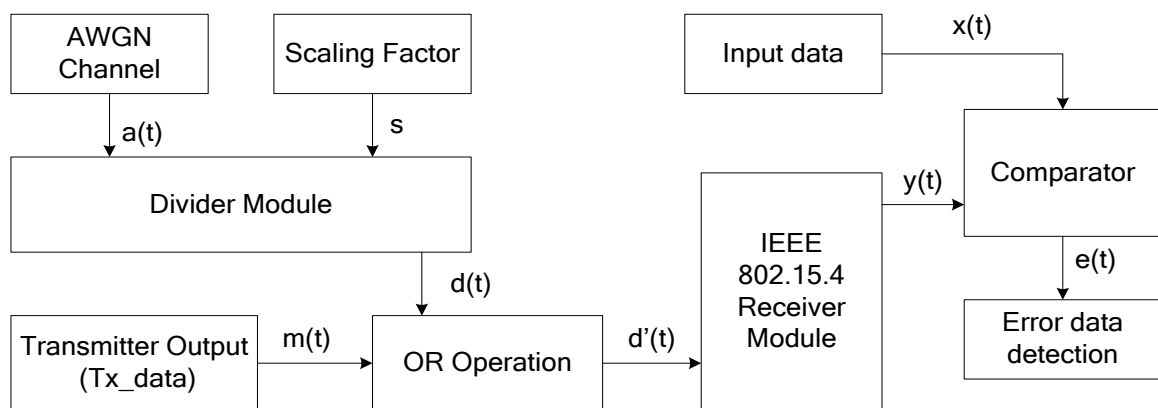

Figure 4. Hardware architecture of BER calculation module

To generate the different SNR values using scaling factor value for the AWGN channel. The linear feedback shift register (LFSR) generates the random sequence of data for AWGN generation a (*t*). The noise data *d(t)* is generated by divide the AWGN data a (*t*) with scaling factor (*s*). Perform the OR operation with transmitter output *m(t)* with noise data *d(t)* to generate the corrupted data *d'(t)*, and it is represented in (4):

$$d'(t) = \frac{a(t)}{s} | m(t) \tag{4}$$

The IEEE 802.15.4 receiver module receives the corrupted data *d'(t)* as input, performs the receiver operation, and generates the receiver output *y(t)*. The error detection *e(t)* is calculated by comparing the delayed input data *x(t)* sequence with receiver data output *y(t)*. If *e(t)* is one, then error data is present; otherwise, no error data appears on the transceiver system, and it is represented in (5):

$$e(t) = 1; \; if \; x(t) \neq y(t) \; \text{Else} \; 0 \tag{5}$$

3. RESULTS AND DISCUSSION

Using the Xilinx ISE environment, the IEEE 802.15.4 physical layer-based digital transceiver is designed and implemented on the Artix-7 FPGA. The Xilinx ISE simulator helps to determine the BER value by simulating the digital transceiver design. To examine performance indicators and resource utilization, the synthesis results are presented for the transceiver module. The performance of current equivalent IEEE 802.15.4 digital transceiver modules with better resource improvements is compared.

The simulation results of the IEEE 802.15.4 digital transceiver module are represented in Figure 5. The global clock (clk) is activated with low asynchronous reset (rst) to initiate the operation of digital transceiver. The 1-bit data input (din) is processed sequence, and transceiver obtains the receiver output (dout) with a latency of 3.5 clock cycles. The delayed input (delayed_in) is used to match the receiver output (dout); if both are equal, there is no error; otherwise, error data is present. The 16-bit error counter (error_cnt) is used to count the number of errors. Additionally, the main counter (total_din) is used to count the number of inputs transmitted to the transceiver module. In this work, the 150,000 bits are transmitted with a scaling factor of 4 and 6 dB of SNR to the digital transceiver module and identifies the three error bits in the ISE simulator. The IEEE 802.15.4 digital transceiver module achieves the BER of 2×10^{-5} for the given 6 dB SNR value in the AWGN channel. A better BER is achieved by increasing the number of input bits to be transmitted.
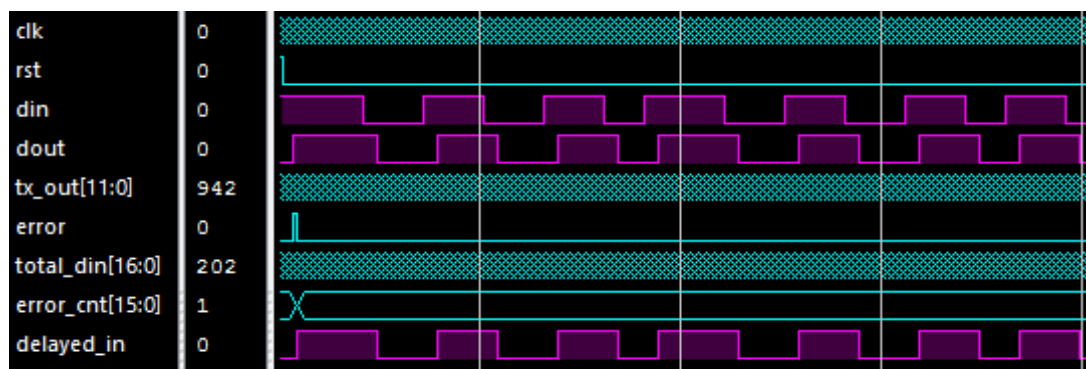

Figure 5. Simulation results of IEEE 802.15.4 transceiver module

The resource utilized for IEEE 802.15.4 digital transceiver module on Artix-7 FPGA is represented in Table 2. The IEEE 802.15.4 digital transceiver module utilizes 123 Slices, 187 LUTs, 106 LUT-FF pairs and works at 268.2 MHz operating frequency. The transceiver module consumes 108 mW of total power, including 26 mW dynamic power at 100 MHz clock frequency using the X-power analyzer tool. The performance metrics like latency, throughput, hardware efficiency, and BER are also tabulated for the transceiver module. The IEEE 802.15.4 digital transceiver module obtains the Latency of 3.5 Clock cycles (CC) using the simulator tool and achieves the throughput of 76.62 Mbps on Artix-7 FPGA. The digital transceiver module receives 62.81 Kbps/Slice hardware efficiency with a BER of 2×10^{-5}.

The performance comparison of the proposed transceiver module with the existing 802.15.4 transceivers for Zig-bee applications is tabulated in Table 3. The different design parameters like the selection of modulation technique, obtained chip area (slice and LUTs), maximum frequency, total power, and selected FPGA devices are considered compared with existing IEEE 802.15.4 transceiver architectures.

The IQ-phases are main part of modulation and demodulation process in any digital transceiver design. The existing IEEE 802.15.4 based digital transceivers uses VCO or LUT based memory modules for the creation of IQ-phases for modulation and demodulation in the design. The VCO or LUT based memory modules utilizes more chip area, drains the operating frequency and consumes more power on FPGA and it affects the overall the performance of the digital transceiver design. The proposed design consumes less chip

area (Slice and LUTs), works at better operating frequency (MHz), and consumes less power than the above existing approaches. The proposed design uses DFS module for the creation of IQ-phases both in modulation and demodulation modules and offers better performance than existing approaches.

Table 2. Resource utilized for IEEE 802.15.4 transceiver module on Artix-7

Resources	Obtained
Chip Area	
Slices	123
LUTs	187
LUT-FF pairs	106
Time	
Minimum period (ns)	3.729
Maximum frequency (MHZ)	268.2
Power	
Dynamic power (mW)	26
Total power (mW)	108
Performance	
Latency (Clock Cycles)	3.5
Throughput (Mbps)	76.62
Hardware efficiency (Kbps/Slice)	62.81
Bit error rate (BER)	2×10^{-5}

Table 3. Performance comparison of proposed work with existing 802.15.4 transceivers

Design Parameters	Muni *et al.* [8]	Massouri and Risset [11]	Supare *et al.* [16]	Elmiligi *et al.* [17]	Guruprasad and Chandrasekar [27]	Proposed Design
Modulation Technique	O-QPSK	BPSK	MQAM	BPSK	O-QPSK	BPSK
Slices	973	1649	320	229	224	122
LUTs	1179	1849	2526	284	428	187
Max.Frequency (MHz)	117.9	200	NA	105.502	270.1	268.193
Total power (mW)	216	NA	NA	NA	171	108
FPGA	Virtex-5	Virtex-6	Virtex-7	Viretx-2 Pro	Artix-7	Artix-7

4. CONCLUSION AND FUTURE SCOPE

In this manuscript, an efficient BPSK based IEEE 802.15.4 digital transceiver is designed on FPGA Platform. The BPSK modulator and demodulators are designed effectively using the DFS module. The transceiver design is flexible to operate in either 868 MHZ or 902 MHz frequency bands. The error calculation module is introduced in the IEEE 802.15.4 digital transceiver to verify the received bits and find the BER calculation. The simulation results of the IEEE 802.15.4 digital transceiver module are verified and analyze the received error bits. The digital transceiver module utilizes around 1% slices and LUT's, operates at 268.2 MHz, and consumes 108 mW of total power on Artix-7 FPGA. The transceiver uses only 3.5 clock cycles and obtains the throughput of 76.62 Mbps with an efficiency of 62.81 Kbps/slice. The transceiver achieves the BER of 2×10^{-5} by transmitting around 150,000 bits in a sequence. The proposed IEEE 802.15.4 digital transceiver is compared with similar transceiver architectures with better chip area, frequency, and total Power. In the future, introduce the phase encryption and decryption module to the digital transceiver to enhance the security features and also realize the performance metrics.

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BIOGRAPHIES OF AUTHORS

Vivek Raj Kempanna 🆔 ⑧ SC ↻ graduated from Visvesvaraya Technological University, Belagavi with Bachelor of Engineering in Electronics and Communication. He received his Master of Technology in Digital Electronics and Communication Systems from the same university in 2014. He is working as Assistant Professor in Department of Electronics and Telecommunication Engineering, Dayananda Sagar college of engineering, Bengaluru, India. Currently he is pursuing Ph.D. from Visvesvaraya Technological University. His areas of interest are HDL, very-large-scale integration (VLSI) design, digital electronics, wireless communication and cryptography. He is member of ISTE. He can be contacted at email: vivekgowda1990@gmail.com.

Dinesha Puttaraje Gowda 🆔 ⑧ SC ↻ received his Ph. D degree from University of Mysore, India, in the year 2014. He is currently a Professor, Department of Electronics and Communicating Engineering, Dayananda Sagar College of Engineering, Bengaluru, India. His research interest is in VLSI design, digital system design and nanotechnology (applications of conducting polymer composites in electronics). He can be contacted at email: dineshprg@gmail.com.