I.FAST

Innovation Fostering in Accelerator Science and Technology

Horizon 2020 Research Infrastructures GA n° 101004730

MILESTONE REPORT

Demonstration of operation with high efficiency and nominal power of the first GaN amplifier

MILESTONE: MS63

Document identifier:	IFAST-MS63
Due date of deliverable:	End of Month 12 (M12) delayed to M18 (October 2022)
Report release date:	31/10/2022
Work package:	WP13: Technology Infrastructure
Lead beneficiary:	UU
Document status:	Final

ABSTRACT

A new solid-state power amplifier in Gallium Nitride (GaN) semiconductor technology was developed in the I.FAST project and is reported here to deliver 205 W with 82% power added efficiency at 750 MHz. This is the first demonstration of operation with high efficiency and nominal power of the first GaN power amplifier at this power level and frequency. In next steps of the project, six of such amplifiers will be combined together, developing a high efficiency combiner into a kilowatt level amplifier demonstrator.

For more information on IFAST, its partners and contributors please see https://ifast-project.eu/

This project has received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement No 101004730. IFAST began in May 2021 and will run for 4 years.

Delivery Slip

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Executive summary

A new solid-state power amplifier in Gallium Nitride (GaN) semiconductor technology was developed in the I.FAST project and is reported here to deliver 205 W with 82% power added efficiency at 750 MHz. This is the first demonstration of operation with high efficiency and nominal power of the first GaN power amplifier at this power level and frequency. In next steps of the project, six of such amplifiers will be combined together, developing a high efficiency combiner into a kilowatt level amplifier demonstrator.

GaN is anticipated to be extensively used for the next-generation power semiconductor devices, as it significantly outperforms silicon-based power transistors, thanks to a higher breakdown strength, faster switching speed, higher thermal conductivity and lower on-resistance. Presently, the nominal power level of single GaN transistors is only in the hundreds watts level.

This work contributes to improve the state-of-the-art for kilowatt level amplifiers at 750 MHz and has direct industrial applications as the RF power source of the RFQ that was developed at CERN.

Solid state power amplifiers (SSPA) rather than vacuum tubes are undoubtedly preferred to make a high-power RF amplifier in case of similar electrical characteristics due to their particular advantages e.g. high reliability, compactness, and low cost. Recently, SSPAs based on two emerging semiconductor technologies (GaN and LDMOS) have been more actively considered as capable to deliver high power levels, i.e. in the kilowatt range. Although scattered activities have been carried out in the last decades, most of them are still in the early stage and require to be investigated more on new technology/instrumentation. In addition, the lack of powerful yet affordable integrated multidisciplinary knowledge prevents the applicability of SSPA technology in the medical equipment. Within the scope of this research project, we propose to develop a kilowatt level cost effective SSPA suitable for replacing with vacuum tubes at 750 MHz.

The purpose of this project is to demonstrate the advantages and feasibility of Gallium Nitride (GaN) semiconductor technologies for radio frequencies (RF) amplifiers using GaN new transistors with higher power density, suitable for extreme high power and high efficiency amplifiers for particle accelerators. We aim at developing GaN based solid-state power amplifiers (SSPA) in the kilowatt range, as the building blocks of larger amplifiers for particle accelerators. We will go beyond the present state-of-the-art, exploring kilowatt level GaN amplifiers targeting accelerator applications.

GaN is anticipated to be the next-generation power semiconductor. With a higher breakdown strength, faster switching speed, higher thermal conductivity and lower on-resistance, power devices based on GaN significantly outperform Silicon-based power chips. The first-generation GaN-based power devices play already a key role in the power conversion within battery chargers, smartphones, computers, servers, automotive, lighting systems and photovoltaics. Today, GaN is grown on a variety of substrates, including sapphire, silicon carbide (SiC) and silicon (Si), allowing to be employed in higher power applications.

The work carried out in Task 13.3 allowed establishing the State of the Art and selection of the transistor to realise the power amplifier following the specifications at 750 MHz. The first point was the selection of technology between GaN and LDMOS. Eventually, GaN semiconductor technology was selected as it works till three times the drain voltage, which enables highly efficient architectures based on harmonics engineering.

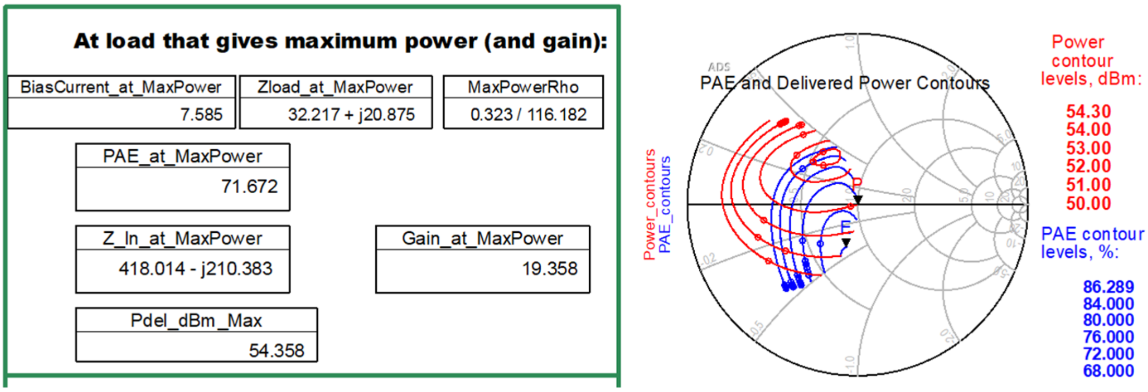
This MS63 reports the achievement of the work carried out in Task 13.3, i.e. the ddemonstration of operation with high efficiency and nominal power of the first GaN amplifier.

After establishing the State of the Art and selection of the transistor to realise the power amplifier following the specifications, GaN semiconductor technology transistor CGHV40180F was selected. It operates from 50 voltage rail, and the maximum rating of Drain-Source voltage swing is 150 V, enabling highly efficient architectures based on harmonics engineering. The transistor is manufactured by the Wolfspeed company and works up to 2 GHz. Its specific advantages include high efficiency and high gain with a reasonable cost. It is an unmatched transistor requiring to design the input and output matching networks. The simulation, fabrication, and measurement of the designed power amplifier at 750MHz are explained in the following report.

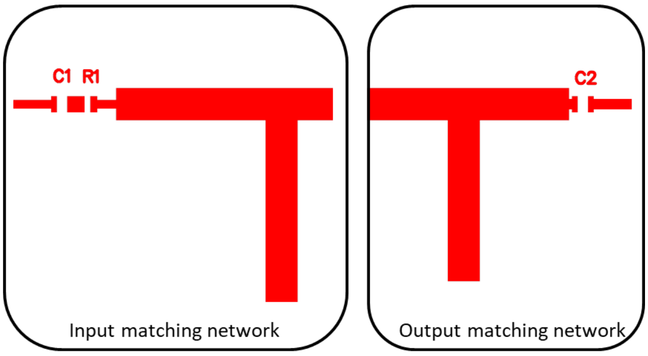
1 First GaN amplifier

1.1 Simulations

Initial simulations were performed using the large signal model of the transistor CGHV40180F offered by the manufacturer, i.e. Wolfspeed and using the simulations software ADS (Advanced Design System), from Keysight Technologies. The transistor gate is biased in the pinch off point i.e. -3 V, enabling to have a high efficiency performance using the harmonic engineering method. Then, the development of RF amplifier starts from load-pull simulations on the large signal model, as the input impedance is considered 2.5 ohm, see Figure 1. Figure 1(a) shows the simulation results for a diverse output impedances, illustrating the drain efficiency of 86% as the output power is compressed to 51dBm (125 Watt) and the output power of 54.3 dBm (269 Watt) as the drain efficiency is compressed to 71.6%. Therefore, an optimum output impedance i.e. 2.7-j 4.2 Ohm regarding to the output power of 53 dBm (200 Watt) and the drain efficiency of 82% is considered. Thus, to realise the power amplifier, the transistor input/output optimum impedances are matched with 50 ohm as shown in Figure 1(b), demonstrating the resulting layout of the designed amplifier, with an expected performance, i.e. nominal output power of 200 W with an efficiency of more than 80% in continuous wave (CW) condition.



(a)



(b)

Figure 1: (a) Simulation results of the amplifier with calculated input and output matching networks. (b) Layout of the input and output matching networks.

1.2 Fabrication of the first prototype

The design is realised on a low loss RF substrate from Rogers Corporation, i.e. RO3006 with a thickness of 1.27mm, a dielectric constant of 6.15, and dissipation factor of 0.002. The fabricated 200 W power amplifier prototype is shown in Figure 2, depicting the initially designed input and output matching networks in addition of decoupling capacitors (C1 and C2) and DC biasing network. In the bias network, we employed a GaN bias circuit from MACOM Company with the part number of MABC-001000 to provide a safe bias sequenc for the transistor.

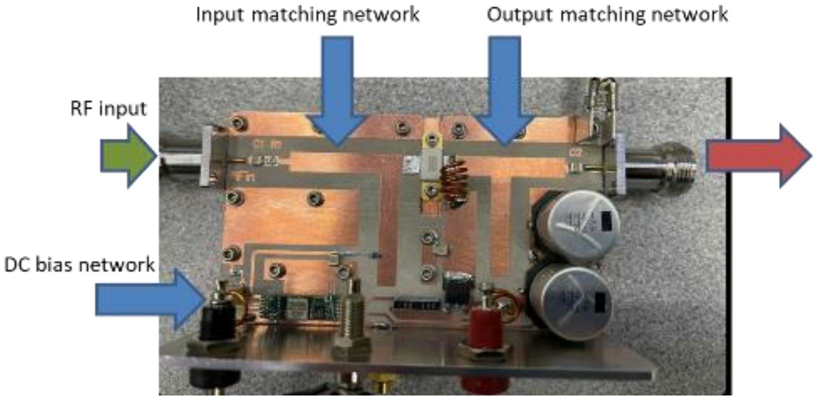


Figure 2: Fabricated 200 W RF power amplifier

1.3 Measurements bench

To characterize the power amplifier (PA), a measurement bench setup including: spectrum analyzer, driver, power meter, bidirectional coupler, dummy load, and related power supplies are organized as shown in Figure 3.

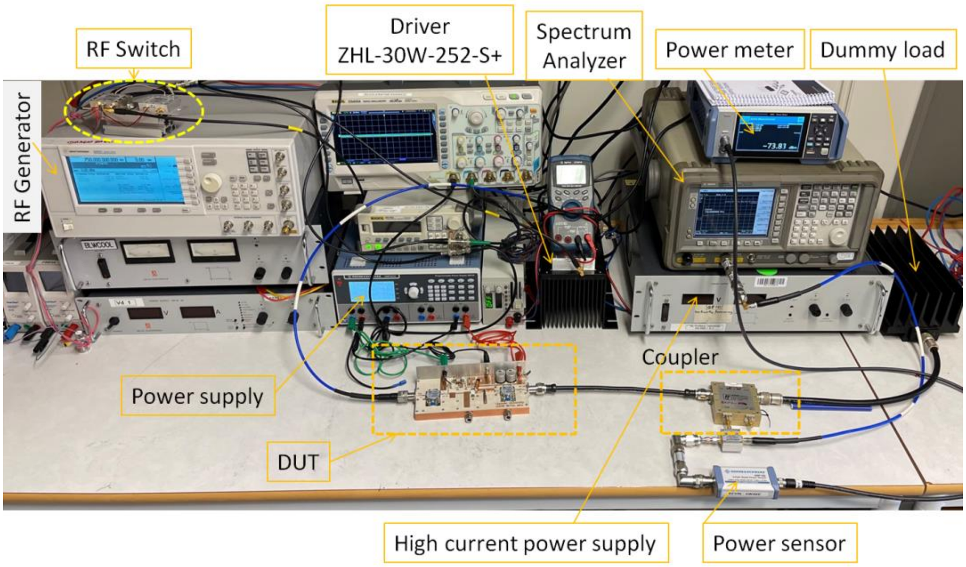


Figure 3: Measurement setup for characterizing the manufactured power amplifier.

1.4 SECOND ITERATION OF THE 200 W NOMINAL POWER AMPLIFIER

In continuation of the primary design of the 200W power amplifier in GaN technology at 750 MHz, we developed further the design of the input matching network from 1st-order filter to 2nd-order filter to meet the optimum input impedance of the selected transistor. We also modified the output matching network by adding a copper bar to improve the thermal performance of the copper traces. Figure 4 shows the second design of the power amplifier, delivering the output power of around 200W. The previous design was here improved essentially considering the microwave performance in terms of both output power and DC to microwave transfer efficiency. A more advanced DC biasing network is also provided.

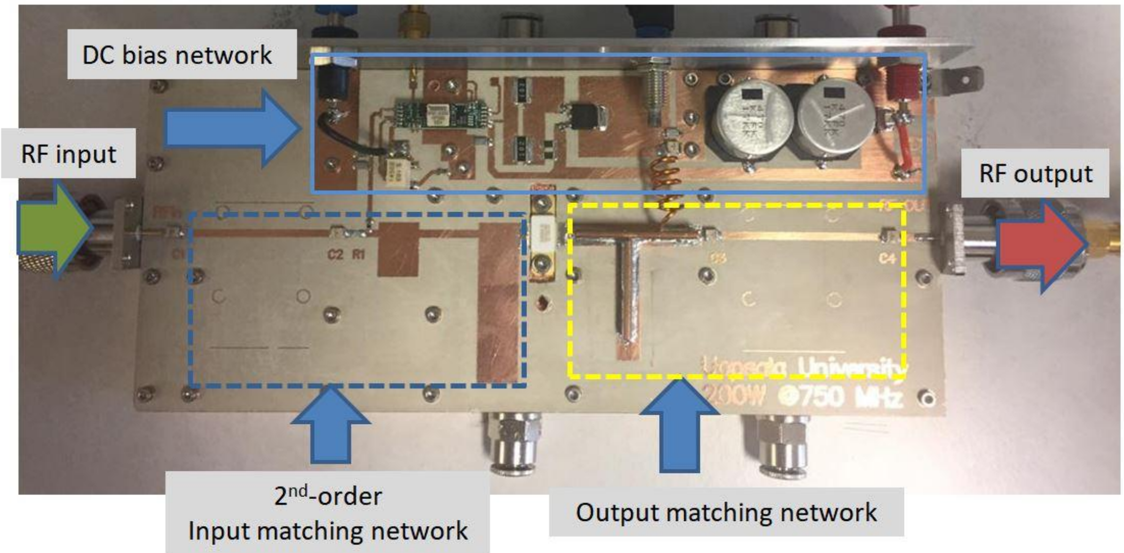


Figure 4: Second iteration of the design of the 200 W RF power amplifier with enhanced input and output matching networks.

1.5 THIRD AND FINAL ITERATION OF THE 200 W NOMINAL POWER AMPLIFIER

To realize the kilowatt level power amplifier (PA), six 200W power amplifiers will be combined together using a low loss power combiner, that will be developed in a later stage. The amplifier must be robust against both output power reflections and input impedance unbalances. Therefore, in a modified version of the PA, two RF isolators are added to the input and the output matching networks, respectively, as shown in Figure 5. Water-cooling connectors are also provided to the heatsink and the PA is ready for characterization under full power and continuous wave (CW) operating conditions.

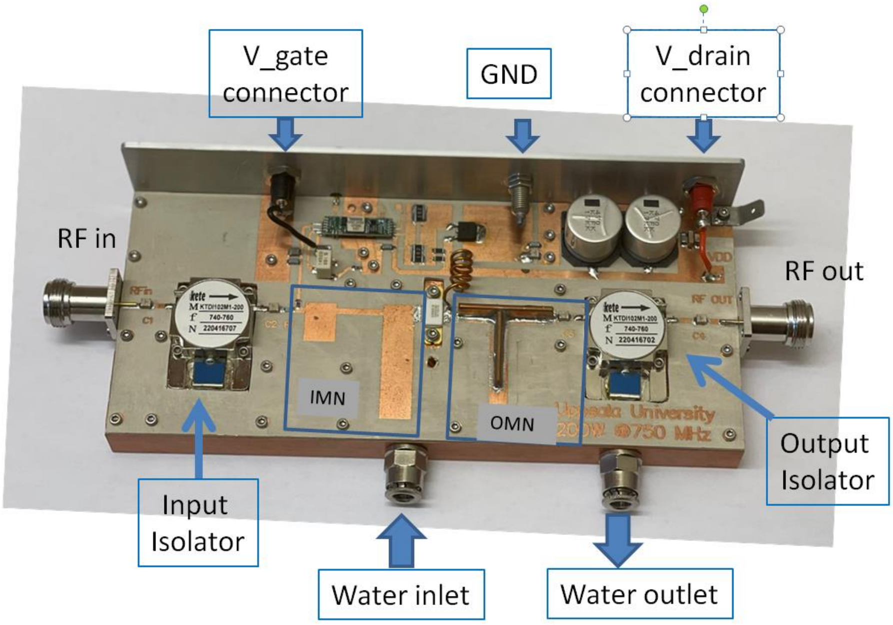


Figure 5: Modified 200W RF power amplifier including input and output isolators and water-cooling connectors.

1.6 CHARACTERISATION OF THE FINAL AMPLIFIER AT NOMINAL POWER

The power amplifier exhibits 180-Watt output power, 17.7 dB signal gain, and 76% drain efficiency at 34.5 dBm input power in its final configuration, i.e. when provided with input and output isolators. The output isolator insertion loss is quite high, i.e. 0.5 dB, but is necessary to ensure good isolation among the six amplifiers that will be combined with a binary type combiner which does not have port to port isolation. In comparison, the PA without isolator , see Fig. 4, delivers 52.45 dBm (205 watt), 82% drain efficiency, and 15.5 dB signal gain as the PA is fed by 37 dBm. The measurement results are presented in Figure 6.

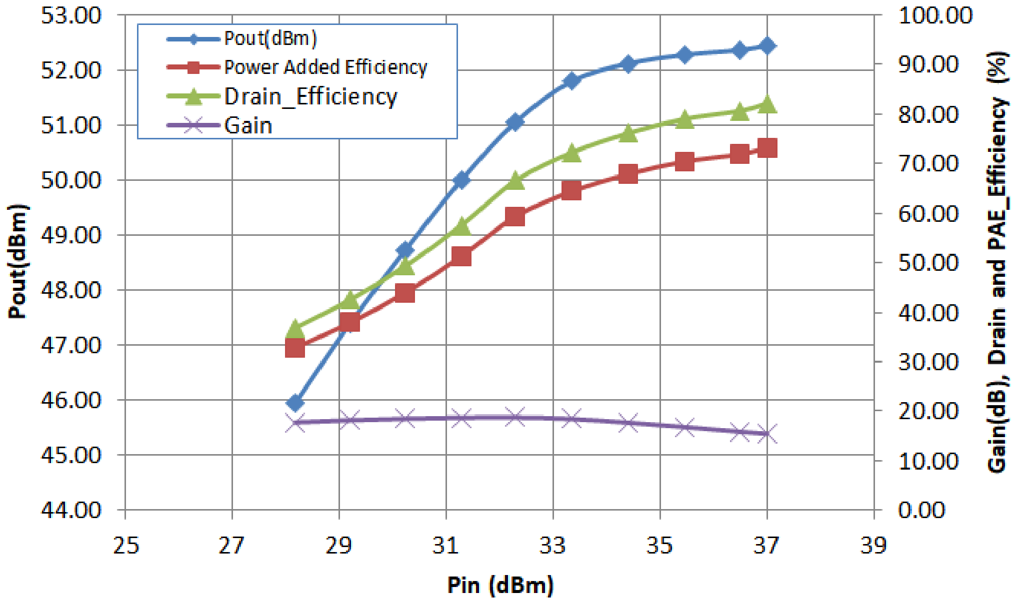


Figure 6: Measurement results of the PA presented in fig. 5 with the input and the output isolators including output power, drain efficiency, power added efficiency, and signal gain.

The thermal performance of the PA was checked under an IR scan during CW operation, thus when the PA was delivering 180W in CW. In order to provide normal operating condition, we kept the copper heatsink temperature 24°C and followed the transistor temperature. As shown in Figure 7, the transistor body temperature reaches to 30.9°C in steady state condition, confirming the high efficiency PA behavior.

Figure 7: IR camera scan of the 200W power amplifier at 750 MHz

2 Annexes

2.1 State of art for UHF power amplifier

The list of commercially available GaN transistors considered for the design of the 750 MHz amplifier within this project is provided below. In addition, we can report that the current state of the art transistor from IMEC is realized on 200mm wafer GaN-on-Si technology platform for 200V and 650V (e-mode) power devices. At the Ferdinand Braun Institute, the current research is focused on low dispersion devices for blocking up to 1000 V and works are on further increasing the threshold voltage. The lateral GaN-on-Si heterojunction field-effect transistors (HFETs) is characterized by a low area-specific on-state resistance for a given blocking strength and a low gate charge required for switching. This allows high-voltage power switching transistors enabling efficient power converters with increased power density.

Year and Reference	Operating class	F_{min} (MHz)	F_{max} (MHz)	P_{out} (dBm)	Gain (dB)	PAE_{min} (%)	Package/Die	Technology	Institution
2020 [1]	Push pull	24.5	27	59.8	25	83	packaged	LDMOS	FREIA – Uppsala U.
2019 [2]	Class AB	400	450	60	15	-	Packaged	GaN	SSPL - Delhi
2018 [3]	Class AB	UHF	-	67.2	-	55	Packaged	GaN	CETC - Nanjing
2017 [4]	Class AB	1200	1400	64	16.7	55	packaged	LDMOS	USTB - Beijing
2016 [5]	Class AB	352	-	60.9	20.5	71	Packaged	LDMOS	FREIA – Uppsala U.
2016 [6]	Class AB	200	500	40	18	71	packaged	GaN	CESAT - Islamabad
2016 [7]	Class B	420	450	60	25	73	3 chip Packaged	GaN	Integra Tech. - CA
2020 [8]	Class E	400.8	-	63.6	22	70	Die	GaN	Integra Tech. - CA
2018 [9]	Class E	680	750	47	-	80	packaged	GaN	U. of Cantabria
2018 [10]	Class E	100	-	60.8	-	82	packaged	LDMOS	FREIA – Uppsala U.
2017 [11]	Harmonic tuned	420	450	60	40 (two stages)	75	Packaged	GaN	Integra Tech. - CA
2017 [12]	Class E	670	900	44.7	-	70	packaged	GaN	U. of Cantabria
2016 [13]	Class F	704	-	58	-	79	packaged	GaN	Green Mountain Radio Research
2016 [14]	Class F	550	950	40	15	75	packaged	GaN	U. of Calgary
2011 [15]	Class F	550	1100	40	10	74	packaged	GaN	Cardiff U.

2.2 References

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3 Future plans / Conclusion / relation to other IFAST work

In the near future the design and implementation of a 6:1 power splitter and combiner is foreseen. Five such amplifiers will be realised and combined together with this combiner to obtain an output power in the kilowatt range. Manufacturing and characterisation of the 1 kilowatt PA prototype are foreseen, resulting in the deliverable D13.3 planned for M33 (instead of M24), due to the delay of MS63 because of the unavailability of some electronic components.

As we mentioned above, in order to design 1 kilowatt RF power amplifier, six power amplifiers must be combined. To this end, the next step of the project is to design 1 to 6 and then 6 to 1 RF signal splitter and RF signal combiner respectively, to spread and collect the RF signal through the six PAs. A planar binary configuration without signal isolation is foreseen for the splitter and combiner architecture, since the PA has been protected from reverse power and input impedance unbalances by using the input/output isolators.

The amplifier module represents a leap forward in higher efficiency and higher power and could serve as building block for larger amplifiers dedicated for particle accelerators. In the same time, UU will upgrade its experimental capabilities at the FREIA laboratory, fostering the dissemination of GaN semiconductor technology for the particle accelerator community.

Impact 1: To ensure and enhance the life-cycle cost reduction (including manufacturing and operations) and increased performance, resulting in the enhanced competitiveness of the European radio frequency manufacturing industry for particle accelerators. By considerably increasing the efficiency of high power amplifiers, the project will bring together microwave engineers and semiconductor technology specialists evaluating the GaN technology for the needs of the particle accelerator community; an opportunity for research and scientific novelty.

Impact 2: To develop further the infrastructure at the FREIA laboratory towards acquiring the capabilities to support future research projects. As an AMICI associated ARIES 2 application, we embrace the opportunity to improve of our accelerator test facility. To support highly innovative projects such as ESS and MYRRHA and other commercial developments as the industrialisation of the RFQ at 750 MHz at CERN.

Impact 3: The impact of this activity will extend beyond the particle accelerator community, towards other applications of high RF power. By developing the European research and technology ecosystem consisting of different parties involved in applications of RF energy.

This work relates also to other works within the IFAST project, as an application based on the results of this WP13.3 was proposed within the I.FAST fund for accelerator innovation, entitled: “Development of highly efficient megawatt class cross fielded vacuum tube amplifier for particle accelerators driven by a solid state power amplifier at 750 MHz”. This is about a megawatt class magnetron at 750 MHz, where we will use the I.FAST developed GaN SSPA at 1kW as driver for the magnetron. Two industrial partners: Exir Broadcasting AB and Scandinova AB, and CERN as supporting partner.

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Annex: Glossary

Acronym	**Definition**
SSPA	Solid State Power Amplifier
GaN	Gallium Nitride – semiconductor technology
VDD	Drain voltage – DC supply voltage
LDMOS	Laterally-diffused metal-oxide semiconductor is a planar double-diffused MOSFET
MOSFET	Metal–oxide–semiconductor field-effect transistor