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MALTA3: Concepts for a new radiation tolerant sensor in the TowerJazz 180 nm technology

Dominik Dobrijević [a,b,*], Phil Allport [c], Ignacio Asensi [a], Dumitru-Vlad Berlea [d], Daniela Bortoletto [e], Craig Buttar [f], Florian Dachs [a], Valerio Dao [a], Haluk Denizli [g], Leyre Flores [a], Andrea Gabrielli [a], Laura Gonella [c], Vicente González [k], Matt LeBlanc [a], Marcos Vázquez Núñez [a,k], Kaan Oyulmaz [g], Heinz Pernegger [a], Francesco Piro [a,h], Petra Riedler [a], Heidi Sandaker [j], Carlos Solans Sánchez [a], Walter Snoeys [a], Tomislav Suligoj [b], Milou van Rijnbach [a,i], Julian Weick [a,j], Steven Worm [d]

[a] *Experimental Physics Department, Organisation Européenne pour la Recherche Nucléaire (CERN), F-01631 Prévessin Cedex, France – CH-1211 Genève 23, Geneva, Switzerland*
[b] *University of Zagreb, Croatia*
[c] *University of Birmingham, United Kingdom*
[d] *Deutsches Elektronen-Synchrotron (DESY), Platanenallee 6, D-15738 Zeuthen, Germany*
[e] *University of Oxford, United Kingdom*
[f] *University of Glasgow, United Kingdom*
[g] *Bolu Abant Izzet Baysal University, Turkey*
[h] *École polytechnique fédérale de Lausanne, Lausanne, Switzerland*
[i] *University of Oslo, Norway*
[j] *Technische Universität Darmstadt, Germany*
[k] *Universitat de València, Spain*

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ABSTRACT

The upgrade of the MALTA DMAPS designed in Tower 180 nm CMOS Imaging process will implement the numerous modifications, as well as front-end changes in order to boost the charge collection efficiency after the targeted fluence of $1x10^{15}$ 1 MeVn_{eq}/cm^2. The effectiveness of these changes have been demonstrated in recent measurements with a small-scale Mini-MALTA demonstrator chip. Multiple changes in the digital periphery are proposed: The asynchronous address generator will be revised to provide more control over the pulse length. The Synchronization memory will be upgraded with the goal of achieving a sub-nanosecond timing resolution. Serial chip to chip data transfer will be prototyped, in order to gauge the plausibility of implementation on a future full sized chip. Apart from these changes, research of the overall sensor architecture will be discussed as well.

1. Introduction

MALTA is a depleted monolithic active-pixel sensor (DMAPS) [1] originally designed to match the requirements of the Inner Tracker (ITk) of the ATLAS experiment [2] at the high-luminosity LHC. This sensor is capable of operating at 5 Gbps [3], and cope with hit rates up to 100 MHz/cm^2 using an asynchronous readout architecture [4], with a pixel pitch of 36.4 μm.

The MALTA sensors are manufactured in Tower 180 nm CMOS imaging process, with additional process modifications [5,6] that enhance the lateral electric field into pixel corners to increase tolerance to non-ionizing energy loss (NIEL) as demonstrated by the Mini-MALTA in particle beam test measurements [7].

The development of the latest full-scale prototype in this series, MALTA2, still focused on increasing the charge collection efficiency. The noise tails of the original MALTA sensor were reduced through the addition of a cascoded transistor and an enlarged feedback loop transistor within the pixel front-ends. This resulted in MALTA2 surpassing the 97.5% charge collection efficiency after 2×10^{15} 1 MeV n_{eq}/cm^2 NIEL requirement set by the 5th layer of the ITk of the ATLAS experiment. Due to this, further development has shifted towards timing performance, and improved integration capabilities of the sensor.

* Corresponding author at: University of Zagreb, Croatia.
E-mail address: dominik.dobrijevic@cern.ch (D. Dobrijević).

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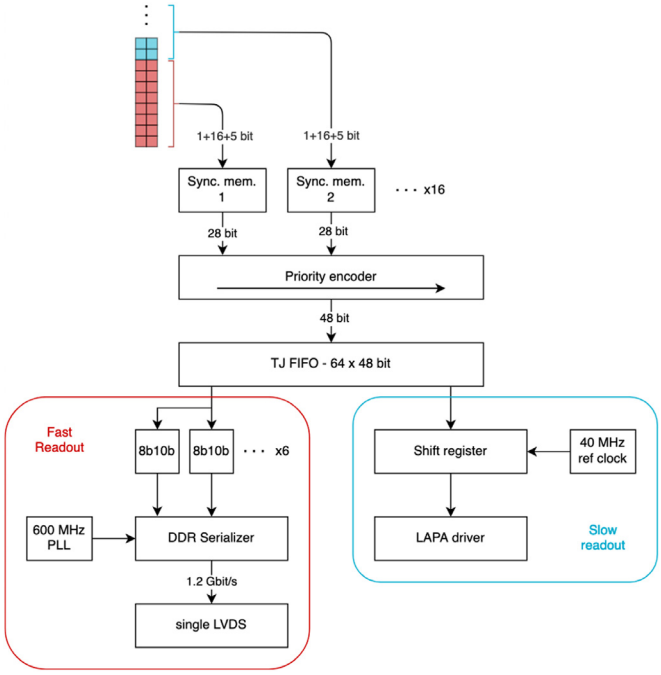

Fig. 1. Mini-MALTA digital periphery block diagram.

The following prototype, MALTA3, will introduce on-chip time tagging, and a high speed serial output.

2. Current architecture

The original MALTA chip was a fully asynchronous MAPS, featuring a 512 × 512 matrix of pixels with a small collection. Once a hit is registered within the pixel, a trigger signal is generated and used to propagate the pixel address towards the periphery. These hit addresses are then merged by a dedicated structure and sent off chip using 37 parallel LVDS drivers towards an external DAQ system. There, the hits are appended a time tag and filtered. This approach offers a very high theoretical timing resolution — once the signal chain is properly characterized, the jitter of the propagated trigger signal is the main limit. However, the integration of such a detector in a real experiment is very complicated due to the requirement of 37 differential data pairs.

The Mini-MALTA small scale demonstrator was created to address this issue. The asynchronous matrix was reduced to a size of 16 × 64 pixels, but otherwise unchanged. Instead of the merging structure, a synchronization memory is found at the periphery. The purpose of this memory is appending a time tag to the hit address while it is still on chip, in turn allowing a more conventional and controllable digital readout afterwards. A general block diagram of the Mini-MALTA digital periphery can be seen in Fig. 1. The priority encoder which follows can be seen as a replacement of the merging tree from the original MALTA, as it passes the hits stored in the synchronization memory one by one towards a FIFO. Lastly, the data stored in the FIFO is serialized and sent off-chip using the same LVDS driver from the original MALTA.

A more detailed diagram of the synchronization memory operation can be seen by Fig. 2. The 640 MHz fine time and the 40 MHz LHC Bunch Crossing ID (BCID) gray encoded counters are contained within each memory block, but the clocks are generated externally. Each memory block has a depth of 4 words which is deemed sufficient for the targeted hit rates of the full size chip.

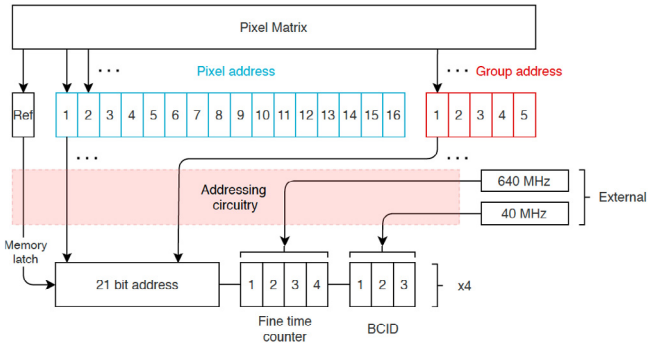

Fig. 2. Mini-MALTA synchronization memory structure.

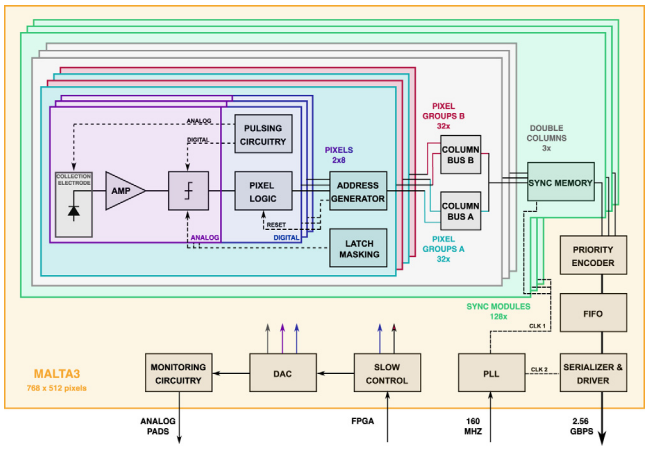

Fig. 3. The proposed MALTA3 block diagram.

3. Proposed upgrades

All the full size MALTA chips up to this point have been fully asynchronous, utilizing the same hit merging structure and parallel LVDS drivers for off chip data transmission. They differ in process modification and pixel flavours, developed with charge collection efficiency improvements in mind. The Mini-MALTA is a small scale demonstrator which explored on-chip synchronization of incoming pixel hits. However, some features of this architecture cannot be directly expanded to a full size chip. In the same regard, previously implemented features such as the chip to chip communication will need to be modified before they can be combined together with the new synchronization circuitry. Merging the successfully demonstrated features of the previous MALTA chips while addressing the shortcomings of the new synchronous concept can be considered as the primary goal of the MALTA3 development. The general block diagram of MALTA3 can be seen in Fig. 3.

3.1. Asynchronous address generation

At the core of the Pixel groups found within the matrix, is the asynchronous reference pulse generator. This circuit is responsible for generating a pulse with a width of 0.5 ns to 2 ns when any of the pixels within the group register a hit. This pulse is then used to generate the address of the pixel in question, as well as a trigger for the synchronization memory. Based on a combination of chained inverters and standard delay cells, its performance was found to be inconsistent, generating pulses in the range of 2 ns to 5 ns. This increases the time a pixel address occupies the common bus, hence reducing the maximum theoretical throughput of the matrix. A new generator was designed, based around a starved inverter delay. It implements a feedback path,

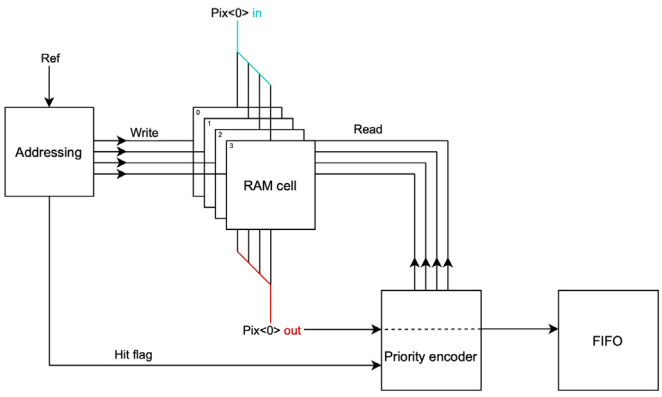

Fig. 4. MALTA3 synchronization memory operation.

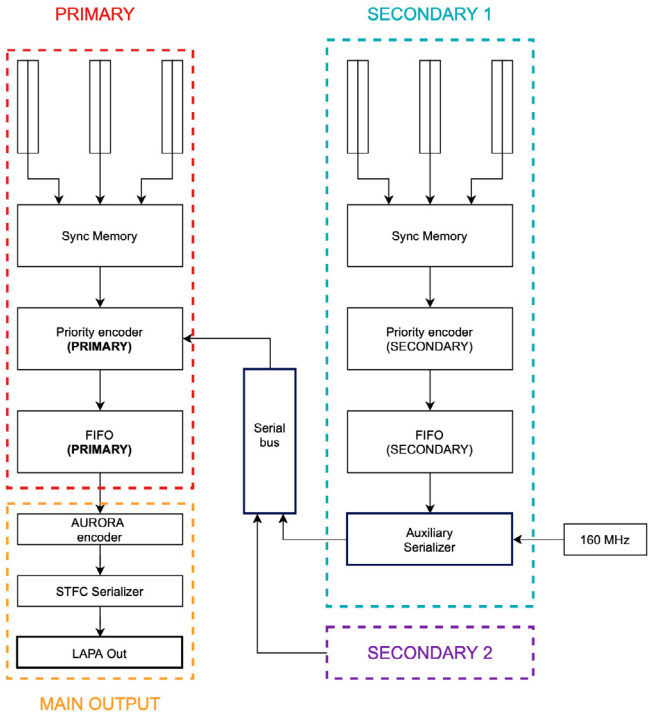

Fig. 5. MALTA3 chip to chip serial transmission concept.

so only one delay cell is used to generate two subsequent pulses. This saves valuable space within the pixel group, allowing for additional features such as a latch pixel masking to be implemented.

3.2. Synchronization memory

One of the main specifications of the MALTA3 chip is a sub-nanosecond timing resolution. This prompted an upgrade of the fine time counter. A 5 bit twisted ring gray encoded counter has been developed for this purpose, running at 1.28 GHz. It is constructed as digital block, containing exclusively standard 180 nm logic cells, in order to provide more flexibility for its integration in the top level. Another challenge of this module was creating a synchronized reset between it and the slower BCID counter, which was achieved at the cost of 5 160 MHz cycles. The reference bit of the hit is used to latch the writing into the RAM cells and reading from the priority encoder into the FIFO. The operation of the synchronization memory can be seen in Fig. 4.

3.3. Chip to chip data transfer

Chip to chip data transfer is an important concept in order to reduce the services on the detector. Previous submissions achieved this through an additional merging level and 40 parallel CMOS drivers on the side of the chip. In this case, the pixel hit words remain unchanged, and the primary chip is only used to pass the hit to the output LVDS drivers. This approach cannot be directly transferred to the synchronous periphery of MALTA3. As a solution, multiple slow serial links are proposed, each serving a predetermined part of the sensor. The data flow of secondary chips will be almost identical to their single-chip operation, but instead of using the high speed output, an auxiliary serializer will send the tagged hits out of the first stage FIFO towards the primary chip priority encoder. The data from the secondary and the primary chip are then combined in the first stage FIFO of the primary chip, and the data flow remains unchanged from that point onward. The conceptual operation of the chip to chip data transmission in MALTA3 can be seen in Fig. 5.

4. Conclusion

The discussed upgrades will first be implemented in a small scale demonstrator chip in 2022. The main purpose of this submission will be to test the new high speed synchronization memory, and produce a design that is scalable to the full size MALTA3 chip.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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