Nuclear Inst. and Methods in Physics Research, A 1040 (2022) 167224

Contents lists available at ScienceDirect

Nuclear Inst. and Methods in Physics Research, A

journal homepage: www.elsevier.com/locate/nima

Development and testing of a radiation-hard large-electrode DMAPS design in a 150 nm CMOS process

I. Caicedo [a,*], M. Barbero [b], P. Barrillon [b], C. Bespin [a], P. Breugnon [b], P. Chabrillat [b], Y. Degerli [c], J. Dingfelder [a], F. Guilloux [c], A. Habib [b], T. Hemperek [a], T. Hirono [a,1], F. Hügging [a], H. Krüger [a], P. Pangaud [b], A. Rozanov [b], P. Rymaszewski [a], L. Schall [a], P. Schwemling [c], M. Vogt [a], T. Wang [a,2], N. Wermes [a]

[a] Universität Bonn, Physikalisches Institut, Nußallee 12, 53115 Bonn, Germany
[b] Aix Marseille University, CNRS/IN2P3, CPPM, 163 Avenue de Luminy, Marseille, France
[c] IRFU CEA-Saclay, Batiment 141, Gif-sur-Yvette Cedex, France

ARTICLE INFO

Keywords:
Pixel detectors
DMAPS
Semiconductor detectors
Radiation hardness
TID
NIEL

ABSTRACT

The LF-Monopix chips are depleted monolithic active pixel sensors that follow the large-electrode design approach and implement a fast synchronous read-out architecture. They are designed in a 150 nm CMOS process and make use of large voltages (>250 V) and highly resistive substrates (>2 kΩ·cm) to collect charge through drift and enhance their radiation hardness.

Samples of the first prototype ("LF-Monopix1") with a thickness of 100 µm were irradiated to assess the tolerance of the chip's substrate and front-end circuitry to the surface and bulk damage doses expected at modern collider experiments. The device remained fully operational, with only a very small gain degradation and an increase in noise by less than 25% after a total ionizing dose of 100 Mrad. Efficiency measurements in a sample exposed to a neutron fluence of 1×10^{15} n_{eq}/cm^2 showed that at least 96% of all minimum ionizing particles going through a fully depleted detector are recorded in less than 25 ns. In the latest design ("LF-Monopix2") the column length was tripled and the pixel pitch reduced by 40% with respect to its predecessor. The chip was successfully thinned down while keeping its breakdown voltage above 400 V and achieving a front-end threshold dispersion of ∼100 e^- after tuning.

1. Introduction

Current and future particle collider experiments aim to make use of large areas of radiation-hard silicon tracker systems with high rate capability. A monolithic active pixel sensor designed in a commercial CMOS process would reduce the material budget and production complexity of pixel detectors by integrating the sensor and read-out electronics in a single piece of silicon [1]. In Depleted Monolithic Active Pixel Sensors ("DMAPS"), the radiation tolerance is enhanced through technology add-ons and careful design, which allow them to be biased with large voltages [2,3] and collect charge through drift in a highly resistive silicon substrate [4–7].

The Monopix chips [8,9] are large-scale DMAPS with fast column-drain read-out architectures. They were designed to meet the requirements of the outer layers of the ATLAS Inner Tracker ("ITk") at the HL-LHC [10]. In terms of radiation tolerance, these conditions correspond to a Total Ionizing Dose ("TID") of 80 Mrad and a Non-Ionizing Energy Loss ("NIEL") fluence of 10^{15} n_{eq}/cm^2.

2. The LF-Monopix DMAPS prototypes

The LF-Monopix detectors are fully functional DMAPS prototypes designed in a multi-well 150 nm CMOS process [11] with a high-resistivity (>2 kΩ·cm) p-type silicon substrate. The use of this technology made it possible to place and isolate each pixel's full front-end and read-out circuitry inside an n-type charge collection node of a size comparable to the pixel area. This approach (known as "Large-electrode DMAPS" and illustrated in Fig. 1) aims at achieving a strong and uniform electric field across the pixel, so that the collection drift paths are short and reduce the probability of charge trapping after irradiation. However, it requires special design efforts to deal with

* Corresponding author.
E-mail address: caicedo@physik.uni-bonn.de (I. Caicedo).
[1] Now at Center for Free Electron Laser Science (CFEL) DESY.
[2] Now at Zhangjiang Laboratory.

https://doi.org/10.1016/j.nima.2022.167224
Received 14 April 2022; Received in revised form 11 July 2022; Accepted 15 July 2022
Available online 20 July 2022

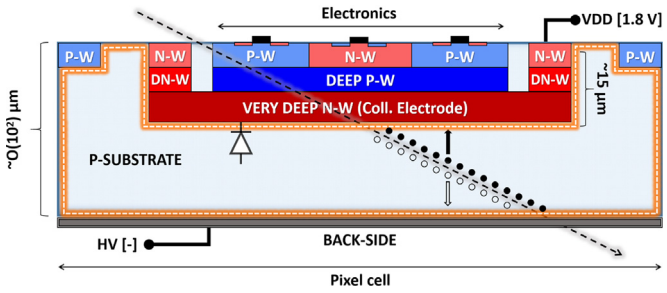

Fig. 1. Schematic profile of a large-electrode DMAPS design. The depletable volume is delimited by white dashed lines.

the drawbacks of the electrode size or the large detector capacitance associated with the placement of electronics within it ($C_d \sim \mathcal{O}(10^2\,\mathrm{fF})$). These effects include the possibility of switching digital signals coupling to the collection node, a large Equivalent Noise Charge ("ENC") and the slow rise time of small signals during amplification. The front-ends implemented in LF-Monopix were designed and optimized to comply with the "in-time" detection requirements of a collider experiment with bunch-crossing frequency of 40 MHz at the LHC.

The devices are preferably thinned-down in order to minimize multiple scattering, material budget and leakage current. Wafers of both LF-Monopix chips were back grinded using the TAIKO method [12]. In addition, their back-side was processed with plasma etching, acceptor ion implantation and aluminum metallization in order to avoid an increase in leakage current at full depletion (as those reported for unprocessed thin sensors in the same CMOS process in [13] or [14]). The reverse bias voltage is applied to the substrate from its back-side, either through a pad in the chip connected to the edge of the device or a pad in the printed circuit board that the chip is conductively glued to.

The design and overall performance of the first prototype – known as "LF-Monopix1"– have been thoroughly described in previous publications [15–18]. This chip has a total area of $1\,\mathrm{cm}^2$, where ~62% of it corresponds to the radiation sensitive matrix of 129×36 pixels with an individual pitch of $250 \times 50\ \mu\mathrm{m}^2$. For the sensor part, it showed a breakdown voltage of at least 260 V with a maximum leakage current of $\sim 0.1\,\mu\mathrm{A/cm}^2$ at room temperature. Different analog front-ends were tested in LF-Monopix1 to determine the combination of preamplifier and discriminator that performs best in terms of timing and radiation hardness. The charge sensitive amplifiers follow a folded cascode structure that uses either a single NMOS ("NMOS CSA") or both NMOS and PMOS ("CMOS CSA") transistors as input devices. As for the discriminator, one version ("V1") features a two-stage open loop amplifier, while the second ("V2") uses a self-biased differential amplifier with a CMOS inverter at the output stage.

In the second chip, called "LF-Monopix2", the length of the pixel column was extended from 0.6 cm to 1.7 cm and the pixel size was reduced to $150 \times 50\ \mu\mathrm{m}^2$ (the pixel layouts for both prototypes are shown in Fig. 2). These changes resulted in a matrix of 340×56 pixels. The main design of the analog front-end is based on the NMOS CSA and V2 discriminator previously tested in LF-Monopix1, although some modifications were added to certain columns as an attempt to improve its timing performance or threshold dispersion.

3. TID irradiation of LF-Monopix1

A 100 µm thick LF-Monopix1 chip was powered and exposed to the output spectra of an X-ray tube with a tungsten target and aluminum filter [19] in order to evaluate its tolerance to TID damage. The chip was uniformly irradiated at a rate of 0.6 Mrad/h up to a dose of 100 Mrad, while it was kept at a temperature of $0 \pm 2\,^{\circ}\mathrm{C}$ during the whole campaign. The irradiation was carried out in 15 dose steps, at the

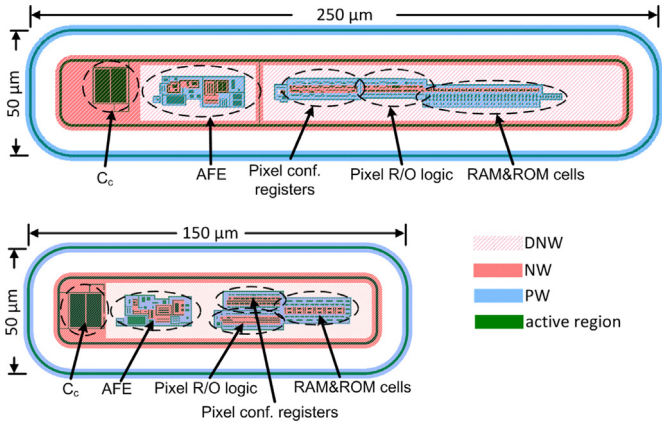

Fig. 2. Top view of the pixel layouts in LF-Monopix1 (top) and LF-Monopix2 (bottom).

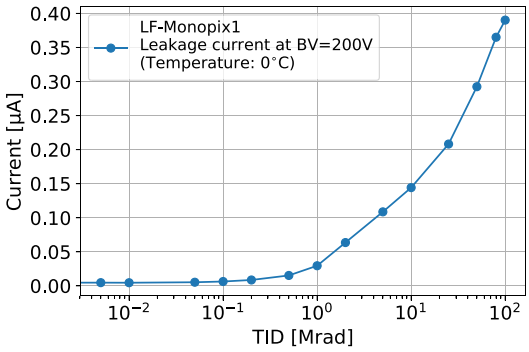

Fig. 3. Leakage current in a 100 µm thick LF-Monopix1 back-side biased with 200 V during the X-ray irradiation in steps up to a total TID of 100 Mrad.

end of which the leakage current of the sensor, power consumption and characteristic values of the different analog front-ends were measured independently. The leakage current at the substrate was recorded for bias voltages up to 200 V. As observed in Fig. 3, it increased by two orders of magnitude after a dose of 100 Mrad.

The currents of the digital, End-Of-Column and I/O power domains showed a similar behavior in all implementations, as illustrated (e.g.) for the pixel digital supply "VDDD" in Fig. 4. They started to increase after a dose of 200 krad and peaked at around 5 Mrad before they made a slow return to their original value by the end of irradiation. These measurements agree qualitatively with the behavior observed in test structures and ICs designed in commercial CMOS technologies of similar feature size [20–22]. In these devices, the threshold voltage of NMOS transistors decreases due to radiation-induced positive charges trapped in their STI oxide, an effect which is slowly compensated and eventually overcome by the build-up of negative charges at the interface with the silicon substrate.

In order to monitor the performance of the digital logic with respect to TID, the read-back reliability of the configuration shift register was tested for different voltages ("VDD") supplied to all power domains at every dose step. Fig. 5 shows the minimum VDD value, for which a pattern written to the pixel matrix could be fully recovered: This value remained close to 0.97 V during the whole irradiation campaign and is much lower than the default operational value of 1.8 V.

The gain and ENC were extrapolated from multiple threshold scans in different front-ends at every irradiation step. As illustrated in Fig. 6, the gain did not show a fluctuation larger than ~3% with respect to its original value in any front-end. Furthermore, Fig. 7 shows the noise behavior as a function of TID. A relative rise of ~15% in ENC was observed for the front-end with CMOS CSA and ~25% for the ones with NMOS CSA. It is important to remark that, even though the relative

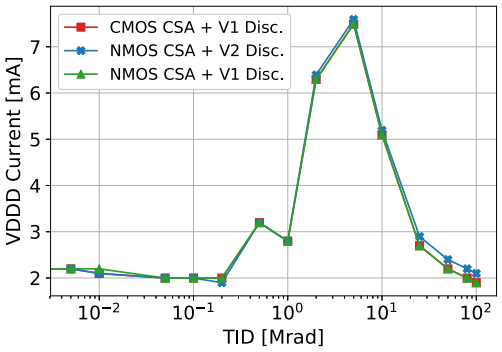

Fig. 4. Measured current in the digital power domain (VDDD) of different front-ends implemented in LF-Monopix1 as a function of TID.

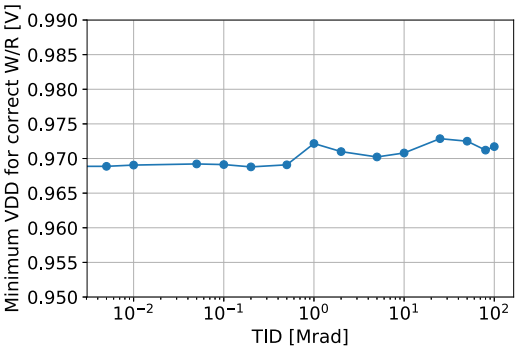

Fig. 5. Evolution with TID of the minimum voltage required in all power domains for proper read-back of configuration bits written to the LF-Monopix1 pixel matrix. The default value for all domains is 1.8 V.

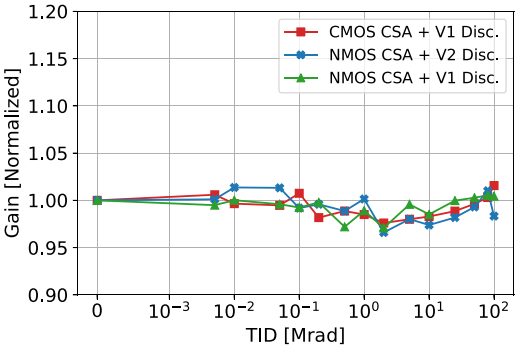

Fig. 6. Normalized gain of different front-ends implemented in LF-Monopix1 with respect to TID.

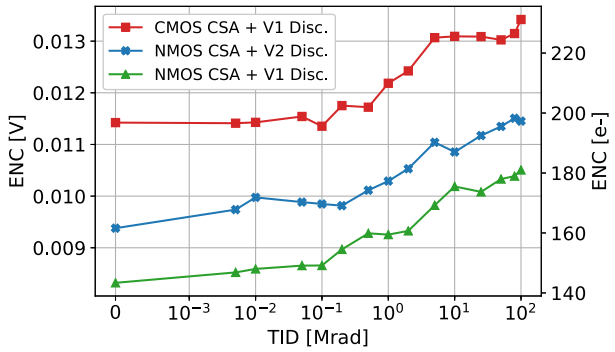

Fig. 7. Evolution of the Equivalent Noise Charge of different front-ends implemented in LF-Monopix1 with respect to TID.

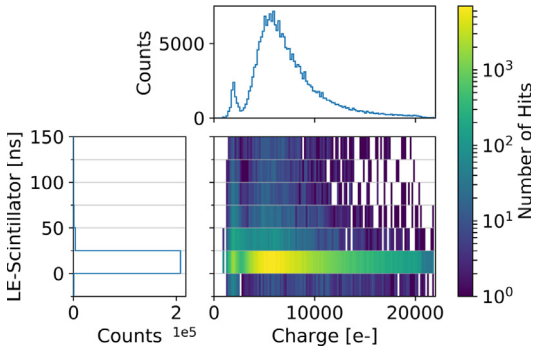

Fig. 8. Time walk of seed pixel hits recorded in a 100 µm thick LF-Monopix1 after a NIEL fluence of 1×10^{15} n_{eq}/cm^2. The projections of both axes include all charge or time bins. The chip was exposed to a 5 GeV e^- beam. Threshold: 2.3 ke^-. Bias voltage: 150 V.

change was larger in the pixels with NMOS CSA, their final nominal value still remained below that of the CMOS CSA. These increases in ENC could be linked to leakage-induced shot noise in the front-end or an observed degradation of the biasing circuitry (whose settings can be readjusted for compensation, but were kept intentionally fixed during irradiation).

4. NIEL damage and timing performance of LF-Monopix1

A hit detection efficiency larger than 99% has previously been reported for LF-Monopix1 devices irradiated with neutrons up to a NIEL fluence of 1×10^{15} n_{eq}/cm^2 at the JSI TRIGA reactor [23]. This value was measured for (1) 725 µm samples using the front-end with CMOS CSA and discriminator V1 [24], and (2) thinned 100 µm samples using the front-end with NMOS CSA and discriminator V2 [25]. The second measurement was of particular interest for the development of LF-Monopix2, since it was done with a fully depleted thin sensor and the front-end that showed the smallest difference ("Overdrive") between in-time and overall threshold in LF-Monopix1 [18]. In addition to the calculation of hit detection efficiency, the same data from a 5 GeV electron test beam campaign at DESY [26] was used to determine the fraction of hits from minimum ionizing particles detected within a time window of 25 ns in a 100 µm thick sample.

A high detection efficiency was still achievable in the thin chip since the amount of charge collected at full depletion (MPV ~ 5.5 ke^-, before and after NIEL damage) was large enough with respect to the operational threshold (~2.3 ke^-, for an irradiated chip at −20 °C). In order to determine the fraction of particles detected within 25 ns, the time difference between the rising edges of hits above threshold in the chip and the signal of the scintillator used as trigger for all devices in the beam was recorded. A map of this variable (known as "time walk") with respect to the charge of the pixels with the largest signal in each event is shown in Fig. 8. 97.1% of all efficient events were in-time for the neutron irradiated chip.

A selection of events in LF-Monopix1 with a time walk below 25 ns was added to the criteria used to calculate the detection efficiency of the chip in the software package used for test beam analysis [27]. The in-time efficiency map for the neutron irradiated sample (projected into a 2 × 2 pixel array) is shown in Fig. 9. The efficiency is uniform across most of the pixel area, with the exception of drops at the corners where the signal decreases due to charge sharing. A mean in-time efficiency of 96.6% was measured for all enabled pixels (~10^4), which is only 0.6% smaller than the one observed in an unirradiated device. This result is very encouraging, since it proves that a DMAPS with large-electrode design (C_d ~ 400 fF) can achieve a good timing performance.

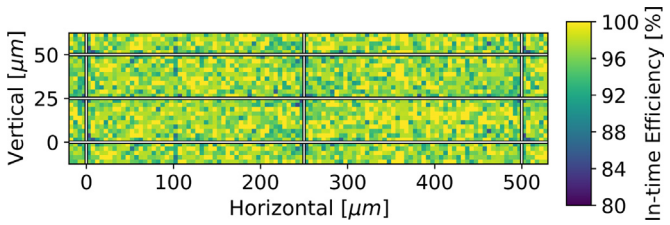

Fig. 9. In-time efficiency map of a 100 μm thick LF-Monopix1 after a NIEL fluence of 1×10^{15} n_{eq}/cm^2 (data from $\sim 10^4$ pixels projected onto a 2 × 2 pixel array). The chip was exposed to a 5 GeV e^- beam. Threshold: 2.3 ke^-. Bias voltage: 150 V.

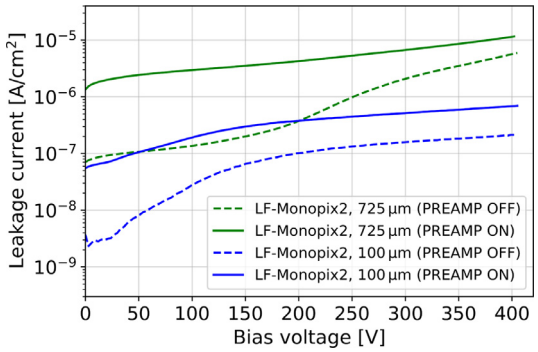

Fig. 10. I-V curves of LF-Monopix2 devices of different thickness. The leakage current was divided by the total area of the chip (1.78 cm^2). Dashed or full lines correspond to the cases where the analog circuitry of the full pixel matrix is disabled or enabled, respectively.

5. Initial measurements in thin LF-Monopix2 devices

Some initial measurements in unthinned (725 μm) LF-Monopix2 devices have already been reported for its main front-end in [25]: An ENC of $\sim 100 \pm 20\, e^-$ (~30% smaller than the one measured for the same design in LF-Monopix1) and no sign of breakdown up to a bias voltage of 320 V.

Fig. 10 shows the IV-curves measured in unthinned and 100 μm thick back-side processed LF-Monopix2 chips at room temperature before irradiation. The curves were measured with and without all preamplifiers in the matrix enabled, where the change in leakage from one case to the other is linked to the variation in temperature of the chip. There was a decrease in leakage current of one order of magnitude after thinning and no breakdown was observed while scanning the bias voltage up to 400 V. These observations show that the electric field across the bulk can be reliably increased far above the full depletion voltage of a 100 μm thick DMAPS with this resistivity (~15 V) while its leakage current remains below 1 μA/cm^2.

In LF-Monopix2, the untuned dispersion of the threshold at the unbiased condition of the main front-end is $\sim 700\, e^-$, a value ~25% smaller than the one measured in LF-Monopix1. In addition, a 4-bit current DAC ("TDAC") is used in both chips to reduce the overall dispersion by adjusting the threshold of the discriminator at every pixel. Fig. 11 shows that a tuned threshold distribution with a dispersion of $\sim 100\, e^-$ can be obtained for all pixels that use the main front-end design (~57% of the matrix). The stacked histogram shows that the whole TDAC range was used and its final values were normally distributed. This result was achieved in an unirradiated chip by making use of only 1/3 of the maximum current available to bias the TDAC, which means that the chip still has a wide range for threshold compensation if the raw dispersion increases or the DAC reference current degrades after irradiation.

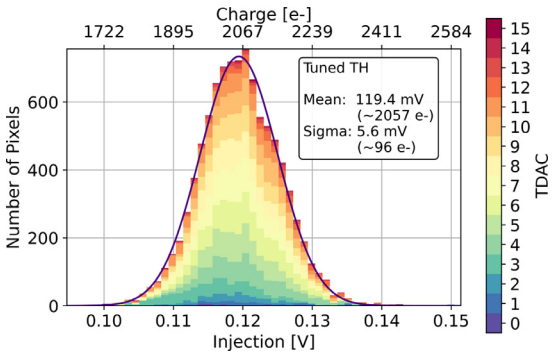

Fig. 11. Tuned threshold distribution of $\sim 10^4$ pixels in LF-Monopix2. The colors in the stacked histogram are associated with the final DAC value of the threshold tuning circuit in every pixel.

6. Conclusions

The radiation hardness of LF-Monopix1, a large-electrode DMAPS design in a 150 nm CMOS process, has been tested up to the surface and bulk damage levels expected in modern particle collider experiments. The chip was fully operational across all stages of an X-ray irradiation campaign that reached a TID of 100 Mrad, while showing an increase of 2 orders of magnitude in the substrate leakage current and 15 – 25% in the ENC of its multiple analog front-end versions. Moreover, samples exposed to a NIEL fluence of 1×10^{15} n_{eq}/cm^2 showed an in-time efficiency of 96.6% during a 5 GeV electron test beam campaign. The front-end with the best compromise between radiation hardness and timing (NMOS CSA with discriminator V2) was chosen as the baseline design for LF-Monopix2.

Initial measurements in LF-Monopix2 showed that the chip can be back-side processed and thinned down to 100 μm while keeping the leakage current below 1 μA/cm^2 and the breakdown voltage above 400 V. The threshold distribution of the pixels in the chip can be tuned reliably to reach a dispersion of $\sim 100\, e^-$. From these results, a positive outlook for the performance of LF-Monopix2 after TID and NIEL damage can be given, based on the assumption that its main front-end design remains as radiation-hard as measured for its predecessor. On top of expecting the relative changes in leakage current and ENC to be the same after irradiation, the performance might improve with respect to the first prototype since its pre-irradiation values have already benefited from design optimization and the reduction in pixel size.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgments

This project has received funding from the Deutsche Forschungsgemeinschaft DFG (grant WE 976/4-1), the German Federal Ministry of Education and Research BMBF (grant 05H15PDCA9) and the European Union's Horizon 2020 Research and Innovation programme under grant agreements No. 675587 (STREAM), 654168 (AIDA-2020) and 101004761 (AIDA-Innova). The measurements leading to these results have partially been performed at the Test Beam Facility in DESY Hamburg (Germany), a member of the Helmholtz Association (HGF).

References

[1] R. Turchetta, et al., A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI CMOS technology, Nucl. Instrum. Methods Phys. Res. A 458 (3) (2001) 677–689, http://dx.doi.org/10.1016/s0168-9002(00)00893-7.

[2] I. Perić, A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology, Nucl. Instrum. Methods Phys. Res. A 582 (3) (2007) 876–885, http://dx.doi.org/10.1016/j.nima.2007.07.115.

[3] M. Kiehn, et al., Performance of CMOS pixel sensor prototypes in AMS H35 and aH18 technology for the ATLAS ITk upgrade, Nucl. Instrum. Methods Phys. Res. A 924 (2019) 104–107, http://dx.doi.org/10.1016/j.nima.2018.07.061.

[4] M. Havránek, et al., DMAPS: a fully depleted monolithic active pixel sensor—analog performance characterization, J. Instrum. 10 (02) (2015) P02013, http://dx.doi.org/10.1088/1748-0221/10/02/p02013.

[5] T. Hirono, et al., CMOS pixel sensors on high resistive substrate for high-rate, high-radiation environments, Nucl. Instrum. Methods Phys. Res. A 831 (2016) 94–98, http://dx.doi.org/10.1016/j.nima.2016.01.088.

[6] W. Snoeys, et al., A process modification for CMOS monolithic active pixel sensors for enhanced depletion, timing performance and radiation tolerance, Nucl. Instrum. Methods Phys. Res. A 871 (2017) 90–96, http://dx.doi.org/10.1016/j.nima.2017.07.046.

[7] L.F.S. de Acedo, et al., Design of large scale sensors in 180 nm CMOS process modified for radiation tolerance, Nucl. Instrum. Methods Phys. Res. A 980 (2020) 164403, http://dx.doi.org/10.1016/j.nima.2020.164403.

[8] K. Moustakas, et al., CMOS monolithic pixel sensors based on the column-drain architecture for the HL-LHC upgrade, Nucl. Instrum. Methods Phys. Res. A 936 (2019) 604–607, http://dx.doi.org/10.1016/j.nima.2018.09.100.

[9] T. Wang, et al., Depleted monolithic active pixel sensors in the LFoundry 150 nm and TowerJazz 180 nm CMOS technologies, in: Proceedings of the 28th International Workshop on Vertex Detectors — PoS(Vertex2019), Sissa Medialab, 2020, http://dx.doi.org/10.22323/1.373.0026.

[10] The ATLAS Collaboration, Technical Design Report for the ATLAS Inner Tracker Pixel Detector, Tech. Rep., CERN, Geneva, 2017, URL https://cds.cern.ch/record/2285585.

[11] LFoundry Srl, Company website, 2022, URL http://www.lfoundry.com/.

[12] DISCO Corporation, Company website, 2022, URL https://www.disco.co.jp/eg/solution/library/grinder/taiko_process.html.

[13] D.-L. Pohl, et al., Radiation hard pixel sensors using high-resistive wafers in a 150 nm CMOS processing line, J. Instrum. 12 (06) (2017) P06020, http://dx.doi.org/10.1088/1748-0221/12/06/p06020.

[14] L. Diehl, et al., Characterization of passive CMOS strip sensors, Nucl. Instrum. Methods Phys. Res. A 1033 (2022) 166671, http://dx.doi.org/10.1016/j.nima.2022.166671.

[15] P. Rymaszewski, et al., Development of depleted monolithic pixel sensors in 150 nm CMOS technology for the ATLAS inner tracker upgrade, in: Proceedings of Topical Workshop on Electronics for Particle Physics— PoS, TWEPP-17, Sissa Medialab, 2018, http://dx.doi.org/10.22323/1.313.0045.

[16] I. Caicedo, et al., The Monopix chips: depleted monolithic active pixel sensors with a column-drain read-out architecture for the ATLAS inner tracker upgrade, J. Instrum. 14 (06) (2019) C06006, http://dx.doi.org/10.1088/1748-0221/14/06/c06006.

[17] C. Bespin, et al., DMAPS Monopix developments in large and small electrode designs, Nucl. Instrum. Methods Phys. Res. A 978 (2020) 164460, http://dx.doi.org/10.1016/j.nima.2020.164460.

[18] M. Barbero, et al., Radiation hard DMAPS pixel sensors in 150 nm CMOS technology for operation at LHC, J. Instrum. 15 (05) (2020) P05013, http://dx.doi.org/10.1088/1748-0221/15/05/p05013.

[19] Silizium Labor (University of Bonn), X-ray irradiation machine, 2019, URL https://github.com/SiLab-Bonn/X-ray_machine/wiki.

[20] L. Gonella, et al., Total ionizing dose effects in 130-nm commercial CMOS technologies for HEP experiments, Nucl. Instrum. Methods Phys. Res. A 582 (3) (2007) 750–754, http://dx.doi.org/10.1016/j.nima.2007.07.068.

[21] F. Faccio, et al., Total ionizing dose effects in shallow trench isolation oxides, Microelectron. Reliab. 48 (7) (2008) 1000–1007, http://dx.doi.org/10.1016/j.microrel.2008.04.004.

[22] K. Dette, Total ionising dose effects in the FE-I4 front-end chip of the ATLAS pixel IBL detector, J. Instrum. 11 (11) (2016) C11028, http://dx.doi.org/10.1088/1748-0221/11/11/c11028.

[23] L. Snoj, G. Žerovnik, A. Trkov, Computational analysis of irradiation facilities at the JSI TRIGA reactor, Appl. Radiat. Isot. 70 (3) (2012) 483–488, http://dx.doi.org/10.1016/j.apradiso.2011.11.042.

[24] T. Hirono, et al., Depleted fully monolithic active CMOS pixel sensors (DMAPS) in high resistivity 150 nm technology for LHC, Nucl. Instrum. Methods Phys. Res. A 924 (2019) 87–91, http://dx.doi.org/10.1016/j.nima.2018.10.059.

[25] J. Dingfelder, et al., Progress in DMAPS developments and first tests of the Monopix2 chips in 150 nm LFoundry and 180 nm TowerJazz technology, Nucl. Instrum. Methods Phys. Res. A 1034 (2022) 166747, http://dx.doi.org/10.1016/j.nima.2022.166747.

[26] R. Diener, et al., The DESY II test beam facility, Nucl. Instrum. Methods Phys. Res. A 922 (2019) 265–286, http://dx.doi.org/10.1016/j.nima.2018.11.133.

[27] Y. Dieter, J. Janssen, D.-L. Pohl, BTA: A testbeam analysis software written in Python and C++. [Computer Software], 2022, URL https://github.com/SiLab-Bonn/beam_telescope_analysis. (Accessed 31 March 2022).