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# A series-connected switched source and an H-bridge based multilevel inverter

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**ABSTRACT**

An inverter circuit is promoted in this paper, using series-connected switched dc sources along with an H-bridge circuit with optimized circuit elements like switching devices and diode clamped (DC) sources. This configuration uses DC supplies that can be strung together in series to create a significant voltage level. This topology consists of two parts, namely: 1) level production part and 2) polarity production part. The combination of some of the dc sources and switching devices completes the level production part. The H-bridge in the presented structure produces the polarity generation part. The DC-link capacitors are not needed in this design. There is a full presentation of the operating modes and modeling process of the proposed converter. Finally, in the MATLAB/SIMULINK setting the proposed topology is simulated and output current and voltage results have been examined.



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## 1. INTRODUCTION

Series-connected switched diode clamped-anode clamped (DC-AC) converters are highly flexible and modular in the family of multilevel inverters. In this group, "cascaded H-bridge (CHB)" converters 11]-[3] are the classical and traditional types. CHB converters have the advantages of equal voltage stress in symmetrical configurations, easy to add/remove the H-bridges to increase/decrease the number of output voltage levels. Multi-layer insulation (MLI) technology is spreading to several areas such as AC drives, static reactive compensators, micro-grid systems and renewable energy sources [4]-[6]. The "neutral point clamped (NPC)" or "diode clamped (DC)", "flying capacitor clamped (FCC)", and CHB converters [7]-[9] are established as standard topologies in the MLI family. In these configurations, the device count increases exponentially w.r.t the number of levels in the output voltage, the requirement of unequal voltage ratings of the clamping diodes, unequal capacitor size and a greater number of dc sources puts limitations on these topologies. Several new MLI configurations with the intention of avoiding the drawbacks in the standard topologies were proposed in the literature for several applications [10], [11]. In recent times, cascaded converters are attracting attention from industries as well as academia. Several such "voltage source inverters (VSIs)" were proposed in the literature [12]-[15] by employing several combinations of switches, DC power supplies. The converter has the advantages of reducing the number of components and reduced blocking voltage over the switching units to reduce the cost. In this configuration, the rest of the paper is arranged is being as: section 2 describes work and operating modes, section 3 presents the

modulation theory for generating the necessary output voltage, section 4 demonstrates the justification by different types of modulation index of the proposed converter, and section 5 concludes finally.

## 2. SYSTEM CONFIGURATION

Figure 1 shows the suggested converter. It's essentially a single-phase AC power supply voltage at nine levels. The converter uses four isolated powers supplied and eight bi-directional conducting switches. Although the switching systems have two-directional driving characteristics, they only block the voltage in one direction because of anti-parallel diodes. The proposed architecture can leverage four different DC sources produced either from battery systems or photovoltaic (PV) systems.

The switching conditions of positive and negative zero voltage crossings are shown in Figures 2(a) and 2(b) respectively. The output voltage at a positive zero-crossing is represented by the symbol $V_0 = 0^+$ and similarly $V_0 = 0^-$ represents the output voltage negative zero-crossing. It is necessary to apply both switching states equally in direction to keep the temperature, increase in entirely switches, and all of the switching devices for being equal. A positive-level voltage is generated entire the outcome side of the converter represented in Figure 3, which is the operation of the converter under consideration. As shown in Figure 3(a), the power semiconductor devices (IGBTs) $S_1$, $S_5$, and $S_8$ operate in the same operating mode as when $V_0 = V_{dc}$ is generated. This operating mode causes the IGBTs $S_2$, $S_5$, and $S_8$ to conduct. In Figure 3(b) generates $V_0 = 2V_{dc}$, and the IGBTs $S_2$, $S_5$, and $S_8$ conduct in this operating mode and Figure 3(c) depicts the maximum voltage of $V_0 = 3V_{dc}$. It indicates that the IGBTs $S_3$, $S_5$, and $S_8$ are operational in this operating mode. Figure 3(d) depicts the maximum voltage of $V_0 = 4V_{dc}$, which indicates that the IGBTs $S_4$, $S_5$, and $S_8$ are operational in this operating mode. Figure 4 illustrates the different working converter's modes that are used toward generate negative output voltage levels. As given in Figure 4(a), when $V_0 = -V_{dc}$ is generated. The IGBTs $S_4$, $S_1$, $S_6$ and $S_7$ are activated in this operating mode. Figure 4(b) shows the output voltage $V_0 = -2\ V_{dc}$, which corresponds to the time period during which the IGBTs $S_2$, $S_6$, and $S_7$ are turned on. During this interval, the IGBTs $S_3$, $S_6$, and $S_7$ are turned on because of the output voltage $V_0 = -3\ V_{dc}$ produced by Figuer 4(c). The output voltage $V_0 = -4\ V_{dc}$ is shown in Figure 4(d), and the IGBTs $S_4$, $S_6$ and $S_7$ are turned on throughout this time period.

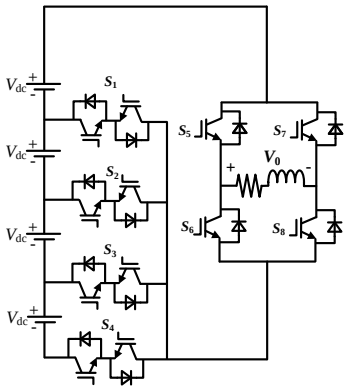


Figure 1. Schematic diagram of the proposed module

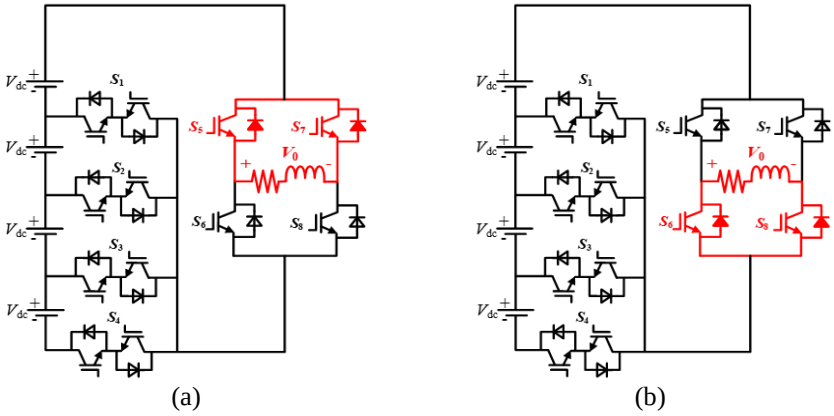


Figure 2. Zero crossover operating modes; (a) $V_0 = 0^+$, (b) $V_0 = 0^-$

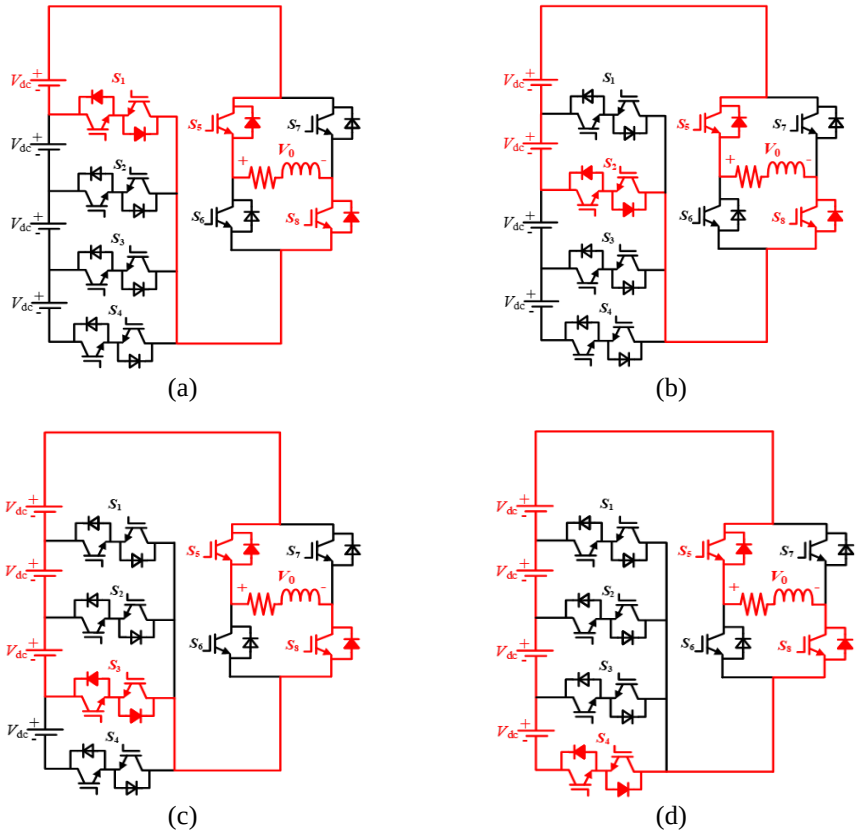


Figure 3. Positive-level operating modes; (a) $V_0 = V_{dc}$, (b) $V_0 = 2V_{dc}$, (c) $V_0 = 3V_{dc}$, (d) $V_0 = 4V_{dc}$

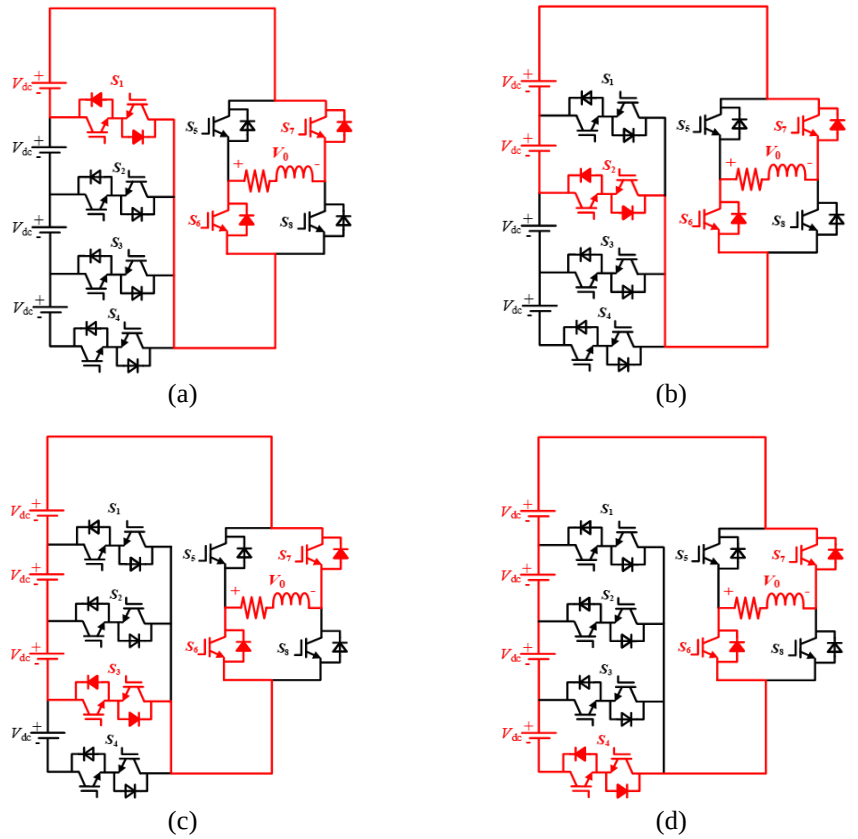


Figure 4. Negative voltage levels for operation modes; (a) $V_0 = -V_{dc}$, (b) $V_0 = -2V_{dc}$, (c) $V_0 = -3V_{dc}$, (d) $V_0 = -4V_{dc}$

## 3. MODULATION TECHNIQUE

For the purpose of providing a more accurate explanation of the switching conditions and on and off modes of the switches in the presented converter at various output voltage values is given in Table 1. Figure 1 IGBTs' on/off states are indicated and shwon Table 1 with 1 and 0 respectively. Examine that the H-bridge switches $S_5$, $S_6$, S7, and $S_8$ are running at lower switching frequency than the other H-bridge switches, as a result of which the switching losses are reduced. Figure 5 shows the modulation method [16]-[18] in the suggested topology for the generation of gate pulse to IGBTs [16]-[18]. 8-triangular waveforms are stacked on top of each other with a sinusoidal waveform on top. The sine wave is known as a wave reference and carrier wave is represented by triangular wave.

The reference wave is impacted by each carrier wave at certain intervals that are shown as 1, 2, 3, 4, 1', 2', 3', and 4'. Therefore, the pulses produced are P1-P4 and N1-N4 because of the interactions among the carrier and reference waves. These pulses are efficiently used to generate the nine-level output voltage via logical gate circuits. In the following terms is defined the "modulation index (M.I.)" that represents the number of output levels [19]:

$$M.I.= \frac{V_{0peak}}{4\times V_{dc}} \quad (1)$$

Table 1. Switching sequence of the inverter

| Output Voltage level ($V_O$) | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 |
|---|---|---|---|---|---|---|---|---|
| $4V_{dc}$ | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| $3V_{dc}$ | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| $2V_{dc}$ | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| $V_{dc}$ | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| $0^+$ | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| $0^-$ | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| $-V_{dc}$ | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| $-2V_{dc}$ | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| $-3V_{dc}$ | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| $-4V_{dc}$ | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |

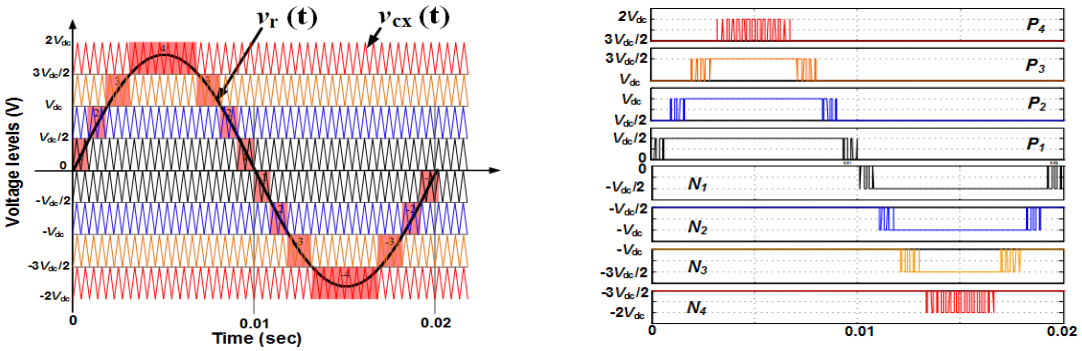


Figure 5. Sine-triangle comparison PWM scheme

## 4. SIMULATION RESULTS

The proposal's functionality is demonstrated using "MATLAB" simulation [20]-[22] and is validated to show how it will perform. According to the simulation, the resulting output voltage is expected to be 230 volts and 50 Hertz. Parameters evaluated for simulation work also feature alternative values in Table 2. The M.I. of 0.9 may be seen in Figure 6(a), where it shows the inverter output voltage and the matching current waveforms. The 9-level voltage signal is shown, along with the current. It is evident that the M.I. decrease reduces the output voltage maximum value ($V_{0peak}$). Figure 6(b) shows the output waveform spectrum of the FFT at various M.I values. When the converter is modulated at 0.9, $V_{0peak}$ is detected as 361 V, with the "total harmonic distortion (THD)" being 16.6% and the harmonic spectrum of the current output waveforms is displayed in Figure 6(c). A value of 6.4 A with a modulation of 0.9 and THD of around 0.5% is observed in the $I_{0peak}$ value. The current waveform and "inverter output voltage" for an M.I. is displayed at 0.7 in Figure 7(a) and the associated load current for that seven-level output voltage waveform. It is evident that the M.I. decrease reduces the output voltage maximum value ($V_{0peak}$). The drop in M.I. leads to a growth in THD because the voltage voltage level in Figure 7(b) is reduced as shown (b). The voltage, $I_{0peak}$ value, falls by

around 0.7 in M. I., the $I_{0peak}$ value, and THD is around 0.6% in Figure 7(c) (see Appendix). The voltage, $I_{0peak}$ values are decreased by about 0.6% [23]-[25].

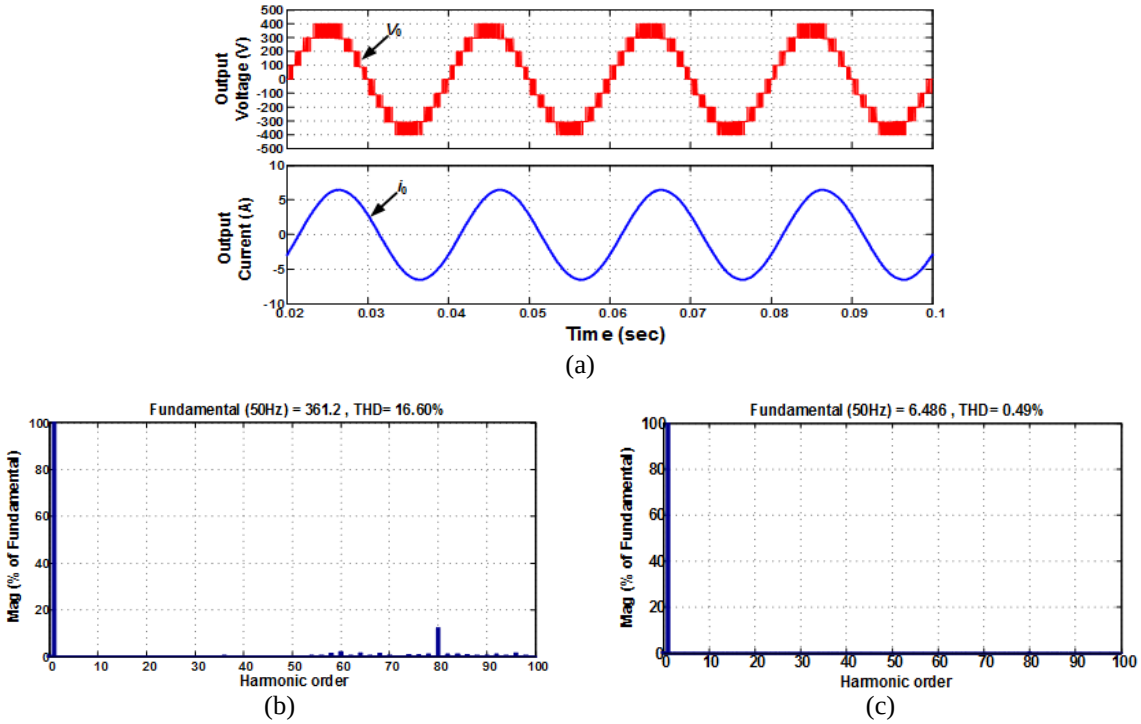


Figure 6. Simulink results of the converter at a peak reference of *0.9*; (a) converter voltage and current waveforms at the output, (b) FFT spectrum of $V_0$, (c) FFT analysis of $I_0$

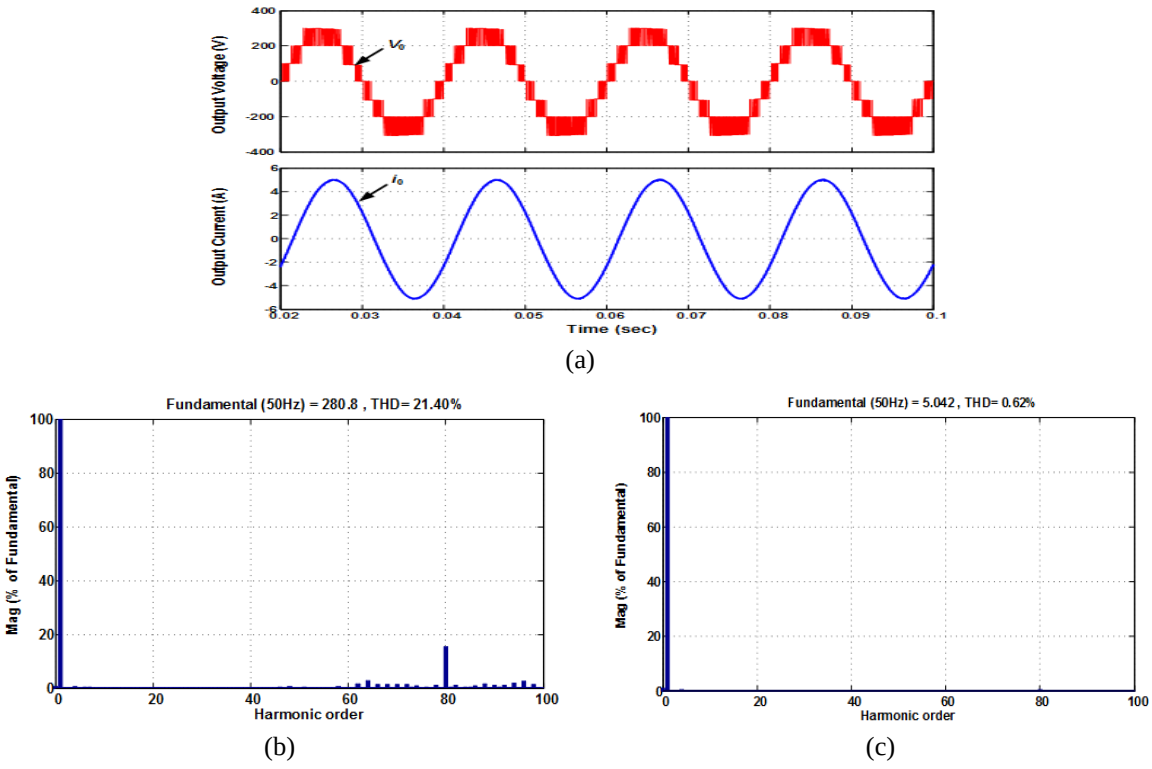


Figure 7. Simulink outcome; (a) converter voltage and current waveforms at the output, (b) FFT spectrum of $V_0$, (c) FFT analysis of $I_0$

Table 2. Design spefcations

| Specfications | Values | |
|---|---|---|
| | M.I. = 0.9 | M.I. = 0.7 |
| $V_{dc}$ (V) | 200 V | 200 V |
| $P_{output}$ (W) | 1070 | 650 |
| $V_0$ (V) | 260 | 203 |
| $I_0$ (A) | 4.5 | 3.5 |
| Switching frequency ($f_{sw}$) | 4 kHz | 4 kHz |
| Fundamental frequency ($f_m$) | 50 Hz | 50 Hz |

## 5. CONCLUSION

The focus of this article is on a novel MLI topology used in the nine-level DC-AC converter family. The presented architecture is the most active group recently made by switched dc source cell and H-bridge, in order to optimise the number of segments in a specific inverter topology. To generate the zero, positive, and negative levels, a complete analysis as well as operating modes have been provided. In the suggested architecture, the H-bridge switches run at an essential frequency, and do so at a lower switching frequency. This results in switching losses that are significantly lower than those of numerous MLI designs, which in turn increases the overall efficiency of the presented system, as presented in the topology. The sinusoidal PWM approach, which is the most effective and least complex, is used to create the firing pulses. For the configuration, it has been demonstrated that the findings of the MATLAB/SIMULINK simulations are true for modulation indexes of 0.9 and 0.7. This graph depicted the total harmonic distortion (THD) content of the output current and voltage waveforms, and the output voltage THD content was found to be significantly lower than the industry standard limits.

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