

## Proportional-integral-derivative controller design for time-delay systems via stability region centroid

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### ABSTRACT

Design of proportional-integral-derivative (PID) controller with proportional, integral, and derivative gains given by  $k_p$ ,  $k_i$  and  $k_d$  respectively, for time-delay systems is presented in this study. The centroid of the convex stability region (CCSR) method in the  $k_i$ - $k_d$  plane for fixed  $k_p$  is used. PID controller design for time-delay systems in the  $k_p$ - $k_i$  plane for a fixed  $k_d$  and  $k_i$ - $k_d$  plane for a fixed  $k_p$  have been extensively researched. Despite the amenability of CCSR method to design of PID controller in the  $k_i$ - $k_d$  plane for fixed  $k_p$ , its application in this regard has not been given serious attention. The stability region in  $k_i$ - $k_d$  plane for fixed  $k_p$  was determined and the required controller gains in the region were determined using the CCSR method. Using the determined controller gains, the system closed loop unit step response for all the considered regions was plotted on same axes. Based on the obtained results, different combinations of controller gains can be implemented depending on the system time domain performance measures (TDPMs) requirements. However, selection of an appropriate controller gains combinations, requires compromise among any of the conflicting TDPMs.

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## 1. INTRODUCTION

Time-delay is an inherent part of all practical control systems [1]-[3] and it may be caused by the time required for processing and/or transmitting of signals in the control loop [4], [5]. To design controllers for these group of systems, full understanding of the effects of time-delay on the system performance is required. Time-delay can reduce system quality of performance or cause system instability in worse case [6]. PID controller is generally used to control this class of systems due to its popularity [7], [8], simplicity [9], robustness and easy to use [10]-[12].

In PID controller design for time-delay systems, the first step is to establish the stability boundary for the system in its parameter space [13]. This is because such design is normally carried out using stability locus method [14]. This area of knowledge has been extensively researched. The method of computing all the stabilizing PID controller gains for a linear arbitrary order system with time-delay in the  $k_i$ - $k_d$  plane with fixed  $k_p$  was reported in [7]. More so, the procedure for the computation of the entire stability gains in the  $k_i$ - $k_p$  plane with fixed  $k_d$  was presented in [15]. The stabilization controller parameters for a time-delay integral fractional-order system under the control of fractional-order PID controller were determined in the  $k_i$ - $k_p$  stability region for a given  $k_d$ , as reported in [16]. The controller gains in the  $k_i$ - $k_p$  plane for a given  $k_d$  yielded

general stability region while the global stability region was obtained after sweeping over the permissible value of  $k_d$ . In [17], [18] parametric methods were used to establish the stability region in the  $k_i$ - $k_d$  and  $k_p$ - $k_i$  planes for a fixed  $k_p$  and  $k_d$ , respectively. Then GA was used to determine the optimum controller gains in the established region of the plane.

PID parameters for second-order plant with time-delay system was obtained by [15] in the  $k_p$ - $k_i$  plane with a fixed  $k_d$  for specified gain and phase margins using dominant poles method. PID controller tuning method for integrating system with time-delay and inverse response was developed in  $k_p$ - $k_i$  stability region for a fixed  $k_d$  in [19]. After determining the stability region, weighted geometrical center (WGC) approach was used to determine the required  $k_p$  and  $k_i$  gains for a given  $k_d$ . Though the method produced good results, it is computationally intensive. PI-PD controller for time-delay systems was tuned by [20] using WGC method which yields satisfactory performance compared to some other methods in the literature. In [14] CCSR method for PI-PD controller design was proposed for unstable systems with time-delay. Both the experimental and simulation results shows that the method is superior to some of the others reported in the literature. The method is simple, less computational and with satisfactory performance.

All the reviewed PID controller design methods were carried out either in the  $k_i$ - $k_d$  plane with a fixed  $k_p$  [21] or in the  $k_p$ - $k_i$  plane for a fixed  $k_d$  [22]. The CCSR method has several merits [14]; however, it is seldom applied in PID controller design. Its application in PI-PD controller design can be extended to PID controller design in the  $k_p$ - $k_i$  plane for a fixed  $k_d$  due to their  $k_i$ - $k_p$  stability locus similarity. The method is amenable to the stability region in the  $k_i$ - $k_d$  plane for fixed  $k_p$  being a convex polygon. Despite the amenability of CCSR design method, its application has not been extensively explored in the research community, hence the need for this study.

A PID controller design for time-delay system in  $k_i$ - $k_d$  plane with a fixed  $k_p$  using the CCSR method is reported in this study. The equations relating controller gains, system parameters and time-delay were derived; and then used for plotting the stability boundaries in  $k_i$ - $k_d$  plane for fixed  $k_p$ . Thereafter the centroids of the stability region, the required controller gains, were calculated. Using the calculated controller gain, the fixed  $k_p$ , the system and time-delay transfer functions, the closed-loop unit step response were plotted for all the generated stability regions on the same axes. The required TDPMs for characterising the designed systems were obtained from its closed loop step response plots.

Based on the TDPMs obtained for the various combinations of controller gains, a unique gain combination can be selected for a system considering its performance specifications. In practice, conflicts do exist among the TDPMs; therefore, a compromise is made when selecting any of the controller gains combinations.

## 2. METHOD

### 2.1. Determination of stability region in the $k_i$ - $k_d$ plane for fixed $k_p$

The closed-loop transfer function required for the analysis and design of PID controlled time-delay system can be derived from the block diagram of unity feedback control system shown in Figure 1. In Figure 1,  $R(s)$ ,  $E(s)$  and  $Y(s)$  is the reference input, error, and output respectively. The expressions for the plant, time-delay and controller transfer function are given in (1), (2) and (3) respectively.

$$G_p(s) = \frac{N(s)}{D(s)} \quad (1)$$

where,  $N(s)$  and  $D(s)$  is the plant transfer function numerator and denominator respectively.

$$G_d(s) = e^{-\tau s} \quad (2)$$

where,  $\tau$  is the time-delay in seconds.

$$G_c(s) = \frac{k_d s^2 + k_p s + k_i}{s} \quad (3)$$

The expression in (1) was decomposed into its even and odd parts after substituting  $j\omega$  for  $s$  as shown in (4) for easy application of D-decomposition method [23]. The  $(-\omega^2)$  term has been removed from  $N_e(-\omega^2)$ ,  $N_o(-\omega^2)$ ,  $D_e(-\omega^2)$  and  $D_o(-\omega^2)$  terms in (4) for compactness purpose.

$$G_p(j\omega) = \frac{N_e + j\omega N_o}{D_e + j\omega D_o} \quad (4)$$

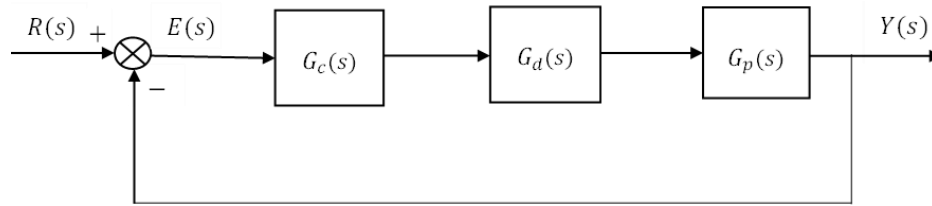


Figure 1. Block diagram of unity feedback time-delay control system

The formulation of the stability boundaries in  $k_p$ ,  $k_i$  and  $k_d$  space is a three-dimensional problem. To simplify the controller design and analysis, it can be reduced to two-dimensions by fixing one of the gains and then finding the stability region in the plane of the remaining two gains. The overall stability region can then be determined using the stability regions in the plane of the two parameters by sweeping over the fixed parameter values. In the proposed method,  $k_p$  was fixed and the stability boundary in  $k_i$ - $k_d$  plane was determined. The equations and conditions required for determining the stability region in the  $k_i$ - $k_d$  plane for a fixed  $k_p$  are presented as follows [17], [18], [23], [24]:

For  $\omega = 0$

$$k_i = 0 \quad (5)$$

For  $\omega > 0$

$$k_p = \frac{(\omega^2 N_o D_o + N_e D_e) \cos(\omega T) + \omega (N_o D_e - N_e D_o) \sin(\omega T)}{-(N_e^2 + \omega^2 N_o^2)} \quad (6)$$

$$k_d = \frac{\omega^2 (N_o D_e - N_e D_o) \cos(\omega T) - \omega (N_e D_e + \omega^2 N_o D_o) \sin(\omega T) + k_i (N_e^2 + \omega^2 N_o^2)}{\omega^2 (N_e^2 + \omega^2 N_o^2)} \quad (7)$$

The frequencies  $\omega = \omega_m$ , ( $m = 1, 2, \dots$ ) are the frequencies at which the line of a given value of  $k_p$  intercepts the graph of  $k_p$  versus  $\omega$  using (6). The stability boundary in the  $k_i$ - $k_d$  plane is formed by the line obtained from (5) and the lines generated using (7) when  $\omega_m$  is substituted for  $\omega$ . It should be noted that  $m$  is the number of points of intersection of  $k_p$  line with the graph of  $k_p$  versus  $\omega$ , that is, the number of lines obtainable from (7).

## 2.2. Determination of controller gains using CCSR method

The advantages of this method over others are as follows: i) no iterative optimization process is required, ii) system's closed loop stability is guaranteed, iii) trial and error are eliminated, iv) no error manipulation, v) low computational load, vi) controller can be design using only the stabilizing controller parameters region, vii) it can be used for any system with closed stability region and viii) it has high precision.

Detailed discussion on the formulation and advantages of CCSR method of controller design can be found in [14]. This method is amenable to PID controller design for time-delay system in the  $k_i$ - $k_d$  plane for fixed  $k_p$  because, the stability region in this plane is a convex polygon (triangle in this study).

To use this method, the coordinates of corner points of the stability boundary were determined. Assuming the number of corner points on the stability boundary is  $n$ , then the coordinates of the corner points in  $k_i$ - $k_d$  plane can be represented by  $(k_{i1}, k_{d1}), (k_{i2}, k_{d2}), \dots, (k_{in}, k_{dn})$ . The coordinate of the CCSR ( $k_{pc}, k_{ic}$ ), for fixed  $k_p$ , which is the required controller gains in  $k_i$ - $k_d$  plane can be calculated using (8) and (9) respectively [14].

$$k_{pc} = \frac{\sum_{j=1}^n k_{pj}}{n} \quad (8)$$

$$k_{ic} = \frac{\sum_{j=1}^n k_{ij}}{n} \quad (9)$$

## 2.3. System performance

There are two major states embedded in the time domain performance of feedback control systems, namely: i) transient-state, which describes the speed of the system closed-loop response to the step input and

ii) steady-state, which gives the accuracy of the system response under decayed transient condition. It should be noted that the system transient-state depends on swiftness and closeness by which the system responds to and tracks respectively the step input. The swiftness depends on the value of rise time ( $T_r$ ) and time-to-peak ( $T_p$ ), while closeness depends on the value of settling time ( $T_s$ ) and percentage overshoot (%OS) [25]. The lower the value of these TDPMs the better the system performance. The quality of system steady-state response depends on the value of steady-state error ( $ess$ ) and the lower it is, the better.

**3. DEMONSTRATING EXAMPLES**

To demonstrate the proposed methods, three Examples were used. The detailed steps of PID controller design, testing and characterization using the proposed method are fully explained and presented for Example 1 in section 3.1. To avoid repetition, these steps are skipped for Examples 2 and 3 as presented in sections 3.2 and 3.3 respectively.

**3.1. Example 1**

Design of PID controller for an integrating second-order time-delay system with system transfer function given by (10) [26] was considered in this example.

$$G(s) = \frac{1}{s(s+1)} e^{-s} \tag{10}$$

For this system, using (2), (4) and (10),  $N_e = 1$ ,  $N_o = 0$ ,  $D_e = -\omega^2$ , and  $D_o = 1$ .

The range of  $k_d$  and  $k_p$  for stability was first determined by plotting the trajectory of  $k_d$  against  $k_p$  for  $\omega=[0, \infty]$  and  $k_i = 0$  as shown in Figure 2 using (6) and (7). Also based on (6), the plots of  $k_p$  against  $\omega$  are shown in Figures 3 for the determination of the relevant frequencies for any fixed value of  $k_p$ .

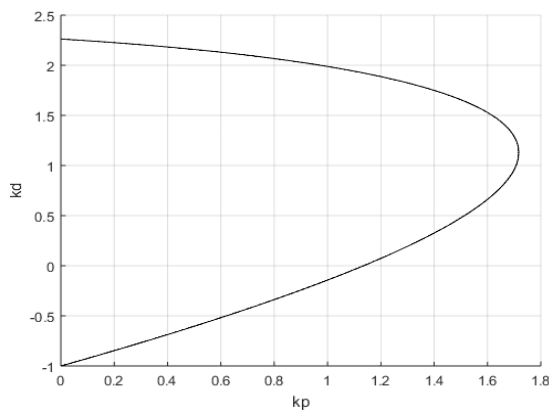


Figure 2. Plotting  $k_d$  against  $k_p$  for Example 1

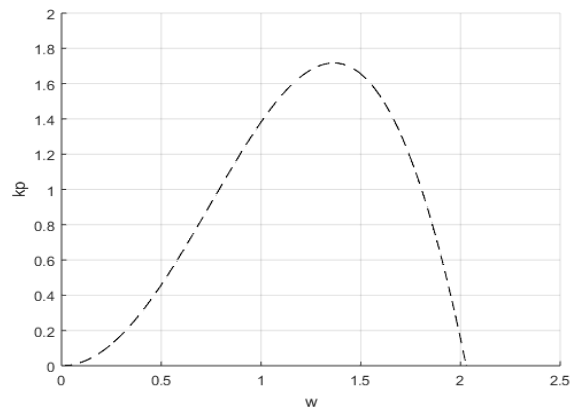


Figure 3. Plot of  $k_p$  against  $\omega$  for Example 1

It can be seen from Figures 2 and 3 that the range of  $k_p$  is 0–1.717. To find the controller gains in the  $k_i$ - $k_d$  plane the fixed gains considered based on range of  $k_p$  as shown in Figure 3 are  $k_p=0.2, 0.4, 0.6, 0.8, 1.0, 1.2, 1.4$  and  $1.6$ . The detail design for  $k_p=0.2$  is presented as follows:

As earlier explained in subsection 2.1, when  $\omega=0$ , the stability boundary equation that can be used for generating one of the boundary lines was derived using (5). To generate the equations that can be used to form the remaining boundary lines, the frequency at the point of intersection of the line of  $k_p=0.2$  (with the graph of  $k_p$  versus  $\omega$  in Figure 3) was determined. From Figure 3, the points of intersection are two and their corresponding frequencies are 0.322 and 1.991 rad/s, respectively. Substituting these frequency values into (7) yielded the two equations required for generating the remaining stability boundary lines. The resulting stability boundary equations are shown in (11)–(13).

$$k_i = 0 \tag{11}$$

$$k_{d1} = 9.6447k_i - 0.8467 \tag{12}$$

$$k_{d2} = 0.2523k_i + 2.2257 \tag{13}$$

Based on these equations and the similar equations obtained when the remaining fixed  $k_p$  values were used following the steps used for  $k_p=0.2$ , the system stability boundaries in the  $k_i-k_d$  planes shown in Figures 4 and 5 was obtained for  $k_p=0.2$  and for the complete set of fixed  $k_p$  considered respectively.

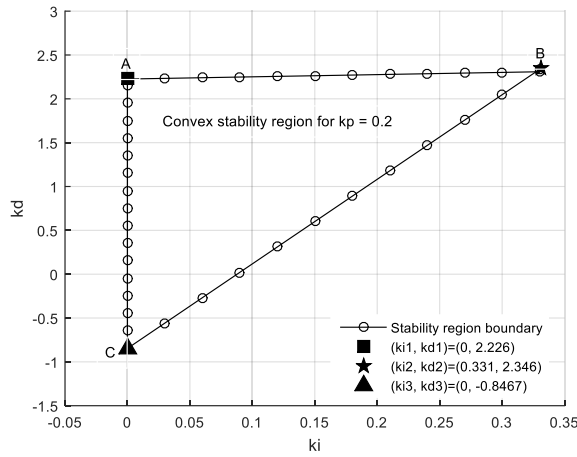


Figure 4. The stability boundary in the  $k_i-k_d$  plane for  $k_p=0.2$  for Example 1

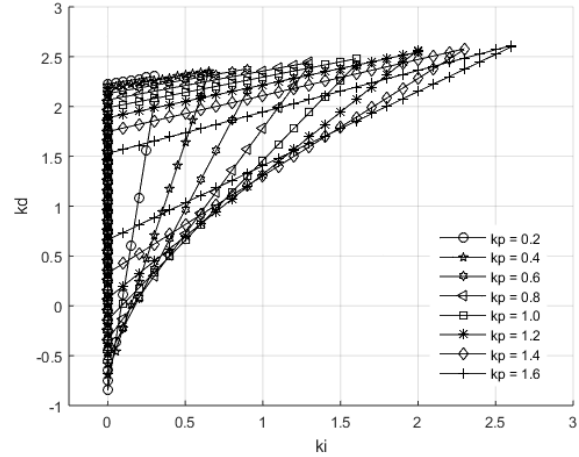


Figure 5. The stability boundary in the  $k_i-k_d$  plane for all set of fixed  $k_p$  for Example 1

In this example, the explanation given in subsection 2.2 was used for determining the controller gains as the CCSR in the  $k_i-k_d$  plane. From Figure 4, the stability boundary is a triangle, therefore there are 3 corners making  $n=3$ . The coordinates of the corner points as indicated in Figure 4 are  $(k_{i1}, k_{d1})=(0, 2.226)$ ,  $(k_{i2}, k_{d2})=(0.331, 2.346)$  and  $(k_{i3}, k_{d3})=(0, -0.8467)$ . Based on these coordinate points, using (8) and (9) the coordinate of the CCSR which is the required gains was determined to be  $(k_{ic}, k_{dc})=(0.1103, 1.2418)$ . The location of these controller gain values is indicated hexagram marker in Figure 6.

The obtained  $k_{ic}$  and  $k_{dc}$  and the corresponding fixed  $k_p$  were used in conjunction with the plant and time-delay transfer functions to plot the system closed loop unit step response. The required TDPMs for the characterization of the designed system were obtained from the step response graph. The adopted TDPMs used in this study are rise time ( $T_r$ ), peak time ( $T_p$ ), percentage overshoot ( $\%OS$ ), percentage undershoot ( $\%US$ ), settling time ( $T_s$ ) and steady-state error ( $ess$ ).

### 3.2. Example 2

An integrating second-order time-delay system with left hand side zero with transfer function shown in (14) [19] was treated in this example.

$$G(s) = \frac{0.6(-0.3s+1)e^{-0.25s}}{s(s+1)} \tag{14}$$

For this system  $N_e = 0.6$ ,  $N_o = -0.18$ ,  $D_e = -w^2$ , and  $D_o = 1$ .

The PID controller design in the  $k_i-k_d$  plane was considered for the following fixed  $k_p$  values:1, 2, 3, 4, 5, and 6. The stability boundary for these range of fixed  $k_p$  is shown in Figure 7. The obtained  $k_{ic}$  and  $k_{dc}$  in the stability region associated with each of the fixed  $k_p$  were also used accordingly as explained for Example 1 in section 3.1. The closed loop unit step response graph was plotted and the necessary TDPMs obtained.

### 3.3. Example 3

In this example a second-order time-delay system with left hand side zero whose transfer function is shown in (15) [23] was considered in this example.

$$G(s) = \frac{(-0.5s+1)e^{-0.65s}}{(s+1)(2s+1)} \tag{15}$$

For this system  $N_e = 1$ ,  $N_o = -0.5$ ,  $D_e = 1 - 2w^2$ , and  $D_o = 3$ .

In this example, the PID controller design in the  $k_i-k_d$  plane was considered for the following fixed  $k_p$  values:  $k_p = -0.5, 0, 0.5, 1.0, 1.5, 2.0, 2.5, 3.0,$  and  $3.5$ . By applying the method used for Example 1 the stability boundary for the considered range of fixed  $k_p$  shown in Figure 8 was obtained. The obtained  $k_{ic}$  and  $k_{dc}$  in the stability region associated with each of the fixed  $k_p$  were appropriately used as earlier explained. The closed loop unit step response graph was plotted and the needed TDPMs obtained.

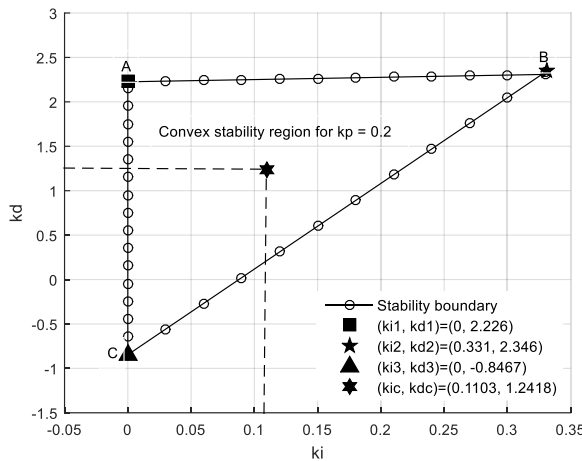


Figure 6. The CCSR in the  $k_i-k_d$  plane for  $k_p=0.2$  for Example 1

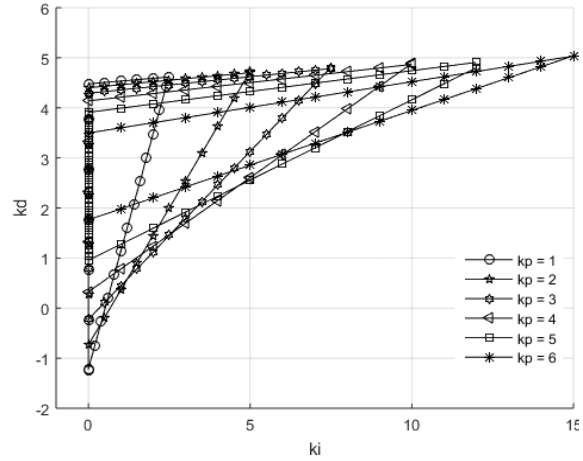


Figure 7. The stability boundary in the  $k_i-k_d$  plane for the set of fixed  $k_p$  for Example 2

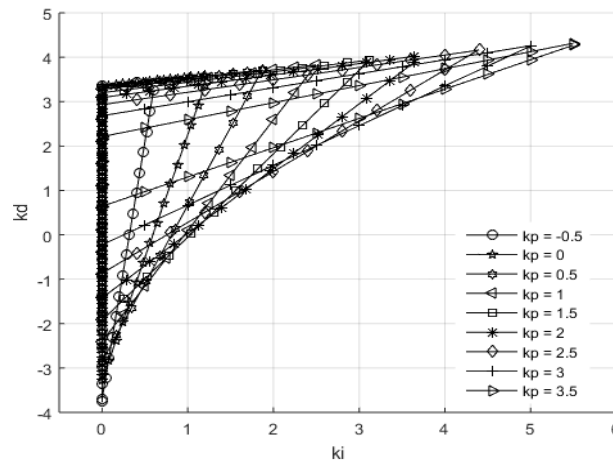


Figure 8. The stability boundary in the  $k_i-k_d$  plane for the set of fixed  $k_p$  for Example 3

**4. RESULTS AND DISCUSSION**

The fixed  $k_p$  values and the corresponding  $k_{ic}$  and  $k_{dc}$  gains in the  $k_i-k_d$  plane for Examples 1, 2, and 3 are presented in Tables 1(a), 1(b), and 1(c) respectively, where it can be seen that  $k_{ic}$  and  $k_{dc}$  increase with the value of  $k_p$  in all the three (3) examples considered. These changes in the controller gains are a form of controller tuning, because for every change a new combination of controller gains is generated in the stability region. For better understanding of the effects of changes in controller gains on the system response, closed-loop unit step response graphs for the controlled and uncontrolled system (UCS) were plotted using the same axes for each of the three illustrated examples.

The system closed-loop unit step responses in Examples 1, 2, and 3 are shown in Figures 9, 10, and 11 respectively. As shown in Figures 9 and 10 (Examples 1 and 2), the response of the UCS is better than the response of some of the controlled systems. Therefore, the required TDPMs value for both the controlled and UCSs were determined for performance analysis. On the other hand, in Figure 11, the response of the UCS can never attain the reference input, hence its TDPMs value cannot be used for performance analysis. The TDPMs for each controller

gains combination using the fixed gains and UCS (where applicable) as indicator are presented in the bar charts shown in Figures 12(a) and 12(b), 13(a) and 13(b), and 14(a) and 14(b) for Examples 1, 2, and 3 respectively.

Table 1. Controller gains in  $k_i$ - $k_d$  plane convex stability regions for (a) Example 1, (b) Example 2, and (c) Example 3

(a)							
$k_p$	0.2	0.4	0.6	0.8	1.0	1.2	1.4
$k_{ic}$	0.110	0.219	0.330	0.440	0.555	0.667	0.775
$k_{dc}$	1.229	1.284	1.345	1.396	1.457	1.509	1.558

(b)						
$k_p$	1	2	3	4	5	6
$k_{ic}$	0.833	1.667	2.520	3.333	4.167	5
$k_{dc}$	2.640	2.799	2.972	3.117	3.276	3.432

(c)									
$k_p$	-0.5	0	0.5	1.0	1.5	2.0	2.5	3.0	3.5
$k_{ic}$	0.208	0.416	0.625	0.833	1.046	1.258	1.473	1.689	1.918
$k_{dc}$	1.070	1.233	1.403	1.571	1.746	1.916	2.087	2.256	2.432

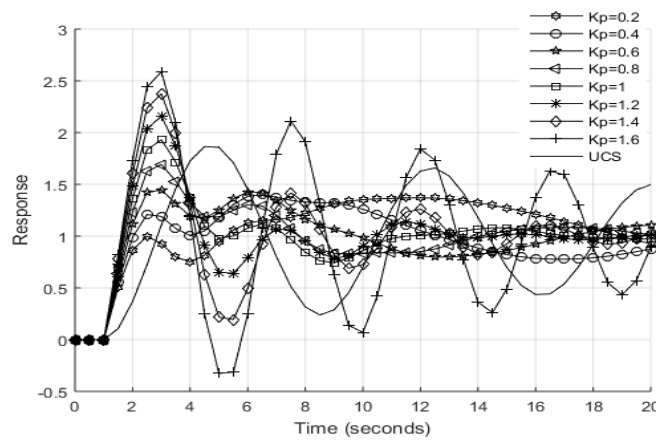


Figure 9. Unit step response graph for Example 1

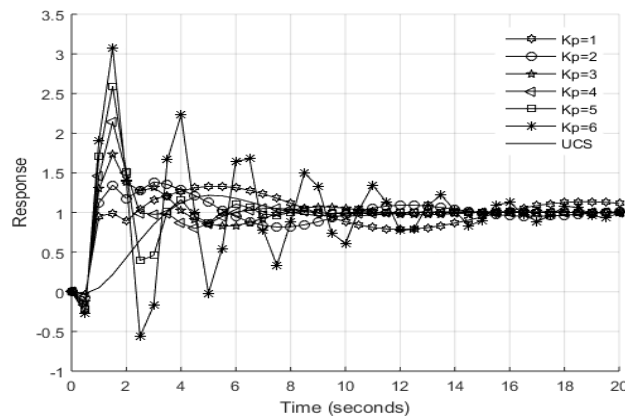


Figure 10. Unit step response graph for Example 2

It can be observed from Figure 12(a), that the minimum and maximum values of %OS corresponds to fixed  $k_p$  of 0.2 and 1.6 respectively and the minimum and maximum values of  $T_s$  correspond to fixed  $k_p$  of 1.2 and 0.2 respectively. Also, from Figure 12(b) the minimum value of  $T_r$  corresponds to fixed  $k_p$  of 1.6 while the maximum corresponds to fixed  $k_p$  of 0.2 and 0.4 but the minimum and maximum value of  $T_p$  correspond to fixed  $k_p$  of 0.6 and 0.2 respectively. From Figure 12(a) the only scenario with %US was when  $k_p=1.6$ . In Figure 12(b) the system of Example 1 yielded good steady-state response for the designed controllers as  $ess=0$

except for when fixed  $k_p=0.2$  and for the UCS that gives  $ess$  of 0.016 and 0.004 respectively which can be tolerated in practice.

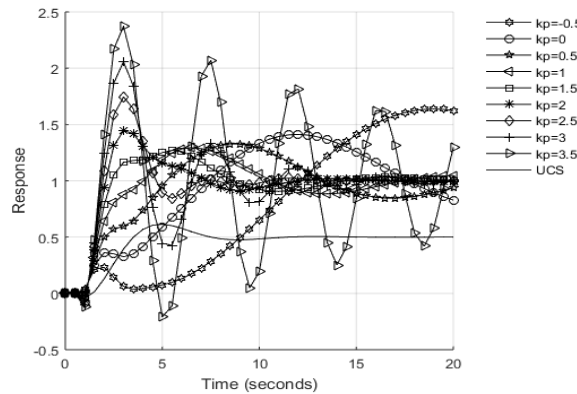


Figure 11. Unit step response graph for Example 3

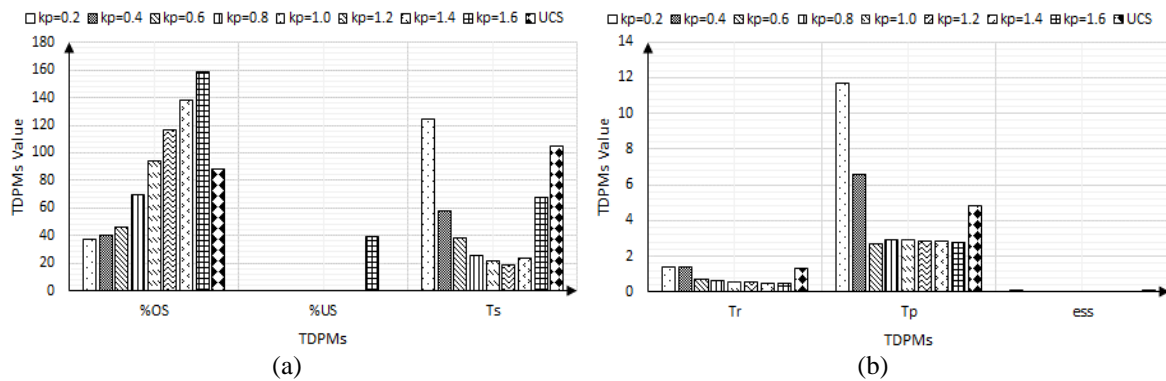


Figure 12. Bar chart of TDPMs for fixed  $k_p$  for Example 1, in (a) TDPMs are  $\%OS$ ,  $\%US$  and  $T_s$  and in (b) TDPMs are  $T_r$ ,  $T_p$  and  $ess$

From Figure 13(a) the minimum and maximum values of  $\%OS$  were attained when the system was uncontrolled and at fixed  $k_p$  of 6 respectively while the minimum and maximum values of  $T_s$  correspond to fixed  $k_p$  of 5 and 1 respectively. From Figure 13(b), the minimum value of  $T_r$  corresponds to fixed  $k_p$  of 6 and the maximum was attained for UCS. But the minimum and maximum values of  $T_p$  correspond to fixed  $k_p$  of 3 and 1 respectively. Also revealed in Figure 13(a) is the system  $\%US$  which has its minimum and maximum values corresponding to UCS and fixed  $k_p$  of 6 respectively. It can be observed from Figure 13(b) that the steady-state response for the system of Example 2 is equally good because  $ess=0$  for the designed systems except for when  $k_p=1$  that produced  $ess$  of 0.004 which will have negligible practical implications.

From Figure 14(a), the minimum and maximum values of  $\%OS$  correspond to fixed  $k_p$  of 1.5 and 3.5 respectively and the minimum and maximum values of  $T_s$  correspond to fixed  $k_p$  of 2.5 and -0.5 respectively. Also, from Figure 14(b) the minimum value of  $T_r$  corresponds to fixed  $k_p$  of 3.5 while the maximum value was at fixed  $k_p$  of -0.5 and 0. But the minimum and maximum values of  $T_p$  corresponds to fixed  $k_p$  of 3.5 and -0.5 respectively. In Figure 14(a), the minimum and maximum values of  $\%US$  was obtained when the fixed  $k_p$  was -0.5 and 3.5 respectively. From Figure 14(b), the steady-state response of the system of Example 3 is better because the designed systems give  $ess$  of 0 except for the system with fixed  $k_p$  of -0.5 that gives  $ess$  of 0.01 which can still be accommodated from practical point of view.

A situation where a system has the lowest value for both the  $\%OS$  and  $T_s$  was not encountered in the results. Also, simultaneous low values of  $T_r$  and  $T_p$  were not realized in any of designed systems. From these observations and explanation on the system performance in subsection 2.3, it can be inferred that, none of the systems can be said to have absolute good transient response since non is having absolute swift response to step input and absolute close tracking of the step input by the response.



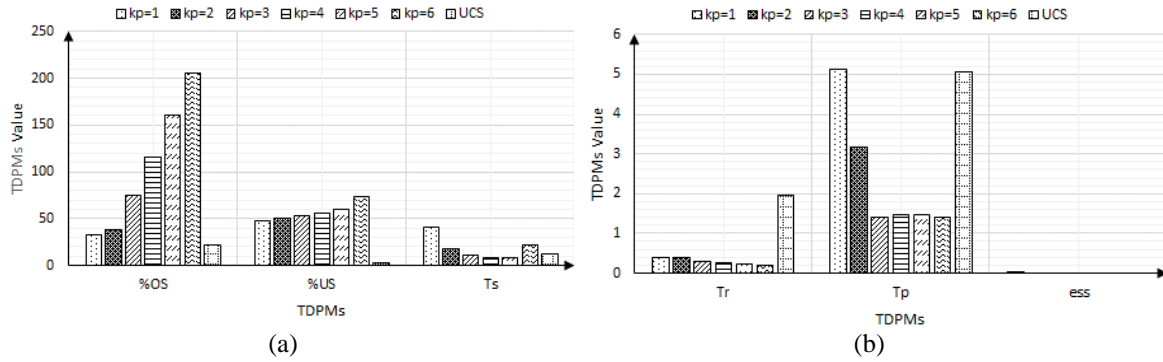


Figure 13. Bar chart of TDPMs for fixed  $k_p$  for Example 2, in (a) TDPMs are %OS, %US and  $T_s$  and in (b) TDPMs are  $T_r$ ,  $T_p$  and  $ess$

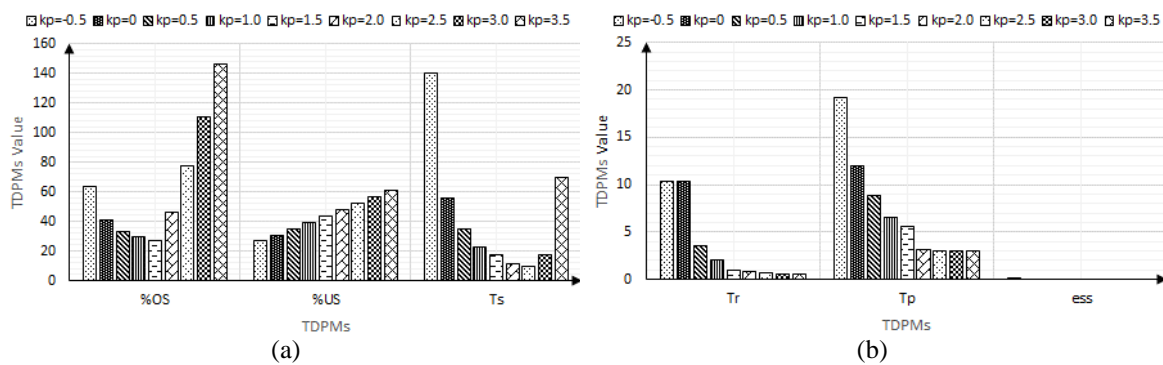


Figure 14. Bar chart of TDPMs for fixed  $k_p$  for Example 3, in (a) TDPMs are %OS, %US and  $T_s$  and in (b) TDPMs are  $T_r$ ,  $T_p$  and  $ess$

In control engineering practice, different applications normally require different system performance specifications in the form of TDPMs. Therefore, the selection of PID controller gains combination will depend on the required system performance specifications. The selection can only be made among these designed controllers because the controllers fall under the region where the systems stability is guaranteed. Most of the times, conflicts do exist among the TDPMs, therefore, to select any of the controller gains combinations, compromise must be made among any of the conflicting or competing TDPMs. It should be noted that, the number of controller gains combinations which determines the number of possible controller selection can be increased by increasing the number of fixed  $k_p$  considered in the system stability region.

**5. CONCLUSION**

PID controller design procedure for time-delay systems using the CCSR method in the  $k_i$ - $k_d$  plane for fixed value of  $k_p$  was presented and more so, the system stability region in the said plane was established. In all the cases considered, the values of the determined controller gains ( $k_{ic}$  and  $k_{dc}$ ) increase with that of fixed  $k_p$ . The performance analysis was based on system transient and steady-state which make it simple to understand. Based on the obtained TDPMs and system performance specifications, a unique combination of controller gains can be selected for the system to improve its performance. Again, selection of any of the controller gains combinations, normally requires a compromise among any of the conflicting TDPMs. The number of gains combinations determines the number of possible controller selections, and the former can be increased by increasing the number of fixed  $k_p$  in the system stability region.




**REFERENCES**

[1] S. Testouri, K. Saadaoui, and M. J. Benrejeb, "Robust stabilization of a class of uncertain systems with time delay," *IFAC Proceedings*, vol. 43, no. 8, 2010, pp. 553-557, doi: 10.3182/20100712-3-FR-2020.00090.  
 [2] L. Barhoumi, I. Saidi, and D. Soudani, "Graphical method for obtaining PID parameters for systems with time delay," *International Journal of Computer Science and Network Security*, vol. 19, no. 7, p. 31-37, 2019.




- [3] A. Yüce, N. Tan, and D. P. Atherton, "Fractional order pi controller design for time delay systems," *IFAC-PapersOnLine*, vol. 49, no. 10, pp. 94-99, 2016, doi: 10.1016/j.ifacol.2016.07.487.
- [4] J. P. Richard, "Time-delay systems: an overview of some recent advances and open problems," *Automatica*, vol. 39, no. 10, pp. 1667-1694, 2003, doi: 10.1016/S0005-1098(03)00167-5.
- [5] L. M. Eriksson and M. Johansson, "PID Controller Tuning Rules for Varying Time-Delay Systems," *2007 American Control Conference*, 2007, pp. 619-625, doi: 10.1109/ACC.2007.4282655.
- [6] A. Gupta, S. Goindi, G. Singh, H. Saini and R. Kumar, "Optimal design of PID controllers for time delay systems using genetic algorithm and simulated annealing," *2017 International Conference on Innovative Mechanisms for Industry Applications (ICIMIA)*, 2017, pp. 66-69, doi: 10.1109/ICIMIA.2017.7975554.
- [7] N. J. Hohenbichler, "All stabilizing PID controllers for time delay systems," in *PID Controller Design Approaches - Theory, Tuning and Application to Frontier Areas*, vol. 45, no. 11, 2009, pp. 2678-2684, doi: 10.1016/j.automat.2009.07.026.
- [8] D. F. A. Putra and A. S. Muharom, "The stability of cannon position on tank prototype using PID controller," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 23, no. 3, pp. 1565-1575, 2021, doi: 10.11591/ijeecs.v23.i3.pp1565-1575.
- [9] M. A. Alawan and O. J. Al-Furaiji, "Numerous speeds loads controller for DC shunt motor based on PID controller with online parameters tuning supported by genetic algorithm," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 21, no. 1, pp. 64-73, 2021, doi: 10.11591/ijeecs.v21.i1.pp64-73.
- [10] K. Åström and T. Hägglung, "Introduction," *Advanced PID Control*, ed: International Society of Automation, Chicago, USA, 2006, pp. 64-93, online: <https://www.isa.org/products/advanced-pid-control>
- [11] L. Ou, W. Zhang, and D. J. Gu, "Sets of stabilising PID controllers for second-order integrating processes with time delay," *IEE Proceedings - Control Theory and Applications*, vol. 153, no. 5, pp. 607-614, 2006, doi: 10.1049/ip-cta:20050463.
- [12] H. Efheij and A. Albagul, "Comparison of PID and Artificial Neural Network Controller in on line of Real Time Industrial Temperature Process Control System," *2021 IEEE 1st International Maghreb Meeting of the Conference on Sciences and Techniques of Automatic Control and Computer Engineering MI-STA*, 2021, pp. 110-115, doi: 10.1109/MI-STA52233.2021.9464484.
- [13] N. B. Hassen, K. Saadaoui, and M. J. Benrejeb, "Stabilizing lead lag controllers for time delay systems," *Conference: Systems, Control, Signal Processing and Informatics Int. Conf., SCSPI'15 at Barcelone, Spain*, vol. 1, no. 2, pp. 106-109, 2015, [https://www.researchgate.net/publication/299469555\\_Stabilizing\\_lead-lag\\_controllers\\_for\\_time\\_delay\\_systems](https://www.researchgate.net/publication/299469555_Stabilizing_lead-lag_controllers_for_time_delay_systems).
- [14] C. Onat, "A new design method for PI-PD control of unstable processes with dead time," *ISA Transactions*, vol. 84, pp. 69-81, 2019, doi: 10.1016/j.isatra.2018.08.029.
- [15] S. Srivastava and V. S. Pandit, "A PI/PID controller for time delay systems with desired closed loop time response and guaranteed gain and phase margins," *Journal of Process Control*, vol. 37, pp. 70-77, 2016, doi: 10.1016/j.jprocont.2015.11.001.
- [16] S. E. Hamamci, "An Algorithm for Stabilization of Fractional-Order Time Delay Systems Using Fractional-Order PID Controllers," in *IEEE Transactions on Automatic Control*, vol. 52, no. 10, pp. 1964-1969, Oct. 2007, doi: 10.1109/TAC.2007.906243.
- [17] K. Saadaoui, S. Elmadssia, and M. J. Benrejeb, "Stabilizing PID controllers for a class of time delay systems," in *PID Controller Design Approaches - Theory, Tuning and Application to Frontier Areas*, 2012, pp. 141-158, doi: 10.5772/32293.
- [18] K. Saadaoui, A. Moussa, and M. Benrejeb, "PID controller design for time delay systems using genetic algorithms," *The Mediterranean Journal of Measurement and Control*, vol. 5, no. 1, pp. 31-36, 2009.
- [19] M. M. Ozyetkin, C. Onat, and N. Tan, "PID tuning method for integrating processes having time delay and inverse response," *IFAC-PapersOnLine*, vol. 51, no. 4, pp. 274-279, 2018, doi: 10.1016/j.ifacol.2018.06.077.
- [20] M. M. Ozyetkin, C. Onat, and N. Tan, "PI-PD controller design for time delay systems via the weighted geometrical center method," *Asian Journal of Control (AJC)*, vol. 22, no. 5, pp. 1811-1826, 2020, doi: 10.1002/asjc.2088.
- [21] S. Sujoldzic, "Stabilization of an arbitrary order transfer function with time delay using PI, PD and PID controllers," M. S. Thesis, Dept. of Electrical and Computer Engineering, Wichita State University, Kansas, United States, 2005, <http://hdl.handle.net/10057/758>.
- [22] M. M. Ozyetkin, "An approximation method and PID controller tuning for systems having integer order and non-integer order delay," *Alexandria Engineering Journal*, vol. 61, no. 12, pp. 11365-11375, 2022, doi: 10.1016/j.aej.2022.05.015.
- [23] N. Tan, "Computation of stabilizing PI and PID controllers for processes with time delay," *ISA Transactions*, vol. 44, no. 2, pp. 213-223, 2005, doi: 10.1016/s0019-0578(07)90000-2.
- [24] S. Sujoldzic and J. M. Watkins, "Stabilization of an arbitrary order transfer function with time delay using a PID controller," *Proceedings of the 45th IEEE Conference on Decision and Control*, 2006, pp. 846-851, doi: 10.1109/CDC.2006.377760.
- [25] R. C. Dorf and R.H. Bishop, "The Performance of Feedback Control Systems," *Modern Control Systems*, 12th edition. ed: Prentice Hall, pp. 304-384, 2011, online: <https://dl.icdst.org/pdfs/files3/3dc1146efcce5cdf49c8d02f24d39ecd.pdf>.
- [26] S. Atiç, E. Cokmez, F. Peker, and I. Kaya, "PID controller design for controlling integrating processes with dead time using generalized stability boundary locus," *IFAC-PapersOnLine*, vol. 51, no. 4, pp. 924-929, 2018, doi: 10.1016/j.ifacol.2018.06.104.

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