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Design and analysis of RNS-based sign detector for moduli set $\{2^n, 2^n\text{-}1, 2^n\text{+}1\}$

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ABSTRACT

Magnitude comparison, sign detection and overflow detection are essential operations of residue number system (RNS) that are used in digital signal processing (DSP) applications. Moreover, sign detection attracts significant attention in RNS as it can also be used in division and magnitude comparison operations. However, these operations are not easy to perform in RNS. So, there is a need arise to propose a computationally advanced RNS based sign detector. This paper presents an area and power-efficient sign detection circuit for modulo $\{2^n\text{-}1, 2^n, 2^n\text{+}1\}$ using mixed radix conversion technique. The proposed sign detector is constructed using a carry save adder (CSA), a modified parallel prefix adder and a carry-generation circuit. Based on the synthesized results using synopsys design compiler, the introduced design offers better results in terms of the area required and power consumption. Although, the speed will remain the same when compared to the recent sign detectors for the same moduli set.

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1. INTRODUCTION

Unlike the binary number system (BNS), the residue number system (RNS) is a non-weighted and non-conventional representation. RNS has some properties that can be used in many mathematical operations that give better results when compared to BNS. In RNS, a large positive integer X is represented using a set of smaller integers known as residues $\{x_1, x_2,\ldots, x_N\}$ and a set of co-prime integers known as moduli set $\{m_1, m_2,\ldots, m_N\}$. Addition [1-3] and multiplication [4-6] are two main basic arithmetic operations in RNS. Remarkably, RNS has non-weighted representation, such that the addition and multiplication operations can be performed simultaneously and independently in each residue channel. Therefore, no carry propagation occurs from one residue channel to another. Hence it is also known as carry free number system. Due to this nature of RNS, it is used in applications that require low power dissipation and high speed, such as digital communications systems [7], digital signal processing [8-12], and cryptography [13-14]. For all such applications, RNS provides outstanding performance with high computational speed, lesser area, and low power dissipation, which are the major objective of today's real-time processors. Additionally, the reverse conversion [15-17], division [18-19], scalar [20], magnitude comparison [21-22], overflow detection [23-25] and sign detection [26-37] are also the essential operation of RNS. These operations are not easy to perform in RNS. Therefore, an improvement in such areas may lead to advanced DSP architectures using RNS. As, sign detection plays an important role in DSP applications.

In addition, a sign detection circuit is also used in division and comparison operations. So, the sign detection is an important arithmetic operation of RNS. The reverse converter can be used as a sign detector as the most significant bit (MSB) of the reverse converter represents the sign of residue number. However, this process is very complex. So, in order to avoid the complexity of the circuit, a truncated version of the reverse converter is used as a sign detector. Recently numerous efforts have been made in the area of sign detector, which presents different architectures of sign detector for different moduli sets. Some of them are designed for universal moduli set [26-29], 3-moduli set [30-34] and extended moduli set [35-37]. The 3-moduli set $\{2^n-1, 2^n, 2^n+1\}$ is very popular as this results in less complex arithmetic circuits due to the availability of the number of modulo properties. Also, the forward and reverse converter circuits require fewer components than other moduli sets.

Initially, the sign detector was implemented using the look-up-table concept that requires some memories to store the look-up-table data [26]. These types of sign detectors were suitable only for small word-length and practically, it is not realizable for larger word-length as it requires huge memories. To overcome this problem, VLSI component based sign detector is proposed in [27] without using any look-up-table. However, the sign detector presented in [27] is very complex as it was implemented using modulo multipliers. Moreover, the sign detection circuit for modulo $\{2^n-1, 2^n, 2^n+1\}$ using CRT-II was presented in [30] that was implemented using two carry generation circuits, a carry-save adder (CSA), and some basic gates. Again, a new sign detector was presented in [31], in which a comparator is used in place of the carry generation circuit to improve the performance of [30]. The recent sign detection circuit using CRT-II and scaling technique is proposed in [33], which was implemented using a carry-generator, a CSA for the accumulation of three numbers, and a adder structure for the calculation of the most significant bit. This paper presents a sign detection circuit for modulo $\{2^n-1, 2^n, 2^n+1\}$ which is based on a mixed radix conversion theorem that requires less circuit as compared to the previous one.

Section 1 itself describes the overview and applications of RNS, and also it consists of a brief overview of sign detection. The remaining paper is ordered in the following sequence: The representation of a number in RNS and some essential properties used to simplify the proposed algorithm are explained in Section 2. The introduced algorithm of sign detector and their circuit implementation are discussed in Section 3. The analysis and comparison of proposed and existing designs for the same moduli set are described in Section 4. At last, a brief summary of the proposed work is drawn in conclusion Section 5.

2. PRELIMINARIES

As per the previous discussion, a positive integer X is denoted by its residues $\{x_1, x_2,\ldots, x_N\}$ and a set of co-prime integers known as moduli set $\{m_1, m_2, \ldots, m_N\}$. The integer X should follow the condition $0 \le X < M$, where M represents the dynamic range of X, $M = \prod_{i=1}^{N} m_i$. The residues x_i is the remainder when number X is divided by m_i ($x_i = X$ modulo m_i).

The signed representation of X can be written as X_s and the sign of X_s can be determined from the (1):

$$sign(X_s) = \begin{cases} 0, & if \quad 0 \le X < \lceil M/2 \rceil \\ 1, & if \quad \lceil M/2 \rceil \le X < M \end{cases} \tag{1}$$

now, the integer X_s can be determined by given in [34].

$$X_s = \left\| \left\lfloor X + \frac{M}{2} \right\rfloor \right\|_M - \left\lfloor \frac{M}{2} \right\rfloor \tag{2}$$

Where, $\lceil . \rceil$ and $\lfloor . \rfloor$ are the smallest and greatest integer function, respectively, i.e. $\lceil 5.2 \rceil = 6$ and $\lfloor 5.2 \rfloor = 5$.

Some of the essential properties of RNS used to design efficient sign detector circuits are discussed here.

Property 1: The modulo of a negative integer X can be obtained by,

$$\left|-X\right|_m = \begin{cases} \overline{X} & if\ m = 2^n - 1 \\ \overline{X} + 1 & if\ m = 2^n \end{cases}$$

here the 1's complement of X is represented by $\overline{X}$.

Property 2: If the integer X is multiplied by any arbitrary scalar quantity in terms of power of two, it can be simplified by given property:

$$\left|2^p X\right|_{2^n-1} = CLS(X, p)$$

where $CLS(X,p)$ denotes the circular left shift of X by p bits.

Property 3: The modulo 2^n-1 addition of two integers X and Y is given by,

$$\left|X + Y\right|_{2^n-1} = \left|X + Y + C_o\right|_{2^n}$$

where, C_o=0, when $X + Y < 2^n - 1$ and C_o=1, when $X + Y \geq 2^n - 1$.

3. PROPOSED SIGN DETECTOR FOR MODULO {2^n-1, 2^n, 2^n+1}

The proposed sign detector for modulo {2^n-1, 2^n, 2^n+1} is described in this section. Let (x_1, x_2, x_3) is the residues of X and {m_1, m_2, m_3}={2^n-1, 2^n, 2^n+1} is taken as the moduli set in a RNS. The bit-wise representation of the residues x_1, x_2 and x_3 are given as:

$$x_1 = x_{1,n-1}x_{1,n-2}\ldots x_{1,0} = x_{1,\,n-1:0}$$

$$x_2 = x_{2,n-1}x_{2,n-2}\ldots x_{2,0} = x_{2,\,n-1:0}$$

$$x_3 = x_{3,n}x_{3,n-1}\ldots x_{3,0} = x_{3,\,n:0} \quad 3$$

in this paper, the MRC theorem is used to determine integer X from its residues (x_1, x_2, x_3) and moduli set {m_1, m_2, m_3}. According to the MRC theorem,

$$X = z_3 m_3 m_1 + z_2 m_3 + z_1 \quad (3)$$

where, $0 \leq z_1 < m_3$, $0 \leq z_2 < m_1$ and $0 \leq z_3 < m_2$. The MSB of (3) represents the sign bit of X which is equal to the MSB of z_3. Therefore, our aim is to determine the MSB of z_3.
To determine the value of z_1, apply modulo m_3 in (3), it gives,

$$z_1 = x_3 \quad (4)$$

to calculate the value of z_2, applying modulo m_1=2^n-1 in (3), it gives,

$$\left|X\right|_{m_1} = \left|z_2 m_3 + z_1\right|_{m_1} \quad (5)$$

substituting the value of m_1, m_3 and z_1 in (5),

$$x_1 = \left|2z_2 + x_3\right|_{m_1} \quad (6)$$

now, (6) can be rewritten as:

$$x_1 + km_1 = 2z_2 + x_3 \quad (7)$$

where, k is the scalar integer. Multiplying (7) by 2^{n-1} and rearranging the equation for z_2 and take modulo m_1,

$$z_2 = \left|2^{n-1}(x_1 - x_3)\right|_{2^n-1} \tag{8}$$

$$\left|2^{n-1}x_1\right|_{2^n-1} = x_{1,0}x_{1,n-1}...x_{1,1} = \hat{x}_1 \tag{9}$$

$$\begin{aligned}\text{Now, } \left|x_3\right|_{2^n-1} &= \left|2^n x_{3,n} + x_{3,n-1:0}\right|_{2^n-1} \\ &= x_{3,n-1}x_{3,n-2}...x_{3,1}(x_{3,0} \vee x_{3,n}) = x_3'\end{aligned}$$

$$\left|2^{n-1}x_3\right|_{2^n-1} = (x_{3,0} \vee x_{3,n})x_{3,n-1}...x_{3,1} = \hat{x}_3' \tag{10}$$

substitute the (9) and (10) into (8) and also applying properties 1 and 3, we have,

$$z_2 = \left|\hat{x}_1 - \hat{x}_3'\right|_{2^n-1} = \left|\hat{x}_1 + \overline{\hat{x}_3'}\right|_{2^n-1} = \left|\hat{x}_1 + \overline{\hat{x}_3'} + C_o\right|_{2^n} \tag{11}$$

to evaluate z_3, apply modulo $m_2=2^n$ in (3), it gives:

$$x_2 = \left|z_3(2^{2n}-1) + z_2(2^n+1) + z_1\right|_{2^n} \tag{12}$$

$$x_2 = \left|-z_3 + z_2 + x_3\right|_{2^n} \tag{13}$$

re-write the (13) for z_3,

$$z_3 = (x_3 - x_2) + z_2 - km_2 \tag{14}$$

applying modulo m_2 on both side of (14) and also substitute the value of z_2 from (11),

$$z_3 = \left|(x_3 - x_2) + \hat{x}_1 + \overline{\hat{x}_3'} + C_o\right|_{2^n} \tag{15}$$

the term $\left|X_3\right|_{2^n}$ can be written as $x_{3,n-1:0}$ and applying property 1 in (15),

$$z_3 = \left|x_{3,n-1:0} + \overline{x_2} + 1 + \hat{x}_1 + \overline{\hat{x}_3'} + C_o\right|_{2^n} \tag{16}$$

the term $\left|x_{3,n-1:0} + \overline{\hat{x}_3'}\right|_{2^n}$ of (16) can be further simplified as,

$$\left|x_{3,n-1:0} + \overline{\hat{x}_3'}\right|_{2^n} = \left|\hat{x}_3' + x_{3,0} - 1\right|_{2^n} \tag{17}$$

substituting the value from (17) in (16),

$$z_3 = \left|\hat{x}_1 + \overline{x_2} + \hat{x}_3' + x_{3,0} + C_o\right|_{2^n} \tag{18}$$

the MSB of z_3 can be determined from the simplified (18) that can be used as sign bit, i.e., sign (X)=sign (z_3). There are two cases of z_3: when MSB of z_3 is 0, i.e., $0 \le z_3 < 2^{n-1}$, in this case, the integer X is a positive number. In other cases, when MSB of z_3 is 1, i.e., $2^{n-1} \le z_3 < 2^n$, that means the integer X is a negative number.

Now, the proposed design of the sign detector can be implemented from (18) using a CSA, carry generator, and a modified parallel-prefix adder (MPPA) as shown in Figure 1. Here, the CSA is used to accumulate the three numbers, which is used to obtain the sum $S = s_{n-1:0}$ and carry $C = c_{n-1:1}0$ in (18). As in (18) modulo 2^n is taken; therefore, the carry generation in the CSA circuit is not required, so it can now be neglected. For the more significant architecture of sign detector, replace the bit c_0=0 of carry C by $x_{3,0}$ of (18). The new carry vector will be $C' = c_{n-1:1}x_{3,0}$. The carry C_o of (11) can be generated using PPA structure with some modification as depicted in Figure 2. Figure 3 shows the circuit diagram of the modified parallel-prefix adder structure for n=8. This circuit is a modification of the parallel prefix adder structure, which is intentionally designed to generate only MSB bit, i.e. MSB (z_3).

Example: For n=8, {m_1, m_2, m_3}={255, 256, 257} and the dynamic range, M=16776960. Let a signed integer X_s=-440 which is equals to the integer X=16776520 in the given RNS. The residue of X is {x_1, x_2, x_3}={70, 72, 74}. The integers x_1, x_2 and x_3 can be written as $(01000110)_2$, $(01001000)_2$ and $(001001010)_2$, respectively. To determine the values of z3 of (18), some intermediate terms are required that can be determined using (9) and (10): $\hat{x}_1 = 00100011$ and $\hat{x}'_3 = 00100101$. Also, $\overline{x_2}$ and $x_{3,0}$ can be written directly from x_2 and x_3, i.e., $\overline{x_2} = 10110111$ and $x_{3,0}$=0. The term C_o can be determine from (11), $\hat{x}_1 + \overline{\hat{x}'_3} = (72)_{10}$ which is less than 255 (2^8-1), so from property 3, C_o=0. Now, substitute all these values in (18), $z_3 = 00100011 + 10110111 + 00100101 + 0 + 0 = 11111111$. Since, the MSB of z_3 is 1, the integer X_s represented by {70, 72, 74} is negative number.

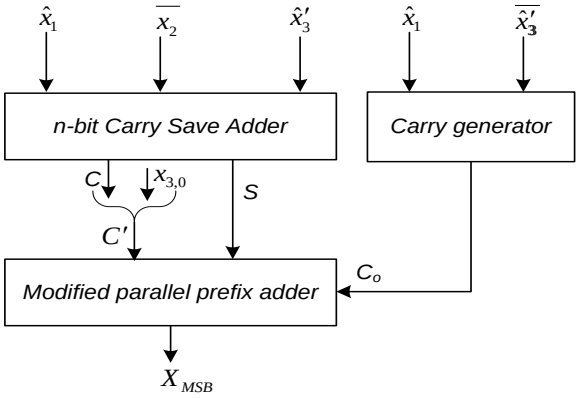

Figure 1. The proposed sign detection circuit

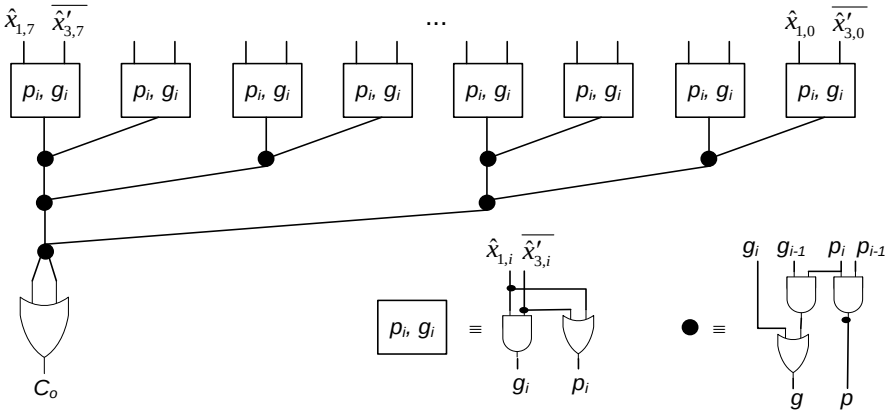

Figure 2. Carry generation circuit

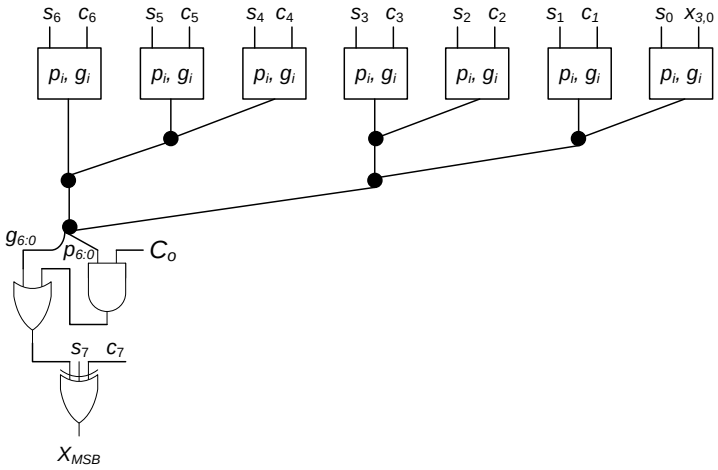

Figure 3. Modified parallel prefix structure [34]

4. SYNTHESIS RESULTS AND COMPARISON

This section describes a comparison between a proposed circuit and the existing circuits of the sign detector for the same moduli set. The comparison is based on two analyses: approximate and exact analysis. The approximate analysis is performed using the unit gate model (UGM) [4]. In this model, two-input digital logic gates (AND, OR, NAND, NOR) are assumed with the delay and area of one unit. The exclusive gates (XOR, XNOR) require the delay and area of two units, whereas the area and delay of NOT gate are counted as zero. Using UGM, the approximate delay and area of all the considered designs are compared in Figure 4 and Figure 5, respectively. These two figures itself show that the proposed circuit requires the lowest area and comparable delay as compared to the already available sign detector [30-33] for the same moduli set.

For exact result analysis and comparison, all the considered designs are verified in Xilinx ISE 8.2i using Verilog HDL. For analysis of results, all the designs are synthesized using TSMC 90nm CMOS library by keeping constant design constraints and environment condition, i.e., 25°C and 1.0V. The synthesis is done using the design compiler of Synopsys tool (version L-2016.03) for n=4, 8, 12, 16, 24 and 32, which is used to obtain the required area, delay and power. The area required for the designs is shown in Figure 6, time-delay in Figure 7 and power dissipations is shown in Figure 8. These results show that the proposed design is better when compared to other sign detector. The resulting figures itself dictate that the proposed design requires lesser area upto 7%, 52% and 3% than [30, 32-33], respectively. It is faster upto 9%, 11% and 77% than [30-32], respectively. It also consumes lesser power upto 22%, 13%, 63% and 1% than [30-33], respectively. The power-delay product (PDP) and area-delay product (ADP) of these designs are shown in Figure 9 and Figure 10, respectively. These figures show that the introduced design has the lowest PDP and ADP as compared to others.

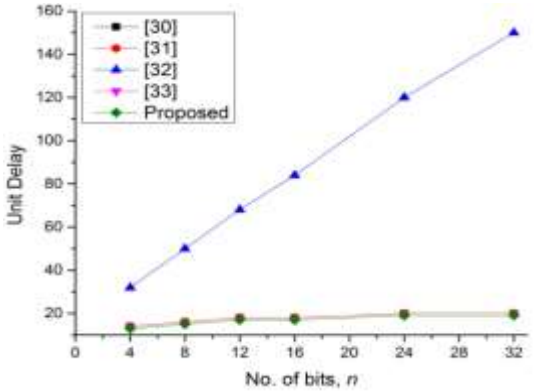

Figure 4. Delay of sign detectors based on UGM

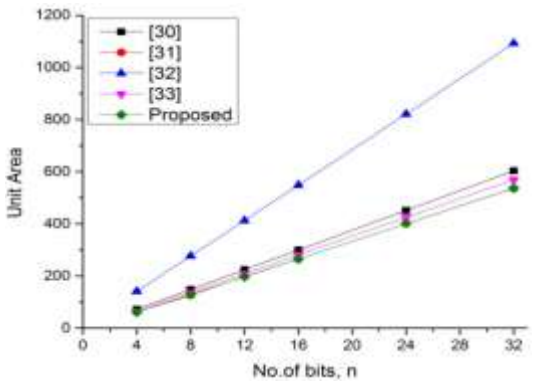

Figure 5. Area of sign detectors based on UGM

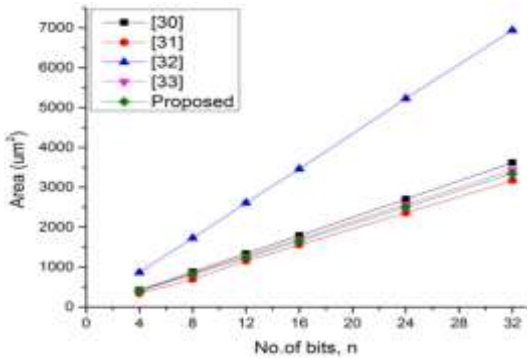

Figure 6. Synthesized area (μm2) of sign detectors

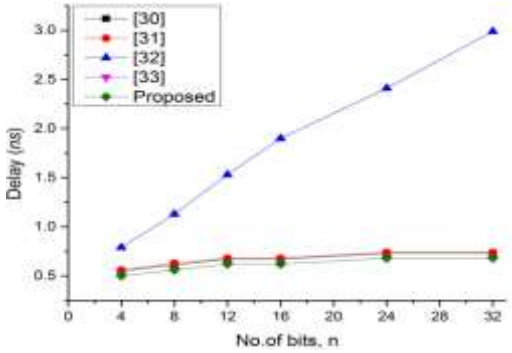

Figure 7. Synthesized delay (ns) of sign detectors

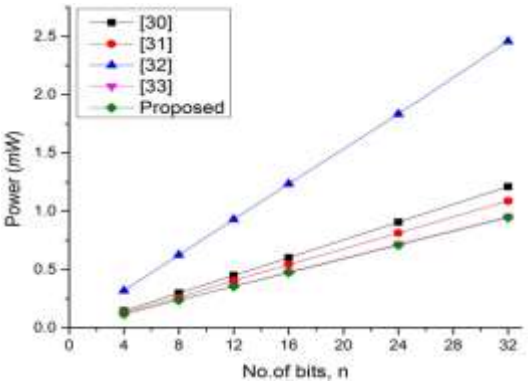

Figure 8. Total power dissipation of sign detectors

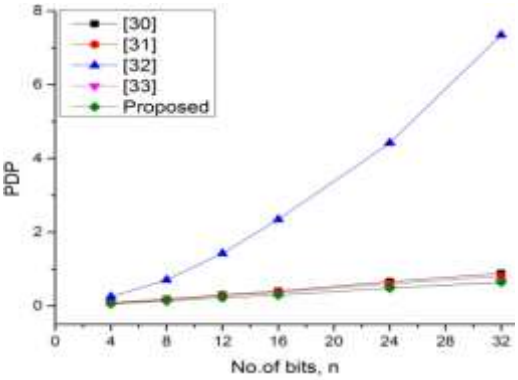

Figure 9. Power-delay product (PDP) of sign detectors

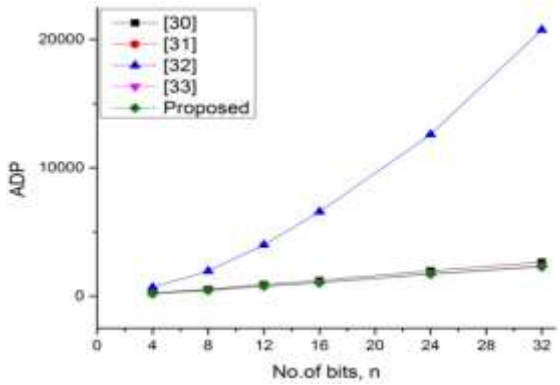

Figure 10. Area-delay product (ADP) of sign detectors

5. CONCLUSION

In this paper, a new sign detector based on the MRC theorem for RNS $\{2^n\text{-}1, 2^n, 2^n\text{+}1\}$ is described. Furthermore, the proposed design is validated using the numerical example and compared with the recent sign detectors. All the considered designs are synthesized using the Synopsys tool; the synthesized result states that the analyzed architecture requires lesser area and power dissipation than others. Also, it has the lowest ADP and PDP that are the prime objectives for real-time processing in portable devices. The analysis reveals that the proposed design saves upto 52% area, 77% delay and 63% power dissipation when compared to the other sign detection circuit for the same moduli set. So, the described sign detector using RNS can give better performance for high-speed and low power applications.

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