

Numerical Computation of Parasitic Slot Capacitances in Electrical Machines

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Abstract— Parasitic capacitive couplings in the machine slots act as an undesired leakage current path. This paper presents a method to compute lumped capacitance values and their distribution through 2D electrostatic finite-element simulation. The method is applied to a real machine slot with double layer. Turn-to-iron and inter-turn capacitive couplings show that negligible values appear between distant turns and turns not facing the slot walls and the iron. This reduction of the matrix size can be exploited on further high-frequency equivalent circuit representation. In addition, the influence of the insulation geometry and characteristics is studied.

Keywords— parasitic capacitances; finite element method; leakage currents; AC motor drives

I. INTRODUCTION

Electrical machines in automotive industry are becoming more and more popular in the latest years. The main traction system in some hybrid and all full-electric vehicles is based on electrical alternating current (AC) actuators fed by switching inverters. In addition, auxiliary utilities such as air conditioning compressors take also advantage of this technology [1].

On the power electronics side, a new generation of wide-bandgap semiconductors such as silicon-carbide or gallium-nitride are emerging due to their increased efficiency [2]. However, the switching frequencies and the voltage gradients (dv/dt) are higher, which leads to high-frequency components up to several MHz [3].

Parasitic capacitive and inductive couplings in the machine interact with these high-frequency components derived from the converter operation. Several machine failure mechanisms arise from the high-frequency phenomena such as interturn insulation breakdown and bearing currents [4]. These failure mechanisms appear typically on machines with large dimensions but with the rise on voltage gradient, also smaller machines can suffer from such failures and electromagnetic interference.

Particularly, the capacitive couplings inside the machine act as a low impedance path for stray currents towards ground or the different conducting parts. The estimation of the distribution and the value of such capacitances is essential to avoid undesired phenomena. In this way, machine designers can predict possible malfunction at early stages of the design.

Several parasitic capacitances exist between different parts of the machine (i.e. stator-to-rotor, winding-to-rotor, end-winding coupling, etc.) [5, 6]. Among all these elements, the highest capacitance values are normally associated to the coupling between winding and stator iron [7, 8]. This, defines the connection winding-frame-ground as the main current leakage path inside the machine.

Analytical and numerical methods are extensively used for slot capacitances determination [9]. The most spread tool for numerical computation on this matter is the Finite Element (FE) method, which is considered more accurate than analytical formulae at a higher computational cost.

The evaluation of slot parasitic capacitances by using FE has already been studied in the past by several authors [7], [11-13]. For machines with a small number of turns, the analysis can be detailed by computing single conductor capacitances [14]. This method is based on a matrix representation derived from multiconductor transmission line theory. Yet, this detailed computation method is not extended to a machine slot.

This work presents a simple and fast method to compute the turn-to-iron and inter-turn capacitances in a two-layer machine slot by using 2D electrostatic FE analysis. The influence of the insulation geometry and its material characteristics is also studied. Section II lays the foundations of the solver and the different capacitance extraction approaches. Section III describes the matrix representation method and Section IV presents the study about the influence of the insulation characteristics.

II. SOLVER AND CAPACITANCE EXTRACTION METHODS

A. 2D Electrostatic FE Method

Since we focus on the slot capacitance computation, a 2D model of a single machine slot is built. End-winding capacitances are not considered on this work and a 2D model is considered as the most computationally efficient approach. The governing equation for the used electrostatic solver is [15]:

$$-s \nabla V = \rho \quad (1)$$

where s is the constant permittivity of the homogeneous region, V is the electric potential and ρ is the charge density. The media permittivity is defined as $s = s_r s_0$, where s_0 is the

vacuum permittivity and s_r is the relative permittivity characteristic of the material.

B. Capacitance Extraction Methods

Two methods for lumped capacitance extraction from electrostatic FE simulation are typically used. The first one is based on the stored energy in a volume. Once this value is extracted from the FE simulation, it is possible to compute the capacitance value by using:

$$C = \frac{2 W_{ctored}}{V^2} \quad (2)$$

where W_{ctored} is the stored energy and V is the voltage difference between electrodes. The second method utilizes the surface charge on the conductors to compute the capacitance between conductors:

$$C = \frac{q}{V} \quad (3)$$

where q is the surface charge density of the conductors.

A parallel plate capacitor model is built for checking the coherence of the results by comparing FE extracted results with analytical formulation. The geometry is defined in a simple way to compare the analytical formulation with the FE results. The plates are infinitely thin with a surface of 10x10 mm and a dielectric thickness of 10 mm between them. Fig. 1 shows the modelled capacitor and the contour plot of the voltage density.

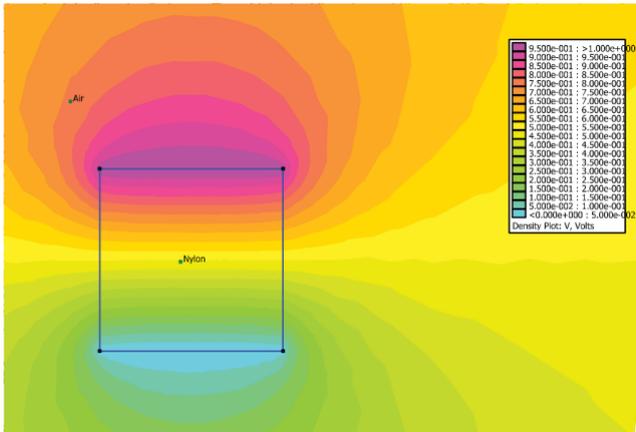


Fig. 1 - Parallel plate capacitor geometry and electric potential density contour plot

The well-known analytical expression for a parallel plate capacitor is:

$$C = s_0 s_r \frac{A}{d} \quad (4)$$

where A is the plate surface in mm^2 and d is the dielectric thickness between plates. Different materials with various relative permittivity values are simulated. Table I shows the

capacitance values for different methods and dielectric materials.

TABLE I. CAPACITANCE VALUES FOR DIFFERENT EXTRACTION METHODS

Dielectric Material	Stored Energy	Surface charge	Analytical
Air ($s_r = 1$)	0.092 pF	0.092 pF	0.089 pF
Polypropylene ($s_r = 2.2$)	0.198 pF	0.198 pF	0.195 pF
Paper ($s_r = 3$)	0.268 pF	0.268 pF	0.266 pF
Nylon ($s_r = 3.8$)	0.338 pF	0.338 pF	0.336 pF

III. SLOT CAPACITANCE MATRIX COMPUTATION

The machine stator has 12 slots with double layer and concentrated winding. The slot under study has 16 turns evenly distributed between the two layers. The nominal diameter of the conductors is 2mm and the stack length is 58mm. The geometry is drawn closely following the original shape of the slot.

The inputs for the model are the slot geometry and the dielectric constant for each material. Note that the turns will have unitary permittivity since the conductors offer a very low resistance to current compared with dielectric materials. For this reason, a material with relative permittivity equal to one (i.e. air) is used for the turns.

The mesh is configured to have at least 2 layers of triangles between turns. The interior conductor mesh is not relevant for this analysis. Fig. 2 shows the geometry of the slot without insulation together with the mesh density.

A matrix representation method for the lumped capacitance values is selected following the principles of a multiconductor transmission lines [16]. In this way, a 16x16 matrix, with elements C_{i-j} and containing all capacitive couplings between each turn and between each turn and the iron is computed. The first step is to index each turn to organize the matrix entries as shown in Fig. 3.

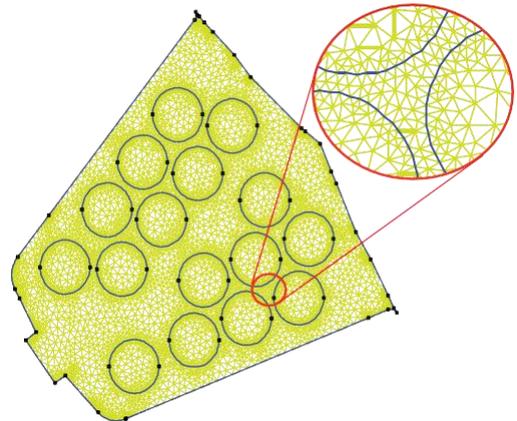


Fig. 2 - Slot geometry and mesh density

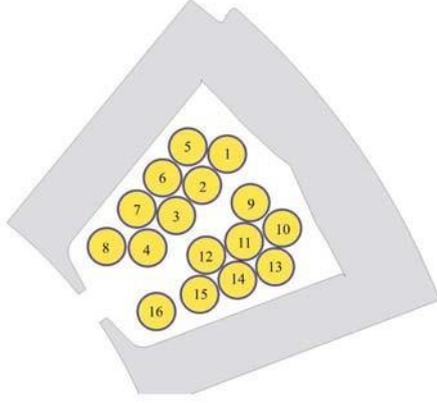


Fig. 3 - Turn indexes

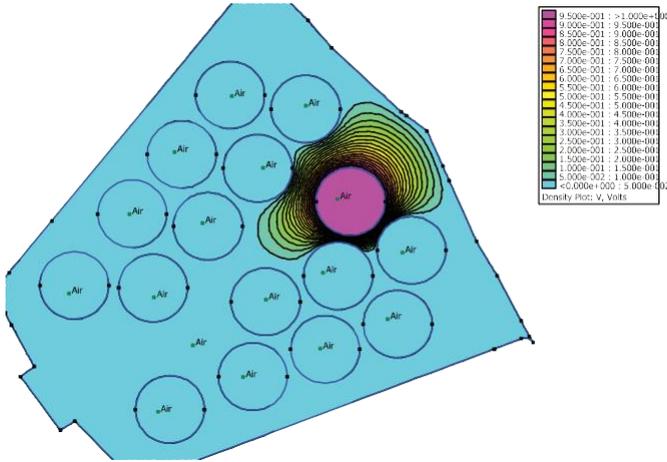


Fig. 4 - Electric potential density contour plot and equipotential lines when 9-th turn is excited

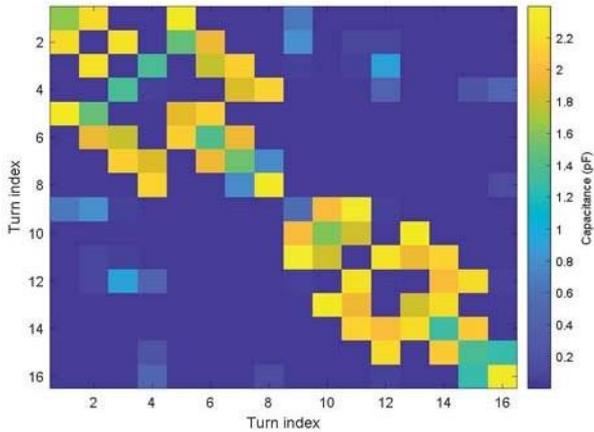


Fig. 5 - Capacitance matrix for the slot without insulation

Each entry of the matrix is computed by setting a i -th turn with a unitary voltage while the remaining j -th turns and the iron walls are set at zero voltage. In this way, one analysis per turn is carried out with each of the i -th conductors under 1V

excitation. The surface charge on the j -th turns and the iron walls represent the capacitance according to equation (3). The diagonal terms represent the turn-to-iron coupling, while the off-diagonal entries are the inter-turn capacitances.

Fig. 4 depicts the field distribution and equipotential lines inside the slot when the 9-th turn is excited. The neighboring turns and the slot walls with null potential excitation confine the electric field in the air region surrounding the excited turn.

The resultant capacitance matrix is presented in Fig. 5. The highest values are observed between neighboring turns and between the iron and the turns facing the slot walls. Very small capacitance values for distant turns and conductors not facing the iron are observed in the matrix. The computation time is approximately 20 seconds for a slot without insulation.

IV. CAPACITANCE DEPENDENCY ON THE INSULATION CHARACTERISTICS

The insulation of the machine has a direct effect on the capacitance values since the materials involved have a dielectric constant higher than one.

Three insulation elements are located inside the slot: the slot liner, the single conductor insulation and the inter-phase separator. Fig. 6 shows the disposition of the insulation inside the slot.

For the machine under study, a parametric insulation geometry is drawn to study the impact of the insulation design on the capacitance matrix. Three levels of insulation are defined to establish different amounts of dielectric material inside the slot. Table II shows the different thicknesses for the machine insulation under study and their nominal value. The insulation levels are defined according to slot geometry spatial constraints taking the nominal design values as a reference. Note that some of the dimensions of the insulators selected for this study may not be suitable to comply with thermal, mechanical or electrical requirements.

TABLE II. SLOT INSULATION THICKNESS LEVELS

Insulation Level	Insulation thickness [mm]		
	Slot-liner	Inter-phase	Turn insulation
Low	0.15	0.05	0.01
Medium	0.25	0.15	0.05
High	0.55	0.25	0.1
Nominal (design)	0.55	0.15	0.1

Polymeric materials are typically used on electrical equipment insulation. The dielectric constant or relative permittivity of each type of polymer depends on their chemical composition and on the frequency of the excitation electric field. For a static field the relative permittivity value is constant.

The relative permittivity of the polymers used for electrical insulation range approximately between 2 and 4 [17]. To simplify the analysis, all the materials are set at the same relative permittivity. The regions in the model are considered homogeneous and the mesh is configured to have at least two layers of elements on each region.

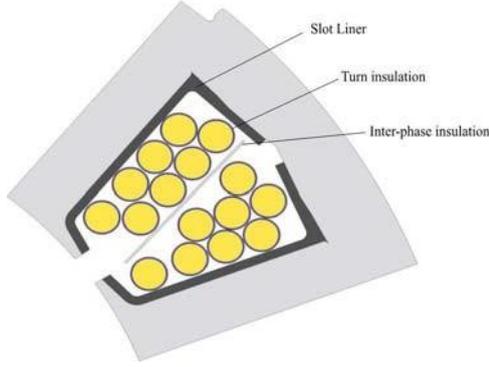


Fig. 6 - Slot insulation layout

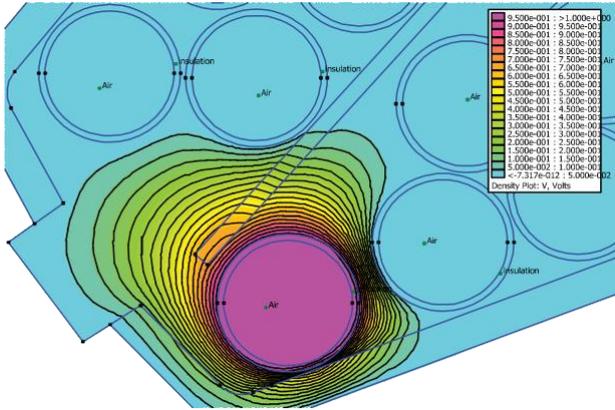


Fig. 7 - Field solution and equipotential lines for the slot with high insulation level ($\epsilon_r=3$)

Fig. 7 shows the contour plot and equipotential lines in a slot with high insulation level and relative permittivity equal to 3, when the 16-th turn is excited. The distortion of the equipotential lines in the insulation shows its influence on the solution.

Fig. 8 shows the dependence of C_{1-1} and C_{9-1} on the insulation thickness and its relative permittivity. These two elements are an example of two capacitances involving different elements of the insulation (i.e. slot walls and inter-phase insulation). The dependency on the relative permittivity is mainly observed when the insulation level is high. The thickness of the insulation affects the capacitance values independently of the relative permittivity.

Capacitance matrices for the different levels of insulation are shown in Fig. 9. For non-negligible entries of the matrix, the values increase together with the insulation thickness.

V. CONCLUSIONS

In this paper a matrix representation method for turn-to-frame and inter-turn lumped capacitance computation is presented and applied to a double layer slot. The computed matrix shows that the strongest couplings are found for capacitances between neighboring turns and between turns facing the slot walls and the iron. It is demonstrated that the

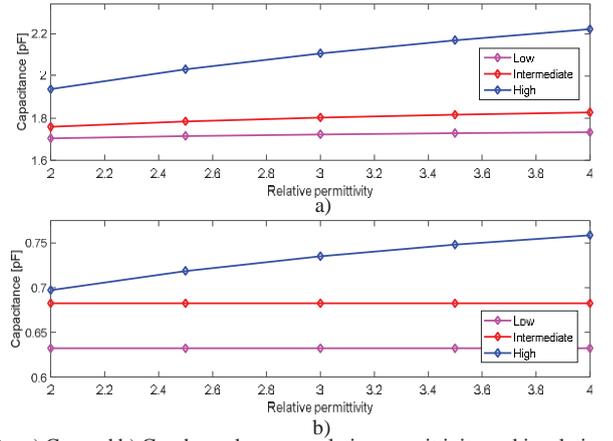


Fig. 8 – a) C_{1-1} and b) C_{9-1} dependence on relative permittivity and insulation level

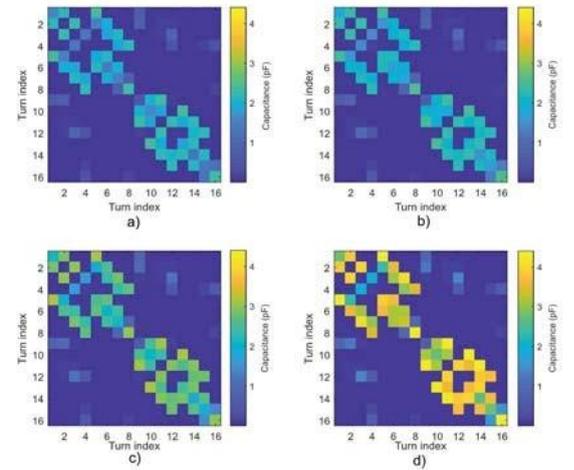


Fig. 9 - Capacitance matrices for different levels of insulation ($\epsilon_r=3$), a) no insulation, b) low level, c) intermediate level, d) high level

capacitance matrix is symmetric and that it can be simplified by neglecting some low-valued entries corresponding to distant elements. The study on the insulation geometry and characteristics shows their influence on the capacitances. The capacitive coupling is proportional to the amount of dielectric material in the slot.

Further work will be focused on the extraction of frequency dependent lumped parameters such as resistances and inductances. These parameters together with the capacitance matrix can be used to build the full impedance response over a broad frequency range of an electrical machine.

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