International Journal of Reconfigurable and Embedded Systems (IJRES)
Vol. 11, No. 1, March 2022, pp. 71~83
ISSN: 2089-4864, DOI: 10.11591/ijres.v11.i1.pp71-83

Distinct ρ-based model of silicon N-channel double gate MOSFET

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Article Info

Article history:

Received Oct 20, 2021
Revised Dec 2, 2021
Accepted Jan 27, 2022

Keywords:

Device capacitance
Double gate MOSFET
Low power
MOSFET scaling
Short channel effect

ABSTRACT

Growing endless demand for digital processing technology, to perform high speed computations with low power utilization and minimum propagation delay, the metal-oxide-semiconductor (MOS) technology is implemented in the areas of very large scale integrated (VLSI) circuit technology. But MOS technology is facing the challenges in linear scaling the transistors with different channel modelling for the present day microelectronic regime. Linear scaling of MOSFET is restricted through short-channel-effects (SCEs). Use of silicon N-channel double gate MOSFETs (DG MOSFETs) in present day microelectronic regime features the short channel effect of MOSFET through a reasonable forward transfer admittance with the characteristics of varying input capacitance values ratio. In this research paper, a distinct ρ-based model is designed to simulate SCEs through the designed silicon N-channel double gate MOSFETs with the varying front and back gate doping level and surface regions to estimate the varying junction capacitances can limit the intrusion detection systems (IDS) usage in VLSI applications. Analytical model for channel length and simulated model for total internal device capacitance through distinct ρ-based model are presented. The proposed distinct ρ-based model is suitable for silicon nanowire transistors and the effectiveness of the proposed model is validated through comparative results.

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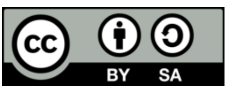

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1. INTRODUCTION

In the modern era, the silicon-based semiconductor industry is developing rapidly and playing a pivotal role in the design of integrated circuits, wireless communication systems, mobile devices and so on according to Moore's Law. The technical and scientific advancement have moved further these semiconductor industries to explore different materials and technologies to serve the purpose of power, cost, area and speed in a high integration density application.

In further approach complementary metal-oxide-semiconductor (CMOS) [1] is facing fundamental physical limits in terms of circuit, device and material, alternative silicon on insulator (SOI) devices [2], which can be scaled more aggressively than bulk CMOS. SOI and its variants partially depleted (PD) and fully depleted (FD) uses the same substrate, the same material with the same fabrication process, but it is very susceptible to floating body effects with scaling constraints as bulk device [3]–[5] causing the threshold

voltage to be sensitive to SOI thickness and device terminal interface. Advanced MOSFET structures are the best alternatives for SOI, such as multiple gate MOSFET, which can scale bulk SOI structures. A double gate MOSFET (DG MOSFET) structure fabricated on SOI wafer is made used in [6] as compared to the bulk MOSFETs.

Among the MOSFET emerging devices [7], the DG-MOSFET is important through [8], [9]. From the surveyed literature, the statements of the problem addressing in this proposed paper DG MOSFET design are: i) Limitation arising from the fixed second gate voltage is that four-terminal driven DG-MOSFETs exhibit non-ideal subthreshold slope [10]. And can be limited by, the minimum channel length imposed by short-channel effects is related to 4 times the thickness width of oxide layer; ii) Limitation arising from *d*ecrease in oxide width, with doping levels high in device substrate. With this, there is an increase in junction capacitance and current tunneling and similarly there is a slope of subthreshold current and mobility of the carriers in the device drain [11] terminal, which results in subthreshold volume inversion; iii) Limitation arising from the slope of the subthreshold which allows the device reduce leakage current in the device through driving current [12], which results in lowering the threshold voltage with the falling subthreshold slope in a channelled DG MOSFETs; and iv) Limitation arises as the top gate is conducted and causing the short-channel effect [13]–[15]. The short-channel effects (SCEs) for tri-gate MOSFET can be controlled than in FinFETs making the double-gate design causing the gain of the tri-gate MOSFET device to increase, which causes SCEs to reduce.

In this research paper, the implementation has been made with designing DG MOSFET device in different cases [16]–[18] by varying channel length and compromise between power and speed performance and linearity. The scaling is made based on the assumptions of dimensional miniaturization of the device and with the scaling constant values. The specific objectives include: i) To propose and design a new distinct ρ-based DG-MOSFET architecture model and ii) To analyze the short-channel effects with current continuity equation based on Poisson’s equation and to investigate the characteristics of the four-terminal driven DG MOSFET to the proposed distinct ρ-based DG-MOSFET architecture model. In section 2, review of previous methods are made. In section 3, the methodology and modeling of the proposed DG MOSFET is presented. in section 4, simulation results and discussion of the proposed DG MOSFET is made. Section 5 and 6 provides conclusions and future scope of the proposed work.

2. LITERATURE REVIEW

A FinFET transistor with multi-gate device, having higher performance, the challenges of FinFETs are:

a) With the decrease in the fin-width, causes the minimization of SCEs, through its fin shape, by minimizing the doping level in channel, the subthreshold variations are minimized. For too thick FinFET, the gate on the sides and top electrostatic influence will be reduced. Too few fins can also cause variability. The challenge of fin doping is the application of high dielectric grain layers in discrete size in DG MOSFET channels doping [19]–[23]. DG MOSFETs work best as regular structures placed on a grid. To increase gate drive strength grains are included in the form of discrete sized high dielectric grain layers, through distinct variations, which is not available in FinFETs. Channel length variation and body biasing are limited in value due to the intrinsic characteristics of the FinFET technology, which can be limited through the application of high dielectric grain layers in discrete size in DG MOSFET.
b) Because of the proximity of gates in FinFET, the charge sharing occurs in the corners of front and back gates, with its premature inversion for the gate-to-channel electric field. The challenge of subthreshold characteristics of the FinFET degrades, use of distinct grains at the middle of gates, where the high dielectric grain layers are positioned at a constant (ρ) and equal position locations with a discrete size during DG MOSFET channels doping from its surface to channel location.

In Double gate MOSFET the source and drain made up of silicon material and gate is made up of Al material. The use of high dielectric grain layers positioned at a constant (ρ) and equal position locations provided in the strained Si materials. The material used for grains is scalable as it provides an acceptable level of electron and hole mobility even at reduced thickness. The MOSFET’s using grain materials can be used as high-performance semiconductor devices. As the leakage current increases, the thickness of the Gate Oxide material is increased to reduce these currents. To increase gate capacitance the relative dielectric constant of the material silicon dioxide is replaced with a relatively high dielectric grain layer material. This will allow the use of thicker dielectric gate layer which can be used to reduce the leakage current through the structure.

The requirements for such distinct ρ-based model of silicon N-channel double gate MOSFET with high dielectric grain layers positioned at a constant (ρ) and equal position compact models include with subthreshold swing and on channel length modulation and the dependence on short channel effects on threshold voltage with temperature and on structures dimensions. Finally, they should be accurate and computationally efficient.

3. PROPOSED DISTINCT ρ-BASED DEVICE MODEL AND METHODOLOGY

In this section, the simulation model of proposed distinct ρ-based device is discussed with theoretical and practical model. MATLAB code has been presented to demonstrate the analytical model of proposed device design and the Distinct ρ-based device design model is adopted to implement Silicon N-channel dual-gate MOSFET. The models for short and long channel DG MOSFET are categorized into electrostatic surface charge distributions, total internal device capacitance and device drain-source characteristics models for analytical and simulation models [24], [25].

In this research work, planar DGMOSFET is considered with a distinct ρ-based device, which is an alternative technology for FinFET's. Compared with GAA and Tri-gate MOSFET's, the performance interms of I_{DS} and DIBL is improved. In this paper, a conventional, one top gate DG MOSFET and both gate DGMOSFET's are considered with gate all around (GAA), FinFETS, and tri-gate MOSFETs. For 10 nm scale, the performance of proposed DGMOSFET is showing an improved ΔV_g a varying gate voltage for different front and back gate voltages. Study and implementation of proposed DG MOSFET through planar design can be made relevant with the usage of doping concentration structures, where resistance can be reduced, inturn increasing the I_{DS} for improved swithching action.

In this research paper, a layered DG MOSFET structure through ballistic quantum simulation is introduced. This layered structure with distinct slots structure solutions is presented through Poisson continuity equation in making ballistic electrons. Using MATLAB, the proposed layered DG MOSFET with device structure and doping levels are analyzed.

3.1. Distinct ρ-based device structure

The structure of the proposed distinct ρ-based DG MOSFET used in this research work is schematically presented in Figure 1, have the design parameters as shown in Table 1. In the defined structure, symmetrical p+ and p- poly gates without drain and source device terminals.

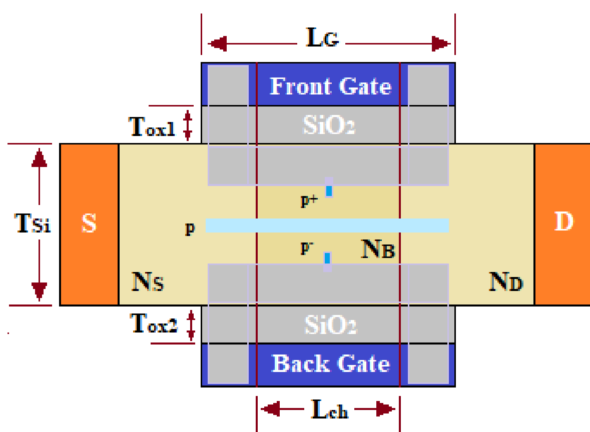

Figure 1. Illustration of proposed DG-MOSFET ρ-distinct slots structure

The background doping of the silicon film for distinct ρ-based slot structure with 1nm of top and bottom ρ slot of gate stack with SiO2 p+ strained Si layer and is considered to be intrinsic, as shown in Figure 2. Uniform p insulation strained-Si contains a middle-ρ-slot gate stack is placed between top and bottom gate stack with a thickness of 0.5 nm. The bottom SiO2 interfacial layer is also stacked with high dielectric constant material uniform p- strained-Si layer whose thickness is 1 nm.

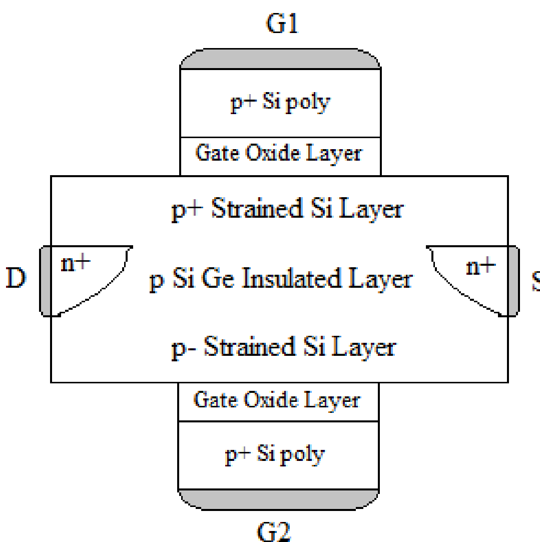

Figure 2. Illustration of proposed DG MOSFET ρ-strained Si structure

3.2. Model development

In DG MOSFET, as shown in Figure 3, with both top p+ gate stack, bottom p- gate stack of high dielectric constant [26], as the bottom gate high dielectric constant layer thickness is increased, causing source to drain potential barrier to reduce, with this bottom gate to increase the threshold level. The drain current through gate stack is improved with top and bottom gate stacks, causing the threshold voltage and drain current to stabilize the device dimensions at a constant rate with the bottom gate having high dielectric constant. With this there is a reduction in dielectric constant potential barrier of the relevant bottom gate stack, causing the electron density to reduce and causing the threshold voltage to reduce with both gate stacks. Proposed model results in a improvement in electron density and reduction of threshold voltage for DG MOSFETs with both p+ and p- gate stacks.

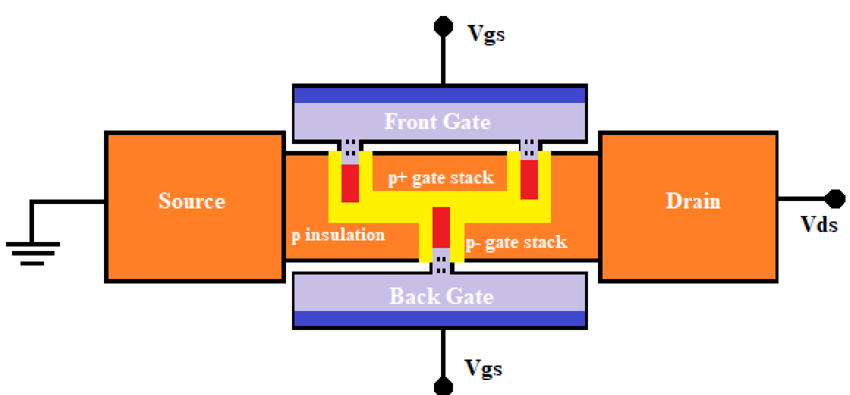

Figure 3. Illustration of proposed distinct ρ-based model of silicon N-channel double gate MOSFET

3.3. Model flowchart

The flowchart of ballistic MOSFET is presented in Figure 4 through ballistic carrier transport is considered. Through one subband conduction, the ultra-thin material film is utilized for proposed DG MOSFET device design. In Figure 5, the distinct ρ-based DG MOSFET design flow chart is shown, with crystalline grains made charged bodies through 1nm vertical cross-section area, having the charged density varying from 1 to 10 u, with u=1.28x10^{-12} C/cm. In the proposed DG MOSFET device design, subthreshold parameters and drain current characteristics were investigated in the presence of top and bottom charged distinct ρ-slots, which become asymmetric with the charge slots of dual-gate dielectric layers.

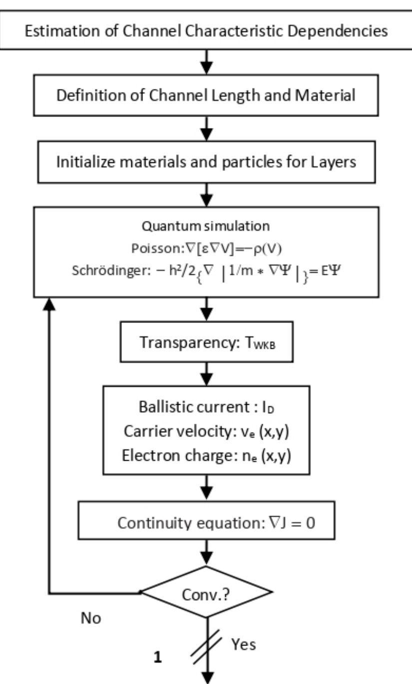

Figure 4. Flowchart of proposed DG MOSFET ballistic mechanism on Flow of ballistic DG MOSFET mechanism

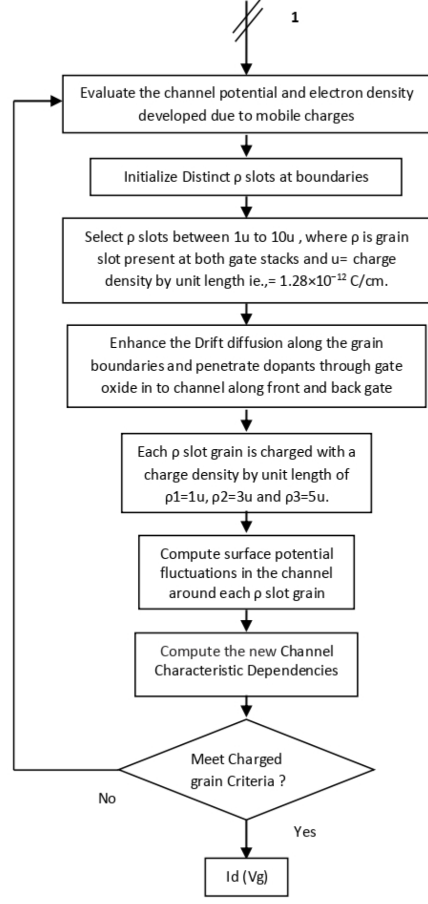

Figure 5. Flowchart of proposed DG MOSFET carrier transport mechanism on Flow of distinct ρ-based DG MOSFET mechanism

3.4. Model mathematical representation

Here, the flowchart of ballistic MOSFET which is presented in Figure 4 through ballistic carrier transport and the flowchart of proposed DG MOSFET carrier transport mechanism which is presented in Figure 5 as the flow of distinct ρ-based DG MOSFET mechanism is illustrated in mathematical presentation.

The proposed model is illustrated in two gate approach as front and back gate, which is a modified form of ballistic complete model with a realistic DG MOSFET model through the use of carriers across surface to scatter in to the gate doping regions with a layer capacitance as a dependent parameter near the field regions across distinct ρ-based front gate and back gate with proposed distinct ρ-based positions having the three grain sizes for ρ=1 u, ρ=3 u, and ρ=5 u. With the flux density concept, the total gate current across the three grains with the drain to source current is expressed as (1).

$$I_g = I_{\rho=5u}^{\rho=1u} - I_{\rho=3u} \quad (1)$$

where $I_{\rho=5u}^{\rho=1u}$ is ρ=1 u to ρ=5u current variations and $I_{\rho=3u}$ is ρ=3 u current variations. Here I_g represents a ballistic DG MOSFET model three grain sizes gate current with a depenedent channel gate channel length varying on distinct ρ-based positions only. And with the distinct ρ-based positions channel length parameter L and the distance between the surface current scattering $I_{\rho=1u}$, $I_{\rho=3u}$ and $I_{\rho=5u}$ position values denoting as δ as an average value. The carrier current scattering from front gate $I_{\rho=1u}$ *and* $I_{\rho=5u}$ towards back gate $I_{\rho=3u}$ with the channel length in the scattered regions is expressed as carrier scattering index as (2).

$$G_F^B = F_1^5 + B_3 \quad (2)$$

where G_F^B is the front to back gate scattering coefficients, F_1^5 is the front gate scatter carrier concentration from $I_{\rho=1u}$ to $I_{\rho=3u}$ and $I_{\rho=5u}$ to $I_{\rho=3u}$ and B_3 is back gate scatter carrier concentration from $I_{\rho=3u}$ to $I_{\rho=1u}$ and $I_{\rho=3u}$ to $I_{\rho=5u}$. The parameters for F_1^5 *and* B_3 are given by (3).

$$F_1^5 = \frac{\delta}{\delta+L} \text{ and } B_3 = \frac{L}{L+\delta} \quad (3)$$

where front and back gate scattering coefficients are variable with δ and L parameters. From the above F_1^5 *and* B_3 parameters, the proposed work is proved to be showing a better comparative work than the other DG MOSFET constructions, as:

a) When F_1^5 is considered for front scattering, the L value is considered to be effective and results in to current-drift in to gate channel, effeccting the I_{DS} variations and limiting the flow of current across the device.
b) When B_3 is considered for back scattering, the δ value is considered to be effective and results in to a linear ballistic gate channel region, effecting all the gate injected carrier charges to deplete at source and enters in to drain, causing the controllable carrier concentration across source and drain terminals.
c) When F_1^5 *and* B_3both are considered for front and back scattering, the mean value of δ and L are considered on the effective charge carriers mobility of electrons, effecting the small field region through $I_{\rho=1u}$ and $I_{\rho=5u}$ present across the source and large field region through $I_{\rho=3u}$ present across the drain.
d) The mean value of δ and L illustarte amount of charge carrier concentration with the present field containing $I_{\rho=1u}, I_{\rho=3u}$ *and* $I_{\rho=5u}$ distinct slots.

From the above analysis of proposed distinct slots usage and implementation, proposed work improves the drain bias through carrier scattering across front gate distinct slots and limits the source bias through gate width controlling through carrier injections from back gate. And causes the scattering across source is minimized compare to drain and with the usage of distinct slots positions, scattering is controlled at $I_{\rho=1u}, I_{\rho=3u}$ *and* $I_{\rho=5u}$, in-turn reducing the carrier charges and capacitance, which are independent to each other.

4. SIMULATION RESULTS AND DISCUSSION OF PROPOSED MODEL

During the simulation of proposed device, the analysis on effect of positions on the gate boundary is made. The characteristics of number of three grains connected boundary surfaces depends on ρ value predicted, it is made through the ballistic approach for the defined device gate material of dielectric polycrystalline structure [27], as drift diffusion is constant at boundary of device gate layers, causing the usage of grains with size of 1 nm only. Comparative device parameters considered in this work are shown in Table 1.

Table 1. Comparative device parameters considered for proposed distinct ρ-based DGMOSFET

Device parameters	Silicon MOSFET (CMOS)	GaAs MESFET	AlGaAs/GaAs MODFET	Distinct ρ-based DGMOSFET
Minimum channel length (μm)	0.1	0.2	0.18	0.2
Gate width (μm)	0.125	0.375	0.375	0.345
Doping (x 10^{18} / cm^3)	2.0	5.0	5.0	2.0
Threshold voltage (V)	0.4	0.2	0.25	0.2

Following proposed work achieved simulation results show three grain sizes for ρ=1 u, ρ=3 u, and ρ=5 u, representing two front gate grains and one back gate grain in the location of positions ρ=1 u, ρ=5 u, and position ρ=3 u respectively.

In Figures 6, 7, and 8 illustrate the total internal device capacitance variation in the 6 ρ=1 u, 7 ρ=3 u, and 8 ρ=5 u. Compare to traditional DG MOSFET designs for the comparison between performance of proposed approach and literature survey approaches, results achieved in the proposed DG MOSFET design are illustrated:

a) The location of positions is moved through the device threshold voltage by varying the device capacitance with zero variations of device gate grain polysilicon boundary in their displacement, which is a new result achieved in the proposed design, because in traditional DG MOSFET, the locations of positions are static and do not provide desirable threshold voltage.
b) The device three gate drain voltage is chosen to be maximum at ρ=3 u location and increases its surface potential across ρ=1u and ρ=5u, causing the drain voltage to increase further, which is a new result achieved in the proposed design, because in traditional DG MOSFET, the three gate drain voltages are varied in either positive or negative gate values and do not provide desirable drain voltage and the intrusion detection systems (IDS) usages.
c) Across the grain boundary, the channel gate device potential is reduced, causing the channel to provide a uniform current flow in the crystalline structure of DG MOSFET, which is a new result achieved in the proposed design, because in traditional DG MOSFET, the grain boundary is not considered for varying channel gate voltage variations and do not provide desirable current flow and channel length variations.
d) The boundary positions of these three grain charges are equalized with underlying SiO2, which is a new result achieved in the proposed design, because in traditional DG MOSFET, the front and back grain boundary charges are not equalized to provide uniform doping levels and do not provide desirable position estimations for gate to channel length distance and distinct slots to allocate with VG and VD variations.

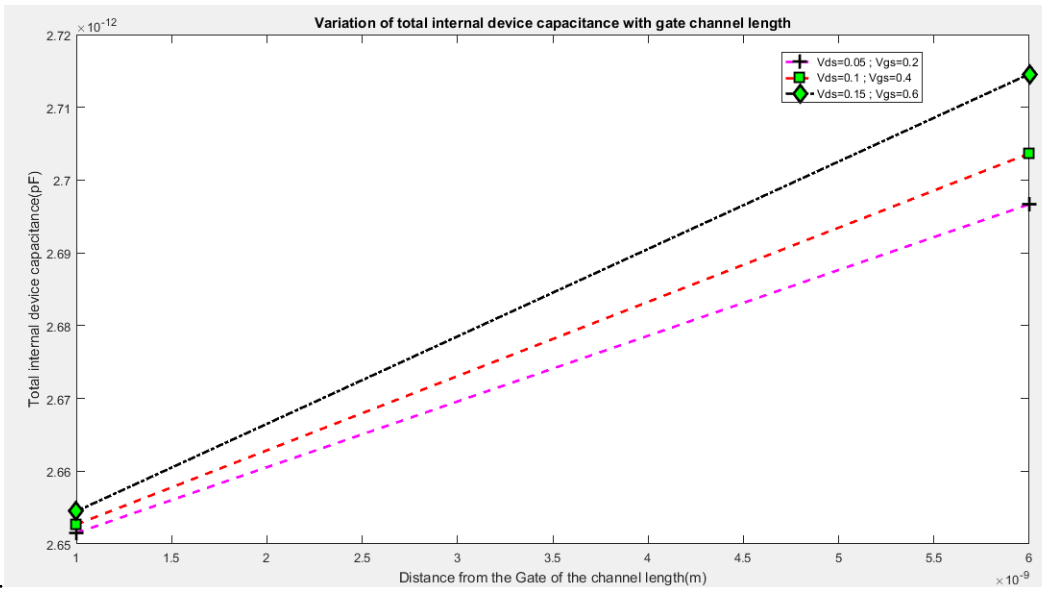

Figure 6. Channel characteristics for distinct ρ=1 u

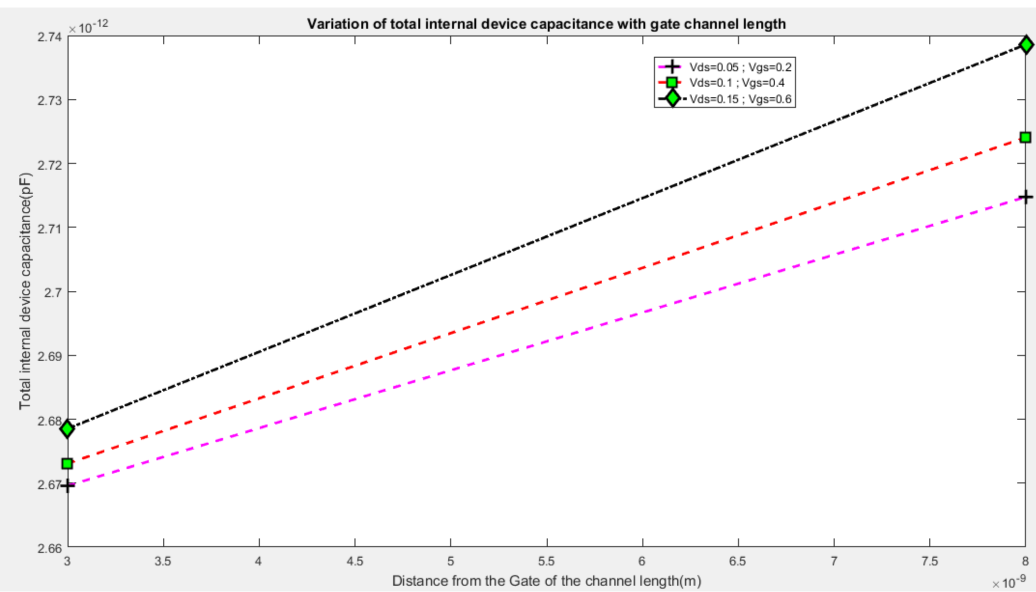

Figure 7. Channel characteristics for distinct ρ=3 u

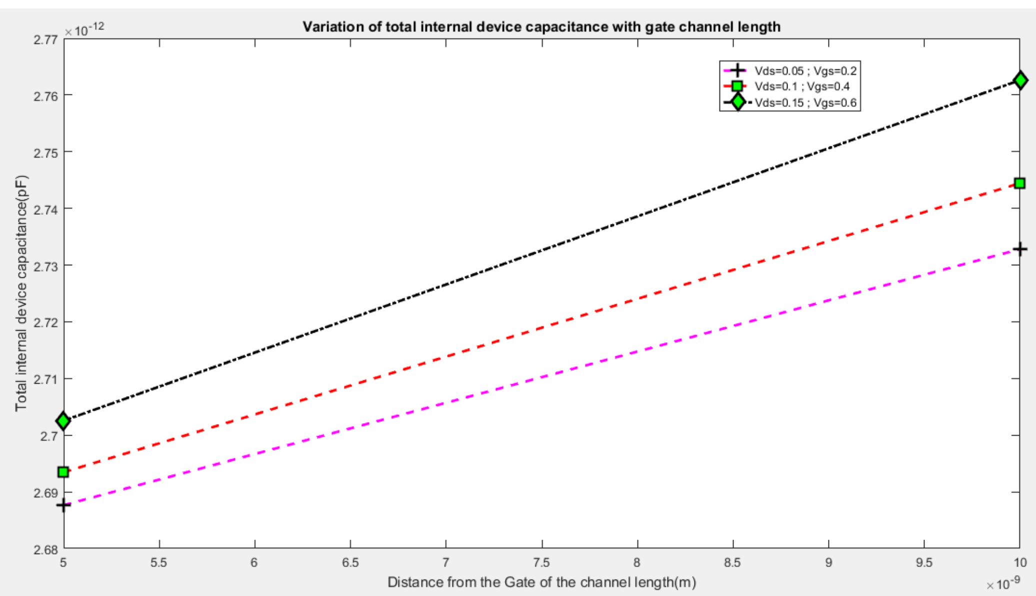

Figure 8. Channel characteristics for distinct ρ=5u

Figures 9 and 10 show the electrostatic charge distribution in the proposed distinct ρ-based MOSFET considering x=2 nm plane grain boundary, right below the semiconductor-insulator interface at VD=1 V and VG=1.5 V.

The DG MOSFET crystalline structure is considered with dielectric constant values of 1, 3 and 5, as shown in Figure 6, through considering both ρ- front gate grains stacks and ρ- back gate grain stack. In Figure 11, the variations of threshold voltage with the device channel distance is made minimum potential across boundary of gate grains, and there is maximum potential changes across gate grains surfaces, with the varied distances of gate grains from 1-5 nm. Figure 12 also shows for gate level high grain bias potential variations of gates voltage with subthreshold drain current; ΔVg for different front and back gate voltages.

Figure 9. Voltage characteristics for distinct ρ-front stack

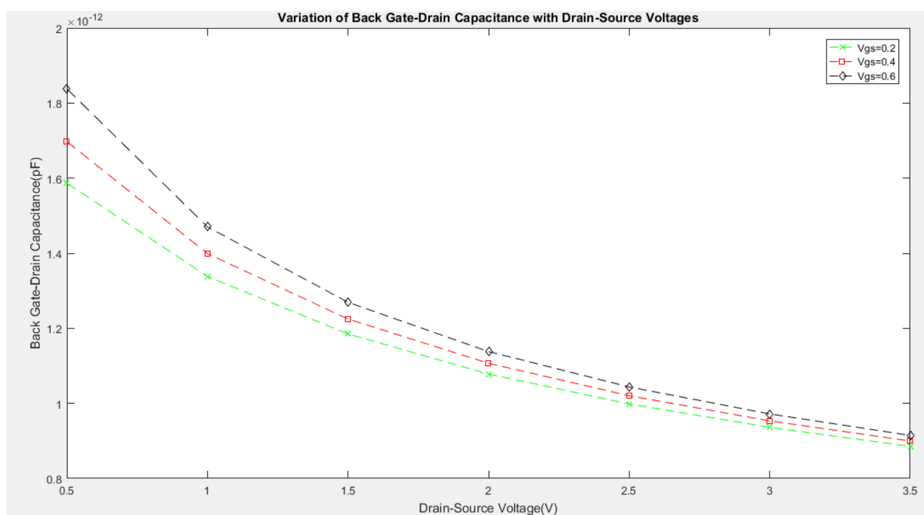

Figure 10. Voltage characteristics for distinct ρ-back stack

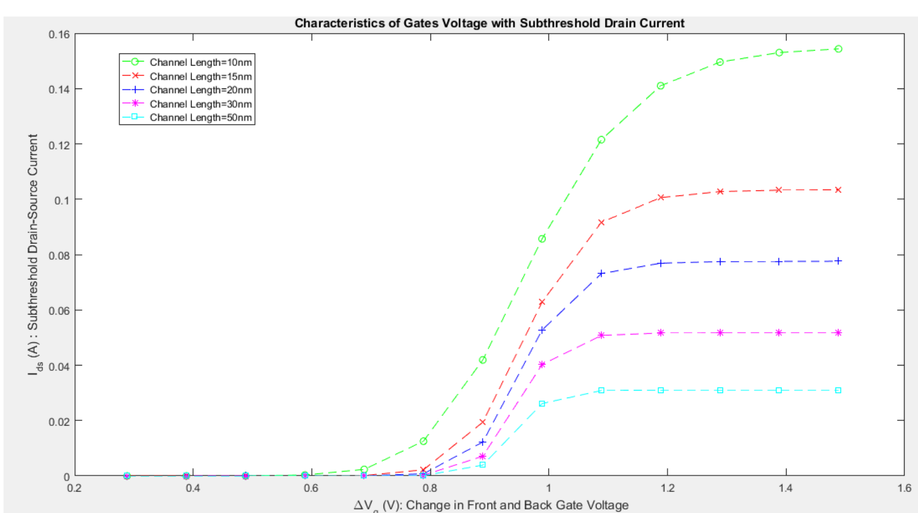

Figure 11. Variation of gates voltage with subthreshold drain current; δVg for different front and back gate voltages

Figures 12, 13, and 14 illustrate the 2-D potential distribution (VD=1 V and VG=1.5 V); Figure 12 for distinct ρ-front gate 2 stack slots; Figure 13 for distinct ρ-back gate 1 stack slots; Figure 14 for distinct ρ-front gate 2 and back gate 1 stack slots. In Figure 14, three grain charges with 1 u, 3 u and 5 u are positioned at a distance among the front gates and back gate device locations at the surface to penetrate the field under high dielectric layer positions.

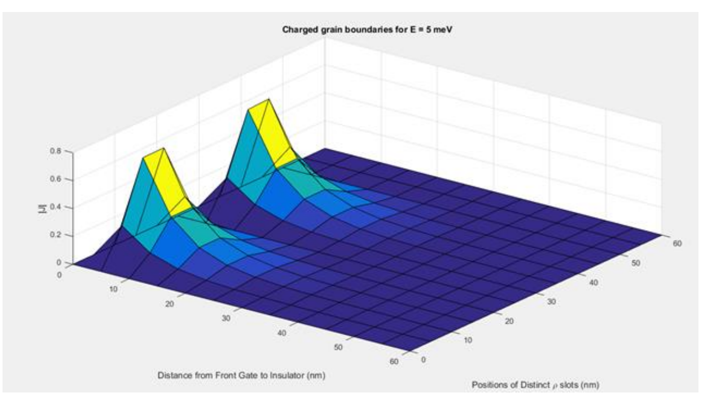

Figure 12. 2-D potential distribution (VD=1 V and VG=1.5 V) for distinct ρ-front gate 2 stack slots

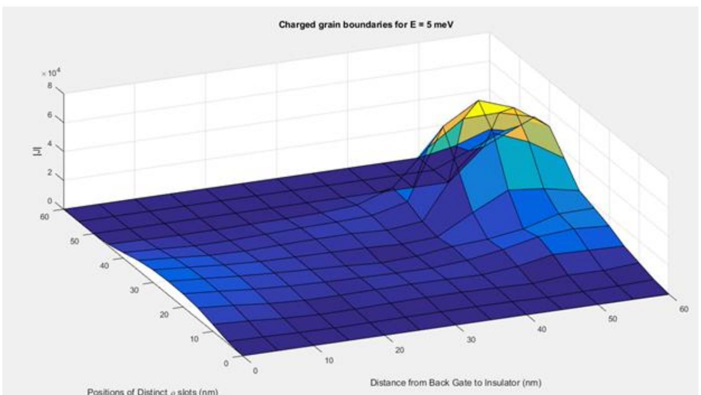

Figure 13. 2-D potential distribution (VG=VD=1.5 V) for distinct ρ-back gate 1 stack slots

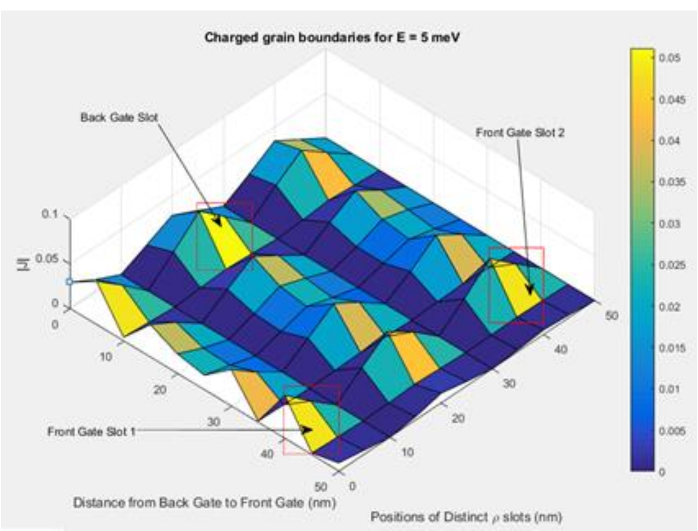

Figure 14. 2-D potential distribution (VG=VD=1.5 V) for distinct ρ-front gate 2 and back gate 1 stack slots

Figure 15 illustrates where the gate stacks-voltage variations are visualized for front gate and back gate on the surface gate stacks. Comparative analysis with TCAD as subthreshold slope modeling and proposed work simulation environment is illustrated in Table 2.

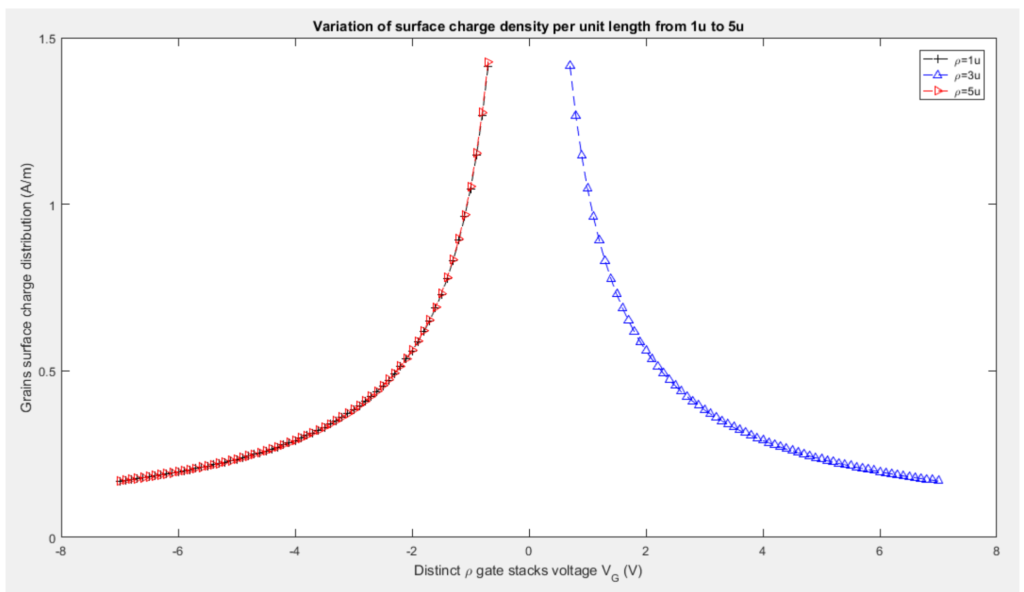

Figure 15. Variation of surface charge distribution for distinct ρ-front gate 2 (ρ=1 u and ρ=5 u) and back gate 1 (ρ=3 u) stack slots

Table 2. Comparative proposed distinct ρ-based model and TCAD as subthreshold slope modeling DG MOSFET

Variable	Front gate distance (nm)	Back gate distance (nm)	Gate length (nm) for Front gate distance	Gate length (nm) for back gate distance	V_{DS} (V)	Subthreshold slope (mV/dec)	DIBL (dec/V)
Subthreshold slope model	50	-	0.1	-	0.2	60	0.02
Proposed model	50	-	0.65	-	0.2	59.75	0.08
Subthreshold slope model	-	30	-	0.1	0.2	60	0.02
Proposed model	-	30	-	0.63	0.2	59.95	0.08

The effect of boundary potential made the subthreshold slope to reduce, even considering zero charge across device stack locations, in turn reducing the drain current to reduce, these limitations are made positive by shifting the current curve towards negative by adding a layer of high threshold voltage. From the above simulation results in 2D and 3D, it is proved that proposed work is having significant value in the implementation of planar DG MOSFET compared to available GAA, FinFETS, and tri-gate MOSFETs.

5. CONCLUSION

The influence of the surface potential polysilicon doping near the boundary in the channel region and the impact of the position-orientation of the boundary between three grains in a polycrystalline gate dielectric is studied. The proposed research work is very useful to understand the electrical parameters of silicon DG MOSFET for doping concentration, dimensions, total internal device capacitance, threshold voltage and drain-source current. The presence of distinct ρ-front and back gate stacks parasitic charge decreases the effect on I-V characteristics of proposed DG MOSFET, through moderate use of dielectric constant value by the use of proposed theoretical simulation parameters by Possions equation having the advantage in usage of consistent and self varying distinct ρ-front and back gate coupling in the estimated DG MOSFET gate regions by resolving the current drift and parasitic diffusion parameters through moderate gate doping. Proposed work simulation results indicates gate level potential variations reduction through charges drift along surfaces and boundaries, by limiting high dielectric traditional DG MOSFET gate material in the

proposed work. The structure of proposed DG MOSFET is chosen to reduce dielectric layer potential fluctuations, in-turn reducing the subthreshold value of the proposed DG MOSFET in the drain current variations compare to the traditional DG MOSFET subthreshold value. Therefore, the significance of this proposed research work is the contribution of a distinct ρ-model to scale DG MOSFET for thermal, static, and dynamic characteristics.

6. FUTURE SCOPE

In this paper, distinct ρ-based DG MOSFET architecture model is proposed through ballistic DG MOSFET device for a compact DG MOSFET model by considering the SCEs parameters scaling and total internal device capacitance, which makes the device to degrades the off-state current and is particularly can be implemented in future DG MOSFET's using ballistic transport equation for further SCEs parameters analysis.

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