Cryogenic Characterization and Modeling of 14 nm Bulk FinFET Technology

Asma Chabane, Mridula Prathapan, Peter Mueller, Eunjung Cha, Pier Andrea Francese, Marcel Kossel, Thomas Morf and Cezar Zota
IBM Research GmbH, Saumerstrasse 4, Ruschlikon 8803, Switzerland, e-mail: zot@zurich.ibm.com

***Abstract*—In this work, we report characterization and modeling of 14 nm bulk FinFET technology from room-temperature down to 4.6 K. A cryogenic device model is used which shows excellent fit to measured data and can accurately predict the performance of the devices at low temperatures. The nMOS device showed satured subthreshold swing of 20 mV/decade, V_T shift of 80 mV and g_m enhancement of 30%, all at 4.6 K. These results show that a tailored cryogenic FinFET technology, i.e. one accounting for the change in V_T and SS, could achieve a sharp reduction of dissipated power by reducing the drive bias. Such technology could have strong impact e.g. in quantum computing, by enabling integration of dense advanced cryogenic ICs inside the cryostat.**

Keywords— cryogenic, subthreshold swing, 14-nm FinFET, compact modeling, quantum computing

I. Introduction

Quantum computing has seen rapid progress in the last few years and there are now roadmaps for quantum systems with over 1000 qubits within the next few years [1]–[3]. Quantum computers today rely on standard high-frequency electronics, such as AWGs and ADCs, and coaxial cables for the control and readout of the qubit processor [4]. Due to cost and complexity, scaling this type of system, i.e. increasing the number of qubits, beyond the few thousands may be challenging. The idea of integrating tailored cryogenic ICs in the cryostat to replace the standard room-temperature equipment has gained increased attention [5]. The quantum architecture benefits in this case from reduced cost and reduced need for cables. So far, dedicated qubit control signal generation ICs at 3-4 K have received the majority of attention [6], [7]. This is in part due to that the control path is less scalable than the readout path, as frequency domain multiplexing is less straightforward and the control equipment costs are higher. Realizing such cryogenic tailored ICs to support dense quantum systems is challenging in part due to the low available cooling power inside the cryostat. Demonstrations today have shown power dissipation of ICs in the range of a few mW per qubit [8]. With a few Watts of available power at 3 K, this places a limit on the number of qubits that can be supported with such electronics. To enable cryogenic ICs with even lower operating power, leveraging the unique features of the cryogenic operation of CMOS transistors is a promising approach [9]. These features include steeper turn on/off characteristics, i.e. lower subthreshold swing (SS), reduced off-current, I_{OFF} and enhanced mobility and on-current, I_{ON}. However, there is also a significant threshold voltage, $|V_T|$, increase, meaning that standard CMOS technologies exhibit lower currents at cryogenic temperatures at fixed bias, and the steeper SS effectively is not leveraged. To enable a cryogenic device technology with superior performance, transistors with either extremely large $|V_T|$, or V_T tuning using a body bias are likely required. In either case, enhanced understanding of the properties of CMOS at cryogenic temperature is needed. Efforts on cryogenic CMOS characterization and modeling, towards a cryogenic PDK as well as tailored device technologies, have so far focused on FDSOI or planar devices, while state-of-the-art FinFET technologies have remained relatively unexplored.

In this work, we characterize and model the operation of commercial 14 nm bulk FinFET CMOS technology down to 4.6 K ambient temperature. We examine the impact of cryogenic operation on key transistor metrics and show that cryogenic properties can be accurately modeled using analytical device models. We report the I_{ON} at fixed I_{OFF} and V_{DD} at 4.6 K and show that given sufficiently large V_T, a tailored cryogenic FinFET technology could achieve >4 times larger I_{ON} than at room temperature, or correspondingly, a strong reduction of dissipated power.

II. Cryogenic Model

In this work, two cryogenic device models recently proposed in [1] have been used, one for the drain current and another for the subthreshold swing, both valid down to cryogenic temperatures. The drain current model relies on the Kubo-Greenwood formalism, which expresses the conductivity as:

$$\sigma = \int_{E_c}^{+\infty} \sigma(E)\left(-\frac{\partial f}{\partial E}\right) dE$$

With E_c, the conductivity band energy and $f(E)$ the Fermi-Dirac statistic, which describes the distribution of particles over energy states:

$$f(E) = \frac{1}{1 + e^{\frac{E-E_f}{kT}}}$$

The conductivity function $\sigma(E)$ can be calculated using the mobility [3][1]:

$$\mu(E) = \frac{1}{qN(E)} \frac{d\sigma(E)}{dE}$$

Where $N(E) = N_{2D}/\left(1 + \exp\left(-E/\Delta E\right)\right)$, is the energy density of states and ΔE the band tail extension. We assume that, at fixed temperature, T, the mobility is constant over E. The FinFETs devices being large enough, we consider a 2D density of states, and we express the energy density of states with an exponential band-tail [1], which leads to:

$$\sigma(E) = q \cdot \mu_0 \cdot N_{2D} \cdot \Delta E \cdot \ln\left(1 + e^{\frac{E}{\Delta E}}\right)$$

It should be noted that the conductivity quickly becomes negligible below the conduction band edge. We assume that

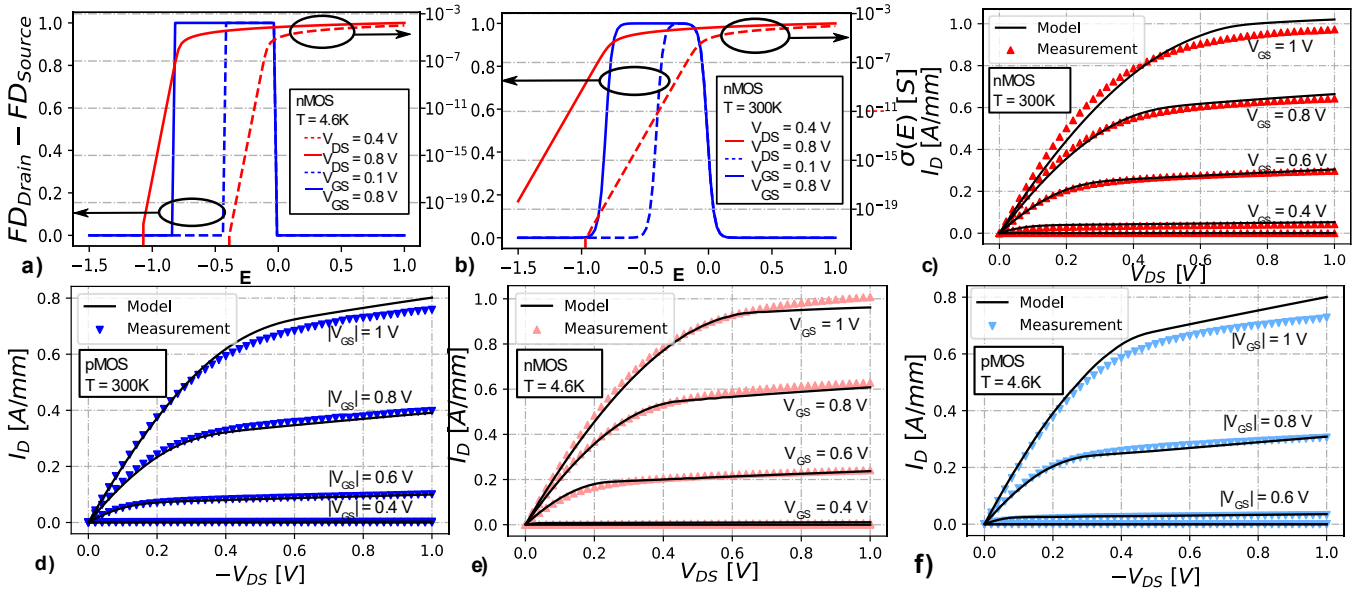

Figure 1: (a) and (b) show the Fermi-Dirac functions and conductivity for nMOS, at V_D = 0.4 and 0.8 V, V_G = 0.1 and 0.8 V, respectively for 4.6 and 300 K. (c), (d) show output characteristics of 14nm FinFET technology nMOS, W = 75 nm and pMOS, W = 76 nm, obtained at $|V_{GS}|$ = 0.2, 0.4, 0.6, 0.8 and 1 V at 300 K. (e) and (f) show the same devices measured at 4.6 K. Solid traces show the modeled values.

the voltage varies gradually along the channel from the drain to the source, thus the drain current is constant (i.e. the gradual channel approximation) and can be expressed as : $I = \mathrm{W} \cdot \sigma(\mathrm{Ef}) \cdot \left(\frac{\mathrm{d}E_f}{\mathrm{dx}}\right) \cdot \frac{1}{\mathrm{q}}$ [1]. After integration over *x*, between the source and drain, the following formula is obtained :

$$I = \frac{W}{qL}\int_{-\infty}^{+\infty} \sigma(E)\left(f(E_{fS}) - f(E_{fD})\right) dE$$

where E_{fS} and E_{fD} respectively denote the Fermi levels at the source and drain, with $E_{fD} = E_{fS} - qVds$.

When a drain voltage is applied, equilibrium is broken by lowering of the band energies on the drain side. This impacts the range of integration of the first integral as it modifies the Fermi level at the drain side. The gate voltage instead affects the conductivity function. At low gate voltage, the potential barrier between the source and the channel is high, so there is no electron flow, and the transistor is in the off state. At higher gate voltage, the barrier is lowered and electrons can flow through the channel. This results in a shift of the energy considered in the conductivity, $\sigma(E - qV_G)$. The function used in the integrand can be seen in Fig. 1 (a) and (b), respectively at 4.6 and 300 K, at different biasing points. In addition, a correction due to the parasitic access resistance between the source and the drain, $R_{DS,}$ has been included in the model by correcting for the change of drain bias $V_D - R_{DS}I_0$ using self-consistent calculations. R_{DS} includes the resistance from the metal wiring and vias.

Several temperature dependent parameters are used in this model. At low temperature, the Fermi potential increases [4] and we observe a mobility increase due to the phonon scattering, which becomes negligible [10]. For each temperature (4.6, 100, 200 and 300 K), mobility, Fermi level, band-tail extension and R_{DS} have been fitted to the measurements. The integration of the drain current has been performed only around the Fermi level as the integrand rapidly decreases when moving away from E_F.

At low temperatures, the subthreshold swing (SS) approaches a constant value, the saturated SS. This effect is considered to be related to the band-tail extension [4]. The band-tail extension corresponds to localized electronic states existing near conduction and valence band edges. Its influence on *SS* is modeled with the saturation temperature parameter, T_S, which depends on the technology used. T_S indicates the transition between the linear region, where the band-tail extension can be neglected and the saturation region, where it dominates the density of states and makes SS higher than its theoretical limit. [4][1]. While an explicit relation between band-tail and saturation temperature exists, $\Delta E = kT_S$, an increasing band-tail extension has been necessary to fit measurement data at higher temperatures [1]. Another important parameter for the fitting is α, as shown in the analytical expression of SS(T):

$$SS(T) = \frac{kT}{q}\frac{C_{ox} + C_d + C_{it}}{C_{ox}}\left(1 + \alpha \ln(1 + \exp\left(\frac{T - T_S}{\alpha T_S}\right)\right)$$

where C_{ox}, C_d, and C_{it} are respectively, the gate oxide capacitance, the depletion capacitance and the interface trap capacitance. The latter two being unknown, we considered ratio values around 1,06 similar to what is used in [1].

III. Measurement Setup and Test Chip

A 14 nm FinFET device test chip was designed for cryogenic characterization. The test devices share source contacts, while drain and gate terminals were wired separately to pads for flexibility and to ensure one shorted device does not prevent measurements of all other FETs. ESD protection was purposely omitted, since such protection structures are large compared to typical FET sizes, which would be used in a low power cryogenic circuit. The leakage and capacitance of the ESD protection circuits could considerably alter the MOSFET device measurements. Even though these FETs can withstand a maximum ESD voltage of only 3V, experience showed ESD protection is not required for careful on wafer measurements. On the other hand, for measurements on packaged devices, ESD damage can become an issue. Cryogenic on-wafer measurements were performed with needle probes in a Janis cryogenic probe station for temperatures between 300 K and 4.6 K. The probe station was

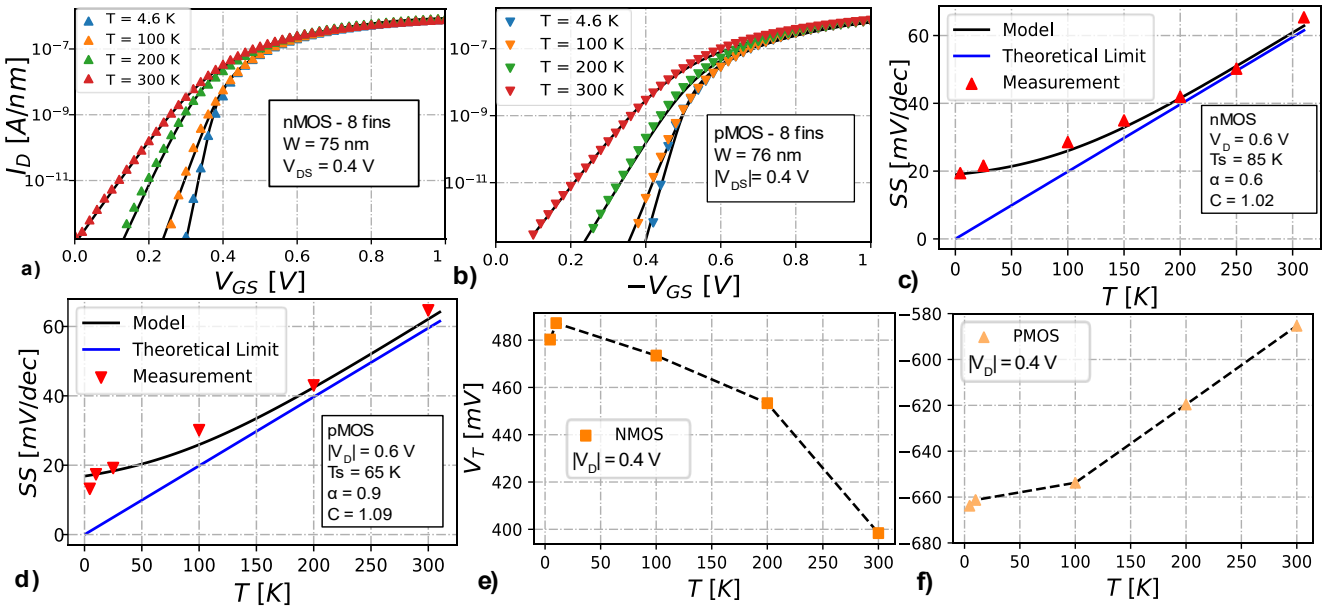

Figure 2: (a) and (b) show input characteristics of 14nm FinFET technology nMOS, W = 75 nm and pMOS, W = 76 nm, obtained at $|V_D|$ = 0.4 V for 300, 200, 100 and 4.6 K. (c) and (d) show subthreshold slope versus temperature for nMOS and pMOS devices, saturating around 20 mV/dec. (e) and (f) show threshold voltage extracted from linear interpolation at peak transconductance.

cooled with liquid helium. Due to the large wiring resistance of approximately 70 Ohms, all measurements were done in Kelvin probe configuration.

IV. RESULTS

In this section, we compare the measurement results to the cryogenic device model previously discussed, over a wide range of temperatures, from 300 K down to 4.6 K. Fig. 1(c) and (d) show the I_D-V_D characteristics of nMOS and pMOS devices, respectively, from $|V_{DS}|$ = 0.2 to 1 V, at 300 K. The devices have 2 gate fingers, each with 4 fins with a gated circumference of 76 nm (pMOS) and 75 nm (nMOS) per fin. Device data is normalized to the total gated circumference. Fig. 1(e) and (f) are showing the output characteristics for the same devices at 4.6 K. The model obtains a close fit to the measured data, with a slight deviation at high V_{GS}. This may be due to e.g. self-heating, surface roughness scattering or other non-ideal effects [11], [12]. Self-heating, in particular, will be pronounced at high-bias/current conditions at low temperature. Self-heating can reach values around 30 K for these types of devices, meaning that a reduction of the drain current relative the model can occur [12]. Generally, the output or characteristics in the on-state remain relatively unchanged at cryogenic temperature. The reason for this is that the reduction of I_{DS} due to the $|V_T|$ increase is approximately cancelled out by an increase of the mobility.

Cryogenic operation mainly impacts the off-state performance, as seen in Fig. 2(a) and (b), which show the transfer characteristics for the same devices, at 300, 200, 100 and 4.6 K ambient temperatures and $|V_{DS}|$ = 0.4 V. We chose 0.4 V here in order to reduce self-heating. Both devices exhibit an increase of the threshold voltage at lower temperatures, as well as a reduction of SS. The device model is able to accurately capture the off-state characteristics. SS is further shown in Fig. 2(c) and (d), for the nMOS and pMOS devices, respectively, at $|V_{DS}|$ = 0.6 V. The figures show the measured data, the modeled values and the theoretical *SS* limit corresponding to k_BT/q. The experimental results closely follow the theoretical limit down to 150 K before starting to saturate. At cryogenic temperatures, the measured SS saturates around 20 mV/decade. This can be explained by an exponential band-tail, which results from intrinsic mechanisms, such as electron-hole interaction, or crystalline periodicity [13]. An additional cause can be the presence of interface traps [11]. The saturation temperature, T_S = 85 K, indicates the temperature at which the measured data significantly deviates from the standard k_BT/q model. Compared to other results for planar technologies, such as 28 nm FD-SOI, these FinFET devices show similar saturation SS, as well as saturation temperature [14]. While reduction of both these parameters would be beneficial for ultra-low power operation, saturation of *SS* at a sufficiently low value could be beneficial in order to make device characteristics robust against self-heating effects.

The threshold voltages for the two devices are shown in Fig. 2(e) and (f), measured at $|V_D|$ = 0.4 V, using extrapolation from peak transconductance. The $|V_T|$ increases by around 80 mV for both nMOS and pMOS, which is lower than the 135 to 225 mV Bulk CMOS values, reported in [15]. This difference could be either intrinsic, or due to slight differences in methodology. The peak transconductance for the two devices is shown in Fig. 3(a) at $|V_D|$ = 0.4 V. For the nMOS, g_m increases by 30%, from 1.3 to 1.7 S/mm. For the pMOS, g_m increases by 17%, from 1.7 to 1.98 S/mm. The increase of g_m is likely due to the increase of mobility, which is related to the decrease of phonon scattering at low temperatures [16]. As shown, the hole and electron mobilities exhibit different temperature dependencies. Fig. 3(b) shows the transconductance efficiency, g_m/I_D, at V_D = |0.4| V. At low temperature, an improvement of 21%, from 4.14 to 5 V^{-1} for nMOS and 13%, from 2.98 to 3.37 V^{-1} for pMOS can be observed. This improvement could lead to power savings at cryogenic temperature, as well as improved high-frequency performance, in particular for low-noise amplifier (LNA) applications, as higher g_m/I_{DS} yields lower minimum noise temperature in LNAs.

The on-state current, I_{ON}, has been measured at constant off-state current of I_{OFF} = 1 nA, V_D = 0.4 V, and V_{GS} = $V_{GS,off}$ +

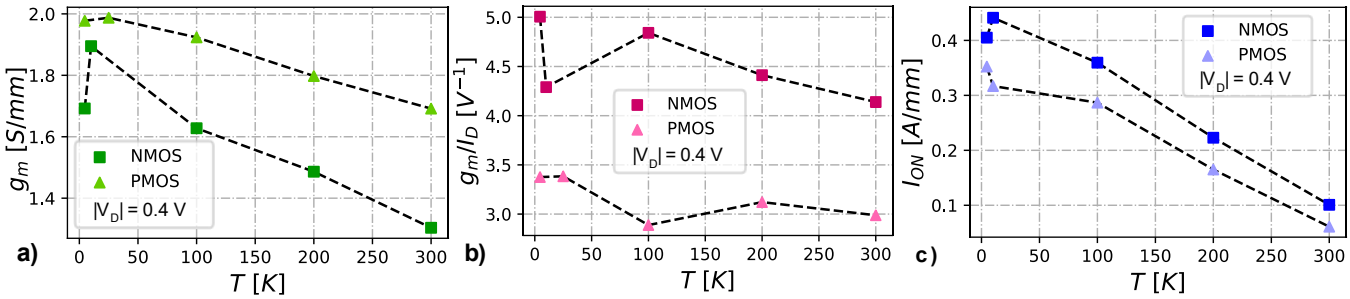

Figure 3: Analog design parameters versus temperature for 14nm FinFET technology nMOS, W = 75nm (square markers) and pMOS, W = 76nm (triangle markers), obtained at $|V_D|$ = 0.4V (a) Peak transconductance (b) Transconductance efficiency (c) on-state current measured at I_{OFF} = 1 nA.

Technology (at 4 K)	Type	Min. SS mV/dec.	ΔVth mV	g_m or I_D increase	I_{ON} increase
This work (14 nm FinFET)	***nMOS***	***20***	***80***	***30% (0.4 V)***	***4x (0.4 V)***
This work (14 nm FinFET)	***pMOS***	***15***	***80***	***17% (0.4 V)***	***6x (0.4 V)***
28 nm bulk CMOS [17]	nMOS	20	160	22 % (0.9 V)	--
28 nm FD-SOI [9]	nMOS	5	160	--	--
40 nm bulk CMOS [18]	nMOS	28	120	13% (1.1 V)	3.5x (0.6 V)
160 nm bulk CMOS [18]	nMOS	23	150	67% (1.8 V)	3x (0.6 V)

Figure 4: comparison table of cryogenically characterized CMOS technologies in literature.

0.4 V, where $V_{GS,off}$ is the gate bias at I_{OFF}. Thus, this method accounts for the V_T shift in the devices. Fig. 3(c) shows a consistent enhancement of I_{ON} from 300 K to 4.6 K, which is enhanced by a factor 4 for nMOS, going from 60 to 245 µA and by a factor 6 for pMOS, from 35 to 214 µA. The greater enhancement for the pMOS is due to the steeper SS exhibited by these devices at 4.6 K. While the increase of I_{ON} at 4.6 K is impressive and could be leveraged for tailored cryogenic CMOS with lower V_{DD}, the shift in V_T must be accounted for through design of an ultra-high-V_T technology. In addition, the V_T variability, must be accounted for and will limit the smallest value of SS that can be leveraged [9].

Fig. 4 shows a comparison table of cryogenically characterized CMOS technologies in literature. This work presents the first characterization of 14 nm FinFETs at 4.6 K. We note that there are some differences in the methodologies used to determine these values between different references. The column "g_m or I_D increase" indicates the increase of either g_m or I_D at 4 K compared to 300 K, which is an approximate measure of the mobility enhancement. Compared to other technologies, the 14 nm FinFETs exhibit similar saturated *SS* at cryogenic temperatures, while there are reports of 28 nm FD-SOI technology reaching down to 5 mV/decade. I_{ON} is here defined as stated above.

V. Conclusions

We have characterized and modeled 14 nm bulk FinFET technology down to 4.6 K. A cryogenic device model based on Kubo-Greenwood formalism showed good fits to measured drain currents and subthresholdold swings and can be used to accurately predict the performance of 14 nm FinFET technology at cryogenic temperatures. The nMOS device, for instance, showed satured subthreshold swing of 20 mV/decade at 4.6 K, V_T shift of 80 mV and g_m enhancement of 30%. These improvements at low temperatures resulted in an increase of I_{ON} (at fixed I_{OFF} and V_{DD}) of a factor 4. To leverage these enhanced properties, a tailored cryogenic CMOS technology is required, with low V_T variability, and with ultra-high V_T matching the cryogenic values. The realization of such a technology would enable cryogenic electronics with extremely low power dissipation, that could support quantum computers with very large number of qubits.

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