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Zero-Bias Power-Detector Circuits based on MoS_2 Field-Effect Transistors on Wafer-Scale Flexible Substrates

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The design, fabrication, and characterization of wafer-scale, zero-bias power detectors based on 2D MoS_2 field-effect transistors (FETs) are demonstrated. The MoS_2 FETs are fabricated using a wafer-scale process on 8 µm-thick polyimide film, which, in principle, serves as a flexible substrate. The performances of two chemical vapor deposition MoS_2 sheets, grown with different processes and showing different thicknesses, are analyzed and compared from the single device fabrication and characterization steps to the circuit level. The power-detector prototypes exploit the nonlinearity of the transistors above the cut-off frequency of the devices. The proposed detectors are designed employing a transistor model based on measurement results. The fabricated circuits operate in the Ku-band between 12 and 18 GHz, with a demonstrated voltage responsivity of 45 V W^{-1} at 18 GHz in the case of monolayer MoS_2 and 104 V W^{-1} at 16 GHz in the case of multilayer MoS_2, both achieved without applied DC bias. They are the best-performing power detectors fabricated on flexible substrate reported to date. The measured dynamic range exceeds 30 dB, outperforming other semiconductor technologies like silicon complementary metal–oxide–semiconductor circuits and GaAs Schottky diodes.

1. Introduction

The mechanical flexibility and electronic transport properties of 2D materials allow their integration on flexible substrates and provide a high potential for transparent bendable and wearable electronics. With a higher charge-carrier mobility than organic semiconductors, 2D materials, such as graphene, black phosphorus (BP), and transition metal dichalcogenides, are in the lead toward the realization of such applications that cannot be achieved with conventional semiconductor technologies.[1–8] Pioneered by the successful mechanical exfoliation of graphene in 2004,[9] an ample number of articles have been published with graphene-based devices and circuits, both on rigid and flexible substrates.[10–18] However, the lack of a bandgap in graphene intrinsically prevents graphene field-effect transistors (FETs) from achieving a distinct OFF state in digital circuitry and limits their achievable current saturation in the output characteristics (drain current, I_{ds}, vs source–drain voltage, V_{ds}). The latter considerably lowers f_{max} of the transistors and limits their performance in terms of power gain in high-frequency designs.[19–22] In contrast to graphene, BP possesses a thickness-dependent direct bandgap that enables transistors with a high ON/OFF current ratio.[23,24] BPs appealing characteristics are somewhat compromised by the lack of stability under ambient conditions and a resulting rapid degradation of its electrical

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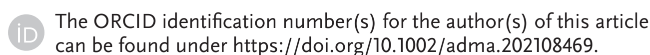
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properties,[7] although encapsulation methods may mitigate this fact.[25,26] Molybdenum disulfide (MoS_2) has attracted interest as a semiconducting 2D material with high stability in ambient air.[1] The presence of an energy gap between 1.3 and 1.8 eV in the multi- and single-layer form permits ON/OFF ratios as high as 10^8 in MoS_2 FETs. This enables electronic circuits, both in the digital[27,28] and the relatively high-frequency analog[29] domains. In addition, the current saturation in the device output characteristics have led to maximum extrinsic f_T and f_{max} of 4 and 10 GHz, respectively, in devices on flexible substrates.[4] Finally, MoS_2-based diodes have been used to build low-power flexible integrated transceivers.[30,31]

Based on these considerations, MoS_2-based low-power wireless transceivers are an attractive and feasible goal toward implementing high-performance microwave electronic circuits on flexible substrates. However, while radio-frequency (RF) mixers[5,32] and amplifiers[6] operating in the megahertz range have been reported, power detectors as important building blocks are still missing. They are typically employed either to detect small signals close to the noise level or to monitor large signal levels. The power detector relies on the nonlinear operation of a single FET. Proper gate biasing (in this case, 0 V) can be applied to operate the device in the square-law region to obtain a DC voltage/current at the transistor drain which is proportional to the RF power delivered to the gate. The working principle relies on the nonlinear characteristic of the active device(s) at the operating point. Under a small-signal voltage, *av*, the current–voltage relation of the device can be represented by a Taylor expansion[33]

$$I = f(V) = f(V_0) + \frac{df}{dV}(av) + \frac{1}{2}\frac{d^2 f}{d^2 V}(av)^2 \quad (1)$$

where V_0 is the bias voltage that defines the operation point and where the derivatives are evaluated. By assuming that higher-order terms are sufficiently small, and due to the symmetry of the linear term, the DC component originates from the second-order term. Therefore, detectors function as square-law rectifiers when the input signal is sufficiently small. Graphene p–n junction or Schottky diodes have been used as power detectors due to their high performance together with their well-established process technology.[15,34] However, these are not easily integrable on-chip and most designs require biasing. Consequently, the noise performance is lowered in comparison to zero-bias designs, which only exhibit thermal noise. Moreover, silicon complementary metal–oxide–semiconductor (CMOS)-based designs have also been implemented as integrated power detectors,[35,36] but are limited in dynamic range and are not suitable for flexible substrates.

Power detectors are generally used in numerous analog wireless applications in different fields such as radar systems, RF identification (RFID) transceivers, or mobile communications.[37] In addition, they are one of the basic components in six-port receivers, together with local oscillators and low-noise amplifiers.[8] The architectures of such receivers present lower complexity in comparison to other front-ends, and potentially allows fully integrated flexible RF front-end design when based on MoS_2 technology. In this work, we report the successful implementation of zero-bias RF power detectors based on two different MoS_2 FETs with mono- and multilayer channel materials, both fabricated with a scalable and manufacturable growth technique.

2. MoS_2 FET Fabrication and Characterization

The MoS_2 films were grown by metal–organic vapor phase deposition (MOCVD)[38,39] on 2 in. sapphire wafers. Multilayer material (M) was deposited using di-*tert*-butyl-sulfide (DTBT) as the sulfur precursor,[38] while H_2S was selected for the monolayer material (S) deposition.[39] The Raman spectra of both materials after transfer onto SiO_2 test substrates show that the distance between the E^1_{2g} and A_{2g} peaks of the M-material is larger than for the S-material, indicating a larger thickness of the former[40] (**Figure 1**a). The statistical distributions of this peak separation, extracted with the help of 625 Raman spectroscopic measurements in an area of 50 µm × 50 µm, are shown in the inset of Figure 1a. The difference in thickness of the two materials, as well as the surface roughness and morphology, was confirmed by atomic force microscopy (AFM) scans, the single layer material (S) is 0.9 nm thick while the multilayer material (M) is 5 nm thick. More information on the AFM scans can be found in Section S1 of the Supporting Information.

The MoS_2 FETs were fabricated on a flexible 8 µm-thick polyimide (PI) film on silicon wafers with standard photolithography. The flexible layer of the desired thickness was obtained by spin coating the liquid PI on a Si carrier substrate and by curing the substrate at 350 °C for 30 min. The back gate consists of a 100 nm-thick aluminum (Al) layer followed by a 35 nm-thick titanium (Ti) layer, which was deposited via electron beam evaporation. An aluminum oxide (Al_2O_3) gate insulator with a thickness of 35 nm was deposited in an atomic layer deposition (ALD) system. The oxide thicknesses were confirmed by ellipsometry. Commercially available hexagonal boron nitride (h-BN) layers and different MoS_2 layers were transferred from their respective growth substrates onto these prepatterned PI on silicon substrates with a wet transfer technique. The MoS_2 was then covered with a second layer of h-BN in order to improve the quality of the interface.[41,42] The channel was patterned by reactive ion etching (RIE) and the electrical contacts to the h-BN/MoS_2/h-BN stack were realized by DC sputtering of a 50 nm-thick nickel layer. The DC sputtering, combined with the RIE step allowed us to contact the MoS_2 layer from the edge of the material, thus creating edge contacted devices. This contact scheme results in reasonable values of contact resistance[43–45] although more recent methods have emerged that we have not yet been able to implement.[46] After the contacts, a 75 nm-thick encapsulation layer of Al_2O_3 was deposited by ALD. Finally, electron beam evaporation was used again to deposit the final Al metallization as probing pads. A schematic of the devices is shown in Figure 1b and optical microscopy images of mono- and multilayer MoS_2 devices with two parallel channels are shown in Figure 1c,d, respectively.

The mask layout for the MoS_2 FETs includes different channel dimensions and the same mask set was used for the M- and the S-type devices. DC transfer (drain current, I_{ds}, vs gate voltage, V_{gs}, in **Figure 2**a) and output (drain current, I_{ds}, vs drain voltage, V_{ds}, in Figure 2b,c) characteristics were measured at room

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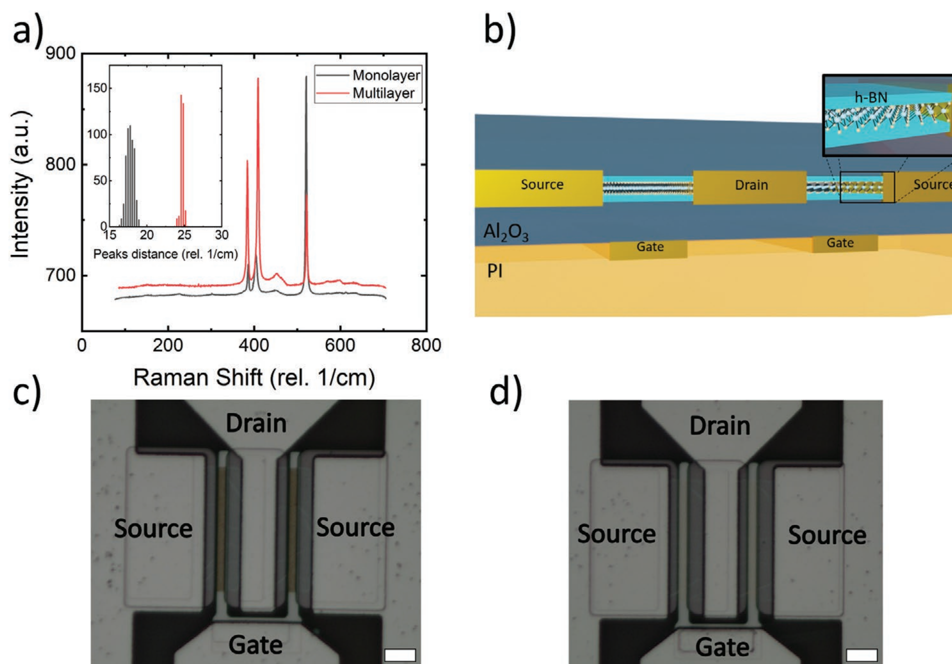

Figure 1. a) Raman characterization of both MoS_2 batches after the transfer onto a SiO_2 test substrate. The inset shows the statistical distribution of the distance between the E^1_{2g} and A_{2g} resonance peaks of MoS_2. b) Schematic cross-section of the MoS_2 devices. c) Optical microscopy image of the multilayer MoS_2 device. d) Optical microscopy image of the monolayer MoS_2 device. The scale bar is 16 µm.

temperature and ambient air with a semiconductor parameter analyzer. The gate length and width of these two MoS_2 FETs are L = 6 µm and W = 60 µm, respectively. The transfer characteristics were measured at a constant V_{ds} = 1 V with increasing and decreasing V_{gs} sweeps, plotted as solid and dashed lines, respectively. An ON current of 12.8 and 16.8 µA was measured for the M- and S-materials, respectively. We define ON current as the value of current flowing across the device for a specific $V_{gs} - V_{th} > 0$ V (in this case, $V_{gs} - V_{th}$ = 4.4 V), i.e., when the transistor is biased above the threshold voltage, V_{TH}. The transfer characteristic allowed us to extract the carrier mobility from the transconductance (g_m) of the devices. The resulting mobility is $\mu_{gm,M}$ = 1.5 cm^2 V^{-1} s^{-1} and $\mu_{gm,S}$ = 1.8 cm^2 V^{-1} s^{-1} for the multilayer and monolayer materials, respectively. The analysis of the curves with the Y function method ($I_{ds}/\sqrt{g_m}$) allowed the calculation of the low field mobility (μ_0) and contact resistance (R_C) from a single transfer curve, and resulted in $\mu_{0,M}$ = 1.63 cm^2 V^{-1} s^{-1}, $\mu_{0,S}$ = 2.18 cm^2 V^{-1} s^{-1}, $R_{C,S}$ = 100 kΩ µm, and $R_{C,M}$ = 131 kΩ µm. It is known that the low field mobility from the Y function is an extraction method that excludes the effects of the contact resistance, therefore higher μ_0 values were expected.[47,48] The constant current method was used to estimate the value of the threshold voltage.[49] For a defined drain current of 1 µA, we obtain $V_{TH,\,M}$ = –7.5 V and $V_{TH,\,S}$ = –4.4 V. A small clockwise hysteresis is observed for the M devices, which is a common phenomenon in MOSFETs with MoS_2 channels.

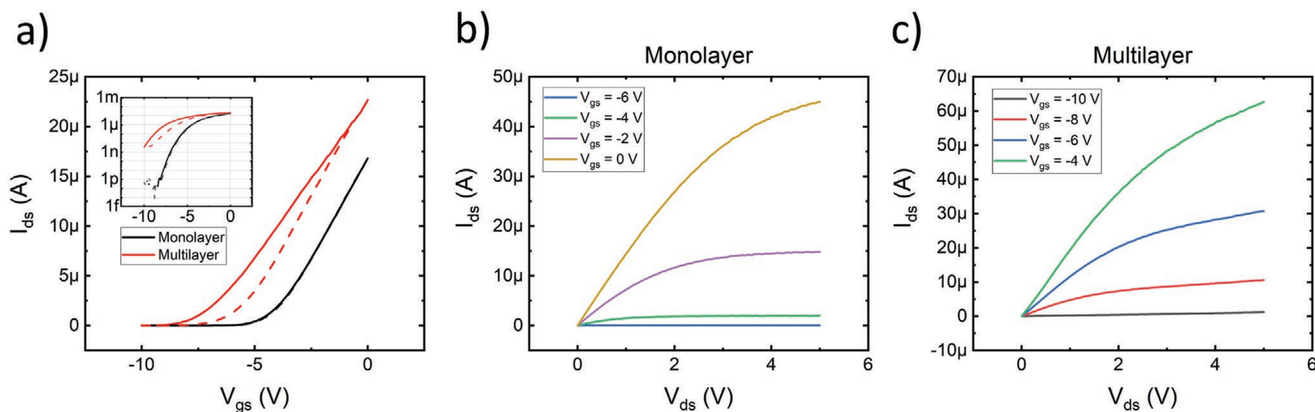

Figure 2. Transfer characteristic of the M-type (red) and S-type (black) MoS_2 devices at V_{ds} = 1 V. The dimensions of the devices are L = 6 µm and W 60 µm. The dashed lines represent backward voltage sweep and show the presence of hysteresis in the measurements. In the inset the same data are plotted in a semilog scale. b) Output characteristic of a monolayer MoS_2 device. c) Output characteristic of a multilayer MoS_2 device.

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Table 1. Comparison of the DC characteristics of the monolayer and multilayer material devices.

	μ_{gm} [cm^2 V^{-1} s^{-1}]	$\mu_{0,\text{ Y Function}}$ [cm^2 V^{-1} s^{-1}]	R_C [kΩ µm]	Threshold voltage [V]	Subthreshold swing [mV dec^{-1}]	ON/OFF current ratio
Monolayer	1.8	2.18	100	–7.5	300	1.25×10^8
Multilayer	1.5	1.63	131	–4.4	900	2.6×10^4

It is usually an indicator of the presence of border traps which are negatively charged during the sweep in the gate oxide of the transistors.[41,50] One can observe some substantial differences in the curves other than hysteresis for the M-material, e.g., a clear degradation of the inverse subthreshold slope (or subthreshold swing, SS) and a reduction of the ON/OFF ratio, compared to the S-material. This may be attributed to the presence of a higher amount of defects, such as sulfur vacancies, in the multilayer material.[51] Since sulfur vacancies have been found to be responsible for an n-doping effect of MoS_2,[52] this would be also consistent with the larger negative threshold voltage of the M-device. Although many methods for the reduction of hysteresis and defect passivation exist, they usually require either high-temperature annealing steps[53,54] or noncleanroom-standard chemical treatments[55,56] and they are not used in this work due to the lack of comparative studies in literature about such processes for flexible devices. The devices were additionally tested on bending rods with different radii and after several bending cycles. Both devices batches show some degradation of the performances after the peeling of the devices. The devices fabricated with the S-material get damaged after the bending tests with the minimum bending radius, while the devices fabricated with the M-material are able to withstand up to 1000 bending cycles without major performances loss. The results are summarized in the Supporting Information while a compilation of the main DC characteristics of both devices batches is summarized in **Table 1**. The high-frequency response was characterized by standard two-port *S*-parameter measurements with different bias conditions ranging from –16 to 5 V for V_{gs} in the M-transistors, –7 to 5 V for V_{gs} in the S-transistors, and from 0 to 11 V for V_{ds}. The channel lengths of the RF-measured S- and M-transistors were 6 and 5 µm, respectively, while the width was 60 µm for both devices. Measurements were carried out from 10 MHz to 40 GHz on-wafer by means of ground-signal-ground (GSG) pads attached to the intrinsic transistor, as shown in Figure 1c. The resulting S_{11}, S_{22}, and S_{21} are plotted in **Figure 3** for 0 V at the gate and drain. As expected for symmetric devices, S_{12} and S_{21} are equal. From the *S*-parameter measurements, the current gain, h_{21}, and the maximum available gain (MAG) were calculated in order to extract the transient frequency, f_T, and the maximum oscillation frequency, f_{max}, (**Figure 4**). Defined as the magnitude at which h_{21} becomes unity, f_T equals 57.7 and 33.27 MHz for the M- and S-transistors, respectively. Similarly, defined as the magnitude at which the MAG equals unity, the obtained f_{max} is 236.6 and 114.1 MHz. These figures-of-merit were extracted in both transistor types for a V_{gs} = 1 V and a V_{ds} = 11 V. The performance is in line with typical values of state-of-the-art flexible MoS_2-based RF devices[6,32] considering the dimensions of the transistors. f_T and f_{max} of an MOSFET, considering drift-diffusion transport and without considering short-channel effects, can be expressed as

$$f_T = \frac{1}{2\pi}\frac{g_m}{C_{gs}} = \frac{1}{2\pi}\frac{3}{2}\frac{\mu}{L^2}\left(V_{gs} - V_{th}\right) \tag{2}$$

and

$$f_{max} = \frac{1}{2}\frac{f_T}{\sqrt{R_g\left(g_{ds} + f_T C_{gs}\right)}} \tag{3}$$

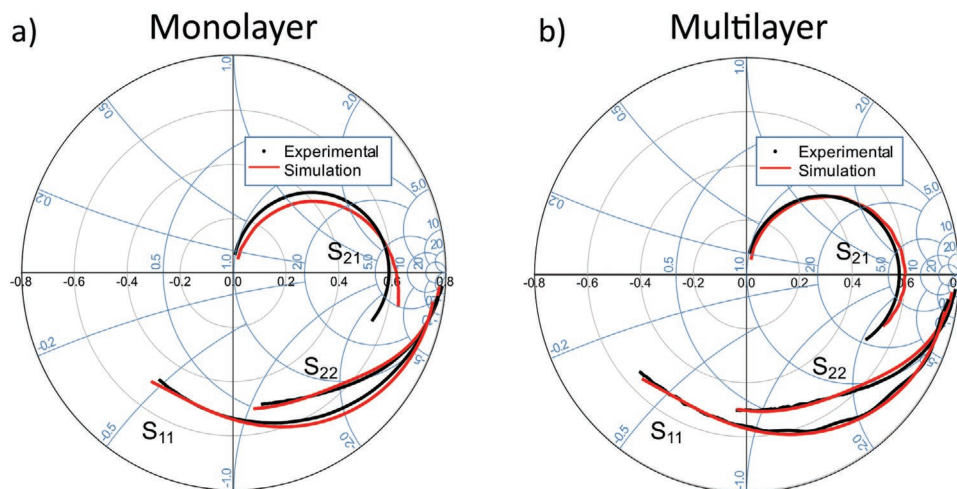

Figure 3. *S*-parameter measurement results at 0 V V_{gs} and 0 V V_{ds} from 1 to 40 GHz. S_{11} and S_{22} are plotted in the Smith chart, while S_{21} is shown in the superimposed polar plot. The measured results are scattered in black and compared with simulations plotted in a solid red line based on the developed device model.

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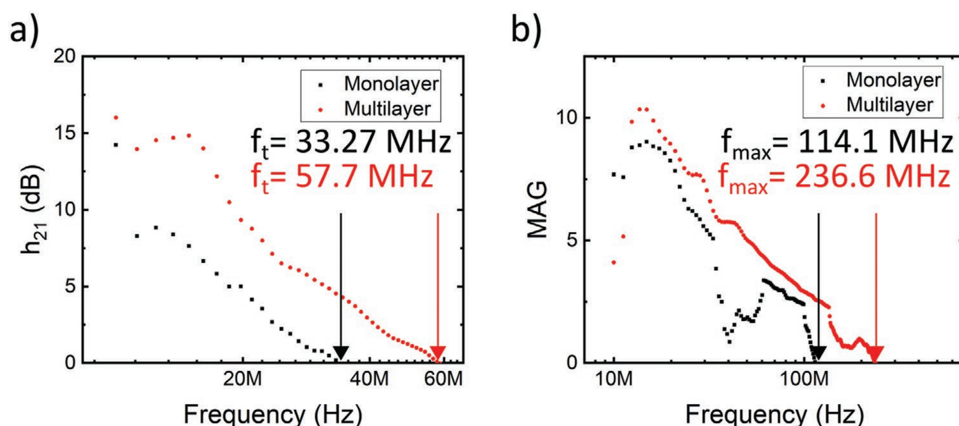

Figure 4. a,b) Comparison of the current gain, $h_{2,1}$, of the two fabricated transistors (a), and of the maximum available gain for the two types of transistors (b).

where μ is the carrier mobility, L is the gate length, R_g is the gate electrode resistance, and g_{ds} is the output conductance.[57] f_T is inversely proportional to the square of the length of the channel (Equation (2)), which explains the difference in performance between the S- and M-devices.

Although there is great interest in improving these two figures of merit (FOMs) of transistors, only microwave circuit applications that make use of the transconductance rely on them.[58] When operated in the linear region at zero V_{ds} bias, transistors behave as a nonlinear gate voltage-controlled resistor and allow applications beyond f_T and f_{max}. Since the mobility also relies on the transconductance, the same argument can be used to explain the high performance of the circuit in terms of frequency (Section 3), despite the extracted low mobility values (Table 1). The extracted model from S-parameter measurements at this operating point (V_{ds} = 0 V) can be simplified as shown in **Figure 5**a, where no g_m is included. The values of the lumped components of the transistor model were extracted from S-parameter measurements according to ref. [59] and are listed in **Table 2**. The equivalent circuit encompasses the intrinsic transistor at the operating point and the parasitic elements of the gate, source, and drain series resistances. Moreover, the resistance to the substrate is included as well as an extra capacitance at the source that increases the asymmetry between the ports. These are related to the pads and the measurement parasitics. Simulations of the equivalent circuit for the transistor at zero bias were performed with the Advanced Design Systems (ADS) software from Keysight, and a good agreement between the model and the measurement results was achieved (Figure 3).

3. MoS_2 Power-Detector Circuit

Power detection requires a nonlinearity in the circuit, as presented in Equation (1). In the proposed design, this is

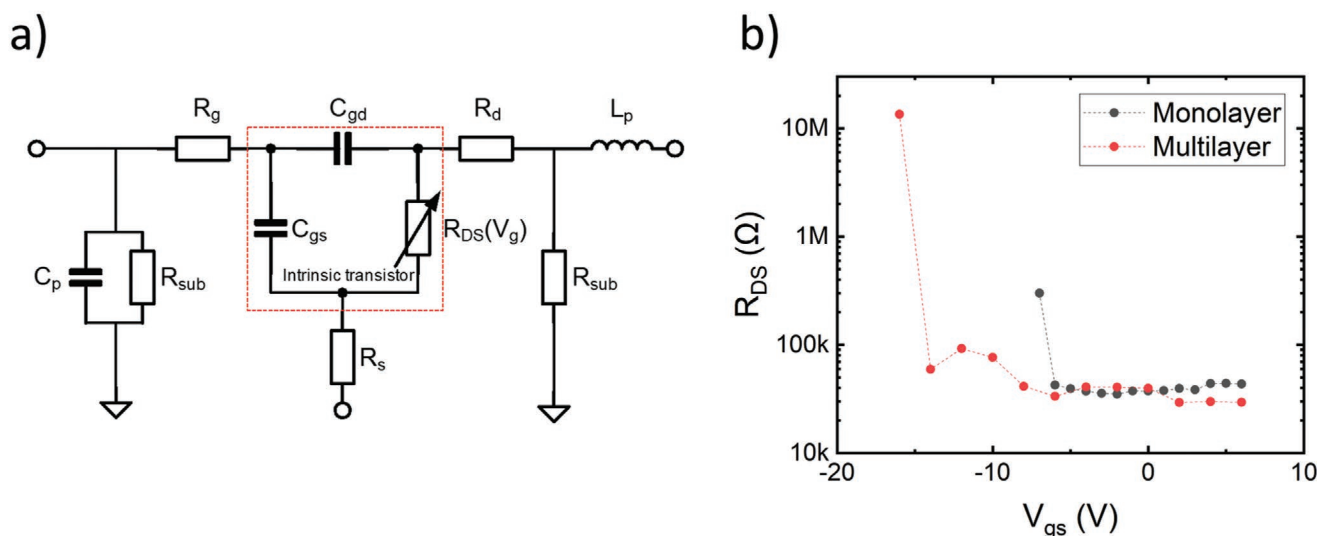

Figure 5. a) Small-signal equivalent circuit for the operating point at V_{ds} = V_{gs} = 0 V. The intrinsic components of the transistor are located inside the red dashed square. The variable R_{DS} represents the nonlinearity of the channel as a function of V_{gs}. R_g, R_d, R_s are the extrinsic elements and C_p, L_p, and R_{sub} are parasitic components. b) Extracted values for R_{DS} over the applied gate voltage range.

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Table 2. Extracted values of the lumped components of the small-signal equivalent circuit.

	R_g [Ω]	R_s [Ω]	R_d [Ω]	C_{gd} [pF]	C_{gs} [pF]	C_p [pF]	L_p [nH]	R_{sub1} [Ω]	R_{sub2} [Ω]
Monolayer	7	5	5	0.11	0.065	0.055	0.01	2000	6000
Multilayer	5	10	7	0.14	0.09	0.065	0.02	2000	6000

incorporated through the modulation of the channel resistance with the gate voltage. Represented as R_{DS} in Figure 5a, the resistance variation with respect to V_{gs} is modeled from the *S*-parameters for different gate bias voltages and constant V_{ds} = 0 V. This nonlinear response of R_{DS} for the two transistor types can be observed close to their respective threshold voltage in Figure 5b. Effectively, the transistors can be considered in their OFF-states at V_{TH}. This behavior was implemented in the simulation with a high-order polynomial fitted to the extracted values. The difference between the V_{TH} values obtained in the DC characterization and the ones presented in the model could be ascribed to some instability in the threshold voltage values. The analysis of the threshold voltage stability measurements is summarized in Section S3 in the Supporting Information.

The power-detector architecture is depicted in **Figure 6**a, where the transistors are on-wafer and further elements are connected externally. The input signal with calibrated power, P_{in}, is provided by the RF source of the microwave vector network analyzer (VNA) through the internal bias tee. The VNA is connected to the gate of the transistor and the bias voltage is set to 0 V. At the gate input, an external 50 Ω coaxial load is included to match the input. The output signal is conducted from the drain to an external bias tee that acts as a lowpass filter (LPF). The RF signal is short-circuited to ground and the DC output is measured with the voltmeter across an 800 kΩ load. Since the expected frequency performance is not related to the f_T and f_{max} of the transistor, the 3 dB RF detection bandwidth is defined as[60]

$$f_{3-dB} = 1/\left(2\pi\left(C_{gs} + C_{gd}\right)R_g\right) \tag{4}$$

This frequency is calculated from the equivalent circuit to be ≈122 and 128 GHz for the M- and S-transistors, respectively, far beyond the cutoff frequencies of the transistors. Nevertheless, this estimated value considers neither the parasitic components nor the nonideal externally connected components.

Previous to the actual power-detector measurements, one-port *S*-parameter measurements were carried out in order to identify the best matched frequencies up to 50 GHz. With a −10 dB matching criteria, S_{11} at the input of the VNA was used as the determining factor to choose the frequencies for the power detection setup. Based on these measurements, 16 and 18 GHz were chosen for the M- and S-FETs, respectively. The measured output voltage as a function of the input RF power for these two frequency responses is shown in Figure 6b. Both transistor types present a similar performance in terms of dynamic range, where the linear-in-dB region extends from −30 up to 0 dBm of input power. The large dynamic range of 30 dB is comparable

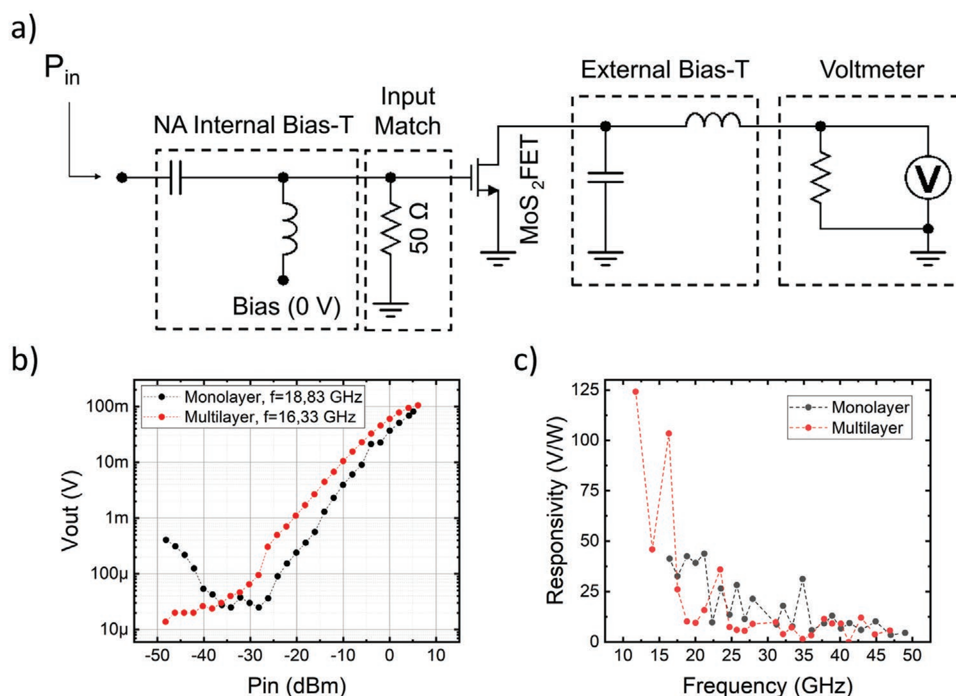

Figure 6. a) Schematic of the power detector with the on-wafer transistor. b) Measured output voltage as a function of the input power at 16.33 GHz for the multilayer (M) device and at 18.83 GHz for the monolayer (S) device. Both detectors show a similar dynamic range of around 30 dB. c) Responsivity comparison between the monolayer (S) and multilayer (M) devices over frequency.

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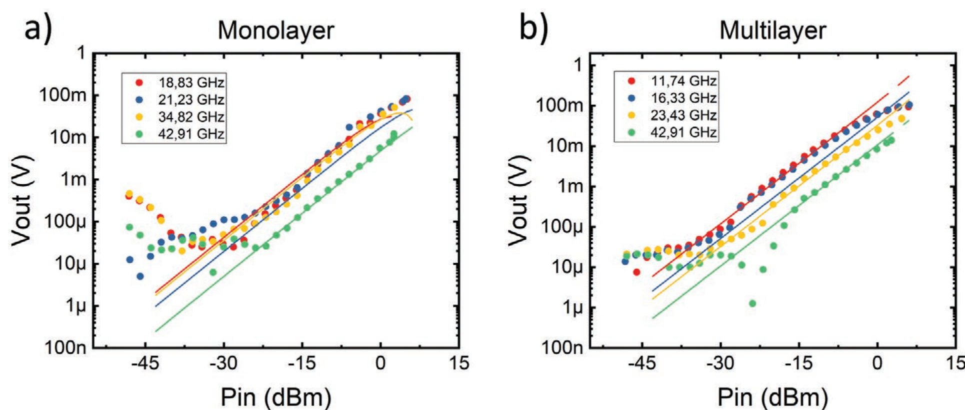

Figure 7. a,b) Performance comparison of the model-based simulation (solid lines) and measurement results (discrete points) in the monolayer (S) (a) and the multilayer (M) (b) devices.

to graphene diode-based power detectors and other FET-based circuits fabricated on rigid substrates.[14,60–62] The responsivity of the power-detector circuits is defined as

$$\text{Responsivity} = V_{\text{out}} / P_{\text{in}} \left[\text{V W}^{-1} \right] \tag{5}$$

where V_{out} is the output DC voltage and P_{in} is the input RF power. The M-transistors show a slightly better performance than the S-devices. Extracted from the slope in Figure 6b, the responsivity is presented in Figure 6c. The highest responses are at 16 and 11 GHz in the M- and 18 and 21 GHz in the S-devices, with measured responsivities of 104 and 134 V W^{-1}, as well as 45 and 49 V W^{-1}, respectively.

Some fluctuations can be observed in the responsivity plots (Figure 6c). Moreover, the theoretical maximum $f_{3\text{ dB}}$ was not achieved in measurements. This is (in part) due to the external components in the setup. Since the circuit relies on a nonideal resistive load for matching and a bias tee at the output, the varying insertion loss over the working frequency range of these devices affects the overall performance of the detector in different ways. The lack of matching prevents the input power from reaching the transistors, and the reflection at the bias tee may lead to spurious higher-order harmonics that lower the conversion efficiency. In order to verify this behavior and to validate the nonlinear resistance model implemented in Figure 5a, a harmonic balance simulation of the full power detector was performed, where the active device was substituted by the extracted equivalent circuit. The *S*-parameters of the 50 Ω load and of the output bias tee were measured and included in the simulation for higher accuracy. Moreover, two extra inductors were added at the output of both the VNA and of the circuit model to include additional inductance originating from the cables. The resulting comparison between simulations and measurements is shown in **Figure 7**a,b, where the output voltage is plotted over the input power for different frequencies. In agreement with the experimental results, certain frequencies present higher responsivities that are related to the matching in the circuit also in simulations. Simulations and measurements are in good agreement, and deviations are direct consequences of shifts in the matched frequencies caused by the inevitable discrepancies between the *S*-parameters used in simulation and the real external components, cables, and adaptors. Moreover, since the real components were included as *S*-parameters measured up to 40 GHz, higher harmonics were considered by interpolation in simulation. It is important to highlight that the model does not include the noise level, thus, it is not useful to determine the dynamic range of the detector. This is reflected in the simulations at low power levels in Figure 7a,b, where the model continues its linear behavior and deviates clearly from the experiments. Furthermore, the detectors are driven into saturation at high input power levels. To capture this effect in simulations, a large-signal model of the transistor would be required. These facts indicate that in addition to the successful demonstration of rectification at such high frequencies, even higher performance can be expected from a fully integrated solution with application-customized device structures, since this would avoid all the mismatches and tolerances from the external devices.

A comparison with the state-of-the-art power detectors built in different technologies based on, both, bulk semiconductors and 2D materials is summarized in **Table 3**, where all the selected designs are implemented using a single device. In ref. [63], the circuit is implemented in 130 nm CMOS technology, and whereas it presents a great responsivity, it is at the expense of a high DC power consumption and a limited bandwidth. On the other hand, refs. [64] and [65] are based on two different types of GaAs diodes, present excellent responsivities and higher bandwidth, but they are limited in dynamic range due to their high junction resistance and being cost inefficient. Furthermore, the three so far mentioned technologies do not allow their integration on flexible substrates. Then, graphene-based power detectors, reported in refs. [15] and [60] based on a graphene FET (GFET) and an MIG (metal–insulator–graphene) diode, respectively, have proved a higher dynamic range than standard technologies for a wide bandwidth at zero bias. Nevertheless, both designs, contrarily to our reported design, are based on rigid substrates and show lower responsivities. Therefore, this work demonstrates the potential of MoS_2 FETs as power detectors for flexible electronics, outperforming the responsivities of other single-device hybrid designs based on 2D materials.

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Table 3. Comparison of the power detector in this work with the state of the art of power detectors based on bulk semiconductors and other 2D materials.

Ref.	Technology	Substrate	Dynamic range	Power consumption	Responsivity	Frequency
[63]	130 nm CMOS	Si	43–50 dB	35.2 mW	23.5 mV dB^{-1}	4–6 GHz
[64]	GaAs tunnel diode	GaAs	20 dB	0 mW	400–1200 V W^{-1}	15–35 GHz
[65]	GaAs Schottky	Al_2O_3	25 dB	0 mW	6000–1000 V W^{-1}	90–110 GHz
[60]	GFET	SiC	45 dB	0 mW	71–33 V W^{-1}	2–110 GHz
[15]	MIG diode	Si	70 dB	0 mW	2.8–1.1 V W^{-1}	2–50 GHz
This work	Single-layer MoS2 FET	PI	30 dB	0 mW	104 V W^{-1}	16 GHz
	Multi-layer MoS2 FET		30 dB	0 mW	45 V W^{-1}	18 GHz

Finally, the M-material-based circuit was incorporated into a real system and characterized as an ON–OFF keying (OOK) signal demodulator at 16.8 GHz. This practical application of the power detector is shown in **Figure 8**a. The OOK modulated baseband signal was generated by the signal generator and upconverted to the 16 GHz band by a passive mixer. A local oscillator was provided by the vector network analyzer, whose maximum available power is 0 dBm. In order to compensate the power losses from the mixer, cables, and connectors, a 30 dB amplifier was used at the output of the mixer to guarantee a sufficient signal level at the input of the MoS_2 transistor. The voltage signal was measured by an oscillator with a 1 MΩ input impedance. The obtained waveforms at 1 and 100 kSymb s^{-1} modulation rates are shown in Figure 8b,c, respectively. The high responsivity of the power detector is demonstrated in the peak-to-peak voltage, equal to over 100 mV for the lowest rate. At 1 kSymb s^{-1}, the ON and OFF-states are clearly distinguishable (Figure 8b). At 100 kSymb s^{-1}, the symbols are still discernible, although the waveform is deformed, and the signal does not decay sufficiently fast when an ON-state immediately follows an OFF-state. This is because the circuit was optimized for its responsivity and linearity rather than demodulation. Therefore, the output bias tee together with the input impedance of the oscilloscope filters the signal and prevents higher modulation rates. Nevertheless, rates as high as 100 kSymb s^{-1} can be demodulated, and by incorporating an amplifier and comparator after the detector, the information can be digitally processed in a receiver.

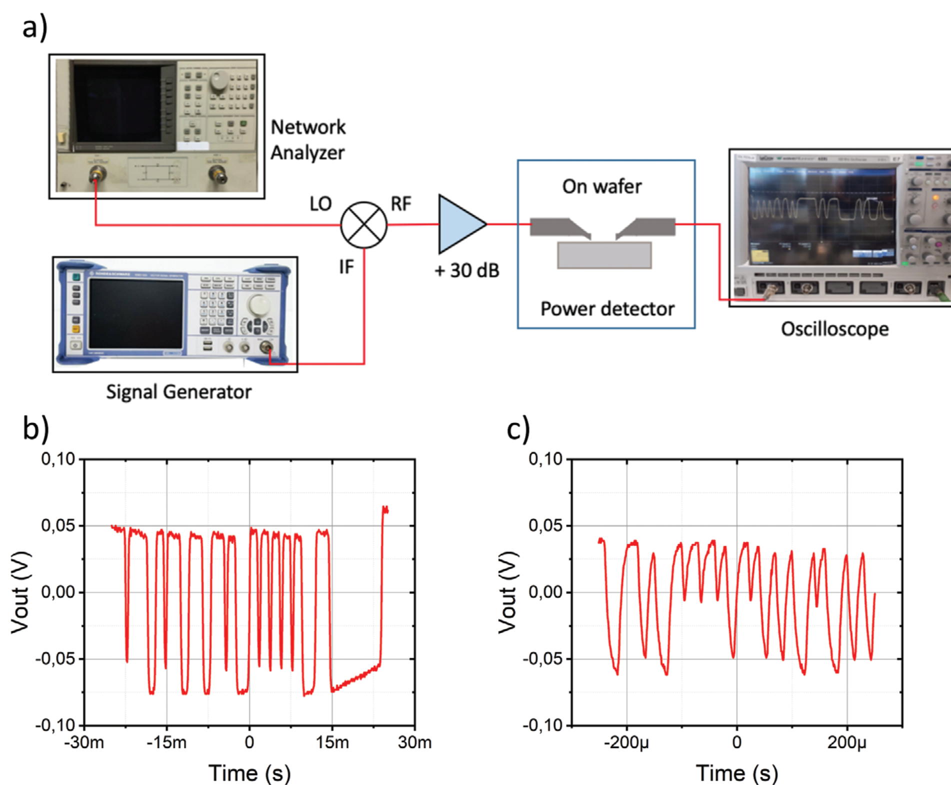

Figure 8. a) Block diagram of the OOK demodulator test setup for the multilayer material-based detector. b,c) The waveform response is obtained at the oscilloscope for 1 kSymb s^{-1} (a) and 100 kSymb s^{-1} (c), with the high and low values representing the ON- and OFF-states, respectively.

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4. Conclusions

MoS_2-based devices allow the monolithic integration of digital and analog circuits on the same flexible substrate. Nevertheless, MoS_2 FET-based microwave applications are limited by the performance of the transistors in terms of their f_T and f_{max}. In this work, zero-bias power detectors based on MoS_2 FETs are implemented for the first time. By relying on the nonlinearity of the channel, the operation frequency is far above the cutoff frequency reported for flexible devices up to date. The power detectors show also high performance in terms of dynamic range and responsivity and are in good agreement with simulation results, with the highest performances among the flexible technologies. It has been established that despite the good performance of other semiconductor technologies, MoS_2 allows the implementation of wide dynamic range power detectors with zero DC power consumption on flexible substrates. Furthermore, in contrast to other 2D material-based technologies, MoS_2 transistors are stable at room temperatures and do present a high ON/OFF ratio allowing the integration of full flexible transceivers. In addition, a circuit has been proven capable of successfully demodulating OOK signals with up to 100 kSymb s^{-1} rates at 16.8 GHz, ultimately demonstrating its potential application when incorporated into a real system. However, this work also shows that still some material growth and device processing parameters need to be carefully tuned in order to allow these circuits to meet the rigorous reliability requirements for mass production. Nonetheless, this work shows that the promising performance, the zero-power consumption, and the fabrication on a flexible substrate pave the way for exploiting this technology in the future bendable and wearable low-power electronic devices.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

2D materials, MoS_2 field-effect transistors, power detectors, radio-frequency flexible devices, zero power consumption

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